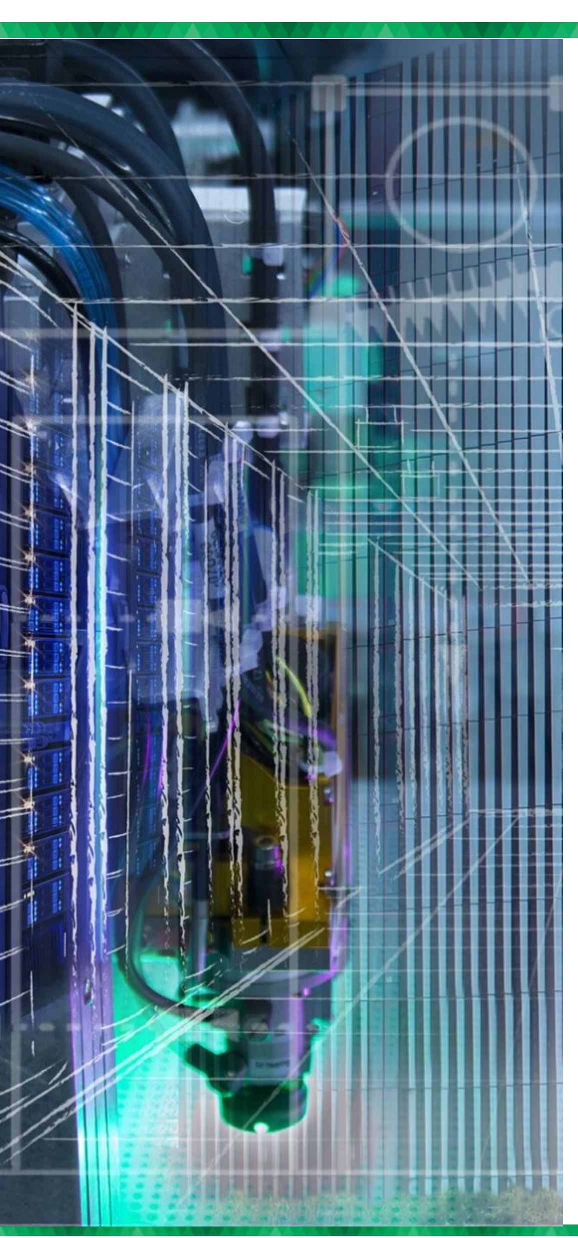


Submicron Die Attach: a key enabler for the future of Photonic-Electronic Systems

Pavel Seroglazov
BESI

EPIC Technology Meeting on Microelectronics & Photonics
Two Sides of One Coin

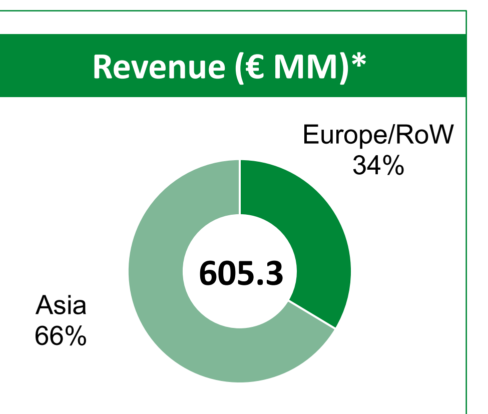
Attocube, Munich, Germany
November 17, 2025

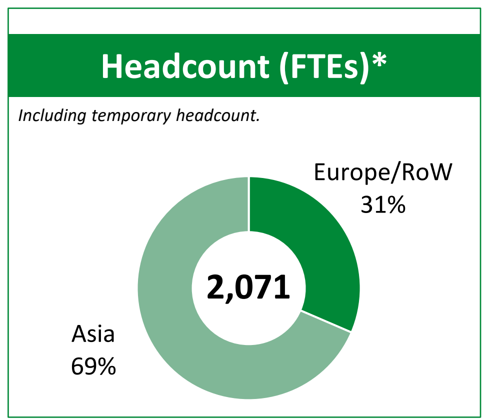
Besi at a Glance

Global Leader in Advanced Semiconductor Packaging Equipment

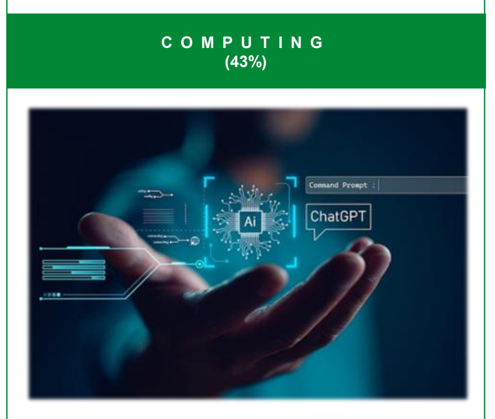
Founded

1995





Besi is a global leader in semiconductor assembly equipment:
high-precision and **high-throughput systems** for **Advanced Packaging.**



Worldwide Operations

Global infrastructure enabling local support and rapid deployment

- Research and Development
- Assembly and Manufacturing
- Sales and Service Office

Netherlands

China
- Leshan
- Shanghai
- Suzhou
- Chengdu

Leshan

South Korea

USA
(Chandler, AZ)

Switzerland

Austria

India

Taiwan

Singapore

Southeast Asia
- Thailand
- Vietnam
- Malaysia
- Philippines

Malaysia

Vietnam

Global Customer Network

Integrated Device Manufacturers	Fabless / OEMs	Foundries / Subcons
ams	AMD	ASE GROUP
OSRAM	BROADCOM	Amkor Technology
BOSCH	DELL	fabrinet
NXP	DELPHI	Carsem
intel	hp	HUA TIAN
Micron	lenovo	INNOLIGHT
RENESAS	MEDIATEK	LG Innotek
SAMSUNG	MOTOROLA MOBILITY	PTI
Texas Instruments	NVIDIA	SPIL
ST	QUALCOMM	SHARP
TDK		TF·AMD
SKYWORKS		JCET
FUJITSU		UTAC
ROHM SEMICONDUCTOR		tsmc
SEMIKRON DANFOSS		FOXCONN
infineon		
qorvo		

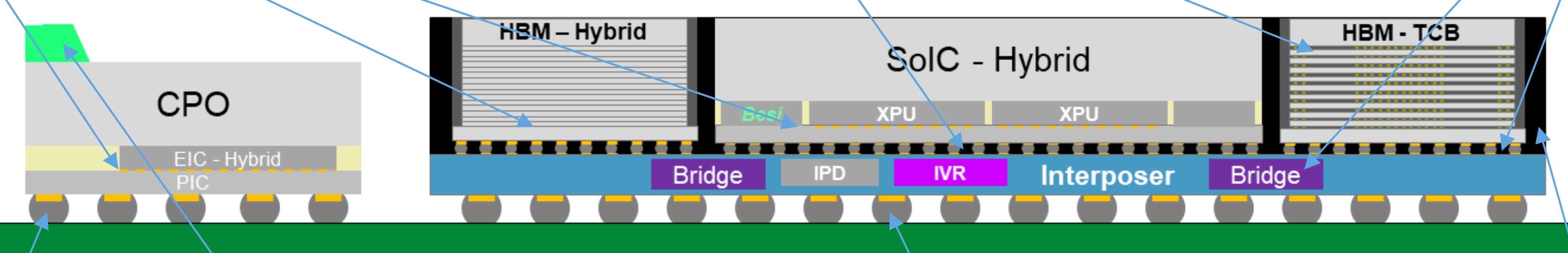
Non-exhaustive List

AI Chiplet Packages Require a Variety of Advanced Packaging Solutions

Hybrid Bonding
3DIC stacking < 9µm pitch
HBM stacking ≥ 16 High
Photonics

Thermo-compression Bonding
C2W chiplet stacking
HBM stacking ≤ 16 High
3D bridge attach

CoW Flip-chip and Fan-out
CoW flip-chip of logic & memory
High-density fan-out
Embedded bridge die attach



Flip-chip CoS
Advanced mass reflow flip-chip attach > 40 um pitch

Photonics
High precision optical component placement

Interposer Attach
oS bonding of large interposers up to 110 mm

Chiplet Molding
CoW encapsulation
CoWoS molded underfill

Besi Developing Complete Portfolio for Complex AI Chiplet Packages

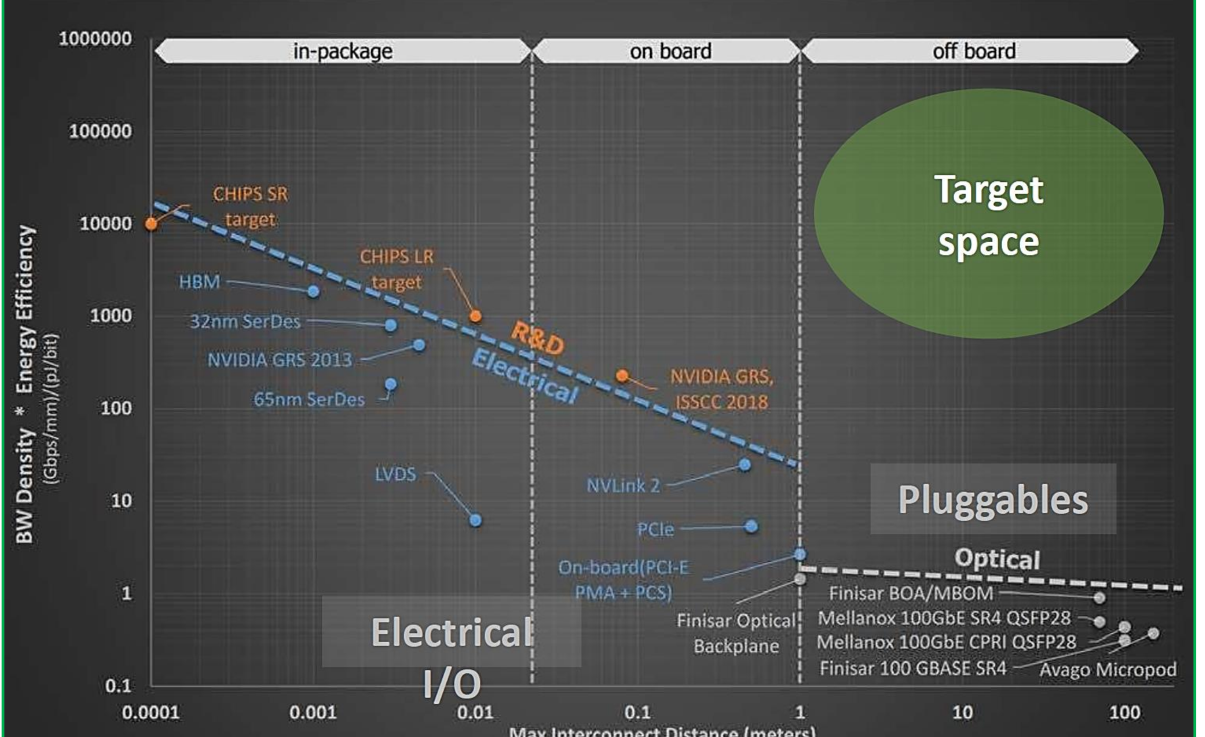
Hybrid Bonding	Thermo-compression Bonding	CoW Flip-chip and Fan-out
8800 CHAMEO UltraPlus AC	9800 TC Next (New)	8800 CHAMEO fleX (Q1-26)

HBM – Hybrid
SoIC - Hybrid
HBM - TCB
CPO
Besi
XPU
XPU
EIC - Hybrid
PIC
Bridge
IPD
IVR
Interposer
Bridge
Package Substrate

Flip-chip CoS	Photonics	Interposer Attach	Chiplet Molding
8800 Quantum AdvX (New)	2200 evo 1µm (Q1-26)	2200 evo Advanced	xMS-NXT (R&D)

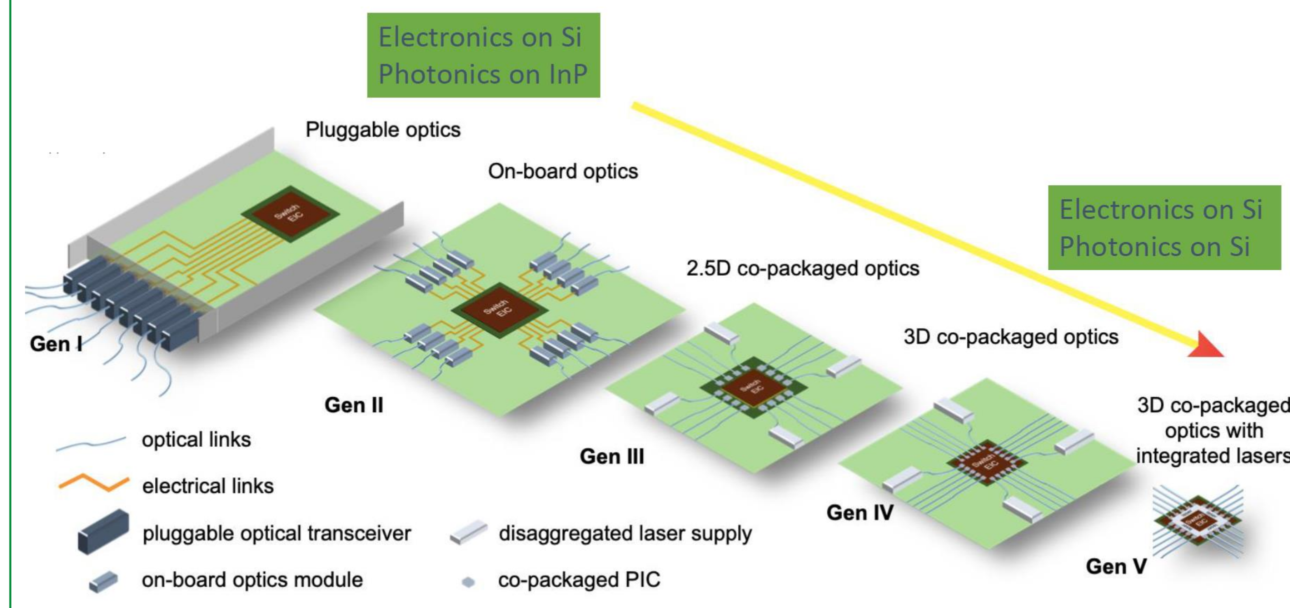
Photonic Engines as a Gamechanger

G. Keeler, DARPA PIPES Proposer's Day 2019



- Electrical I/O can support high BW density and low power, but **very short reach**
- Pluggable transceivers - **low BW density and high power**
- **Modern AI workloads hit a wall**: compute power ↑ **60,000×,** but I/O bandwidth ↑ **only 30×** (TSMC, 2025)
- Photonics becomes the only viable path

Margalit, Xiang, Bowers, Bjorlin, Blum, and Bowers, "Perspective on the Future of Silicon Photonics and Electronics", Applied Physics Letters Perspective, (2021)



Merging Photonics and Electronics: Tighter Integration is a solution

Bringing optics closer to the switch:

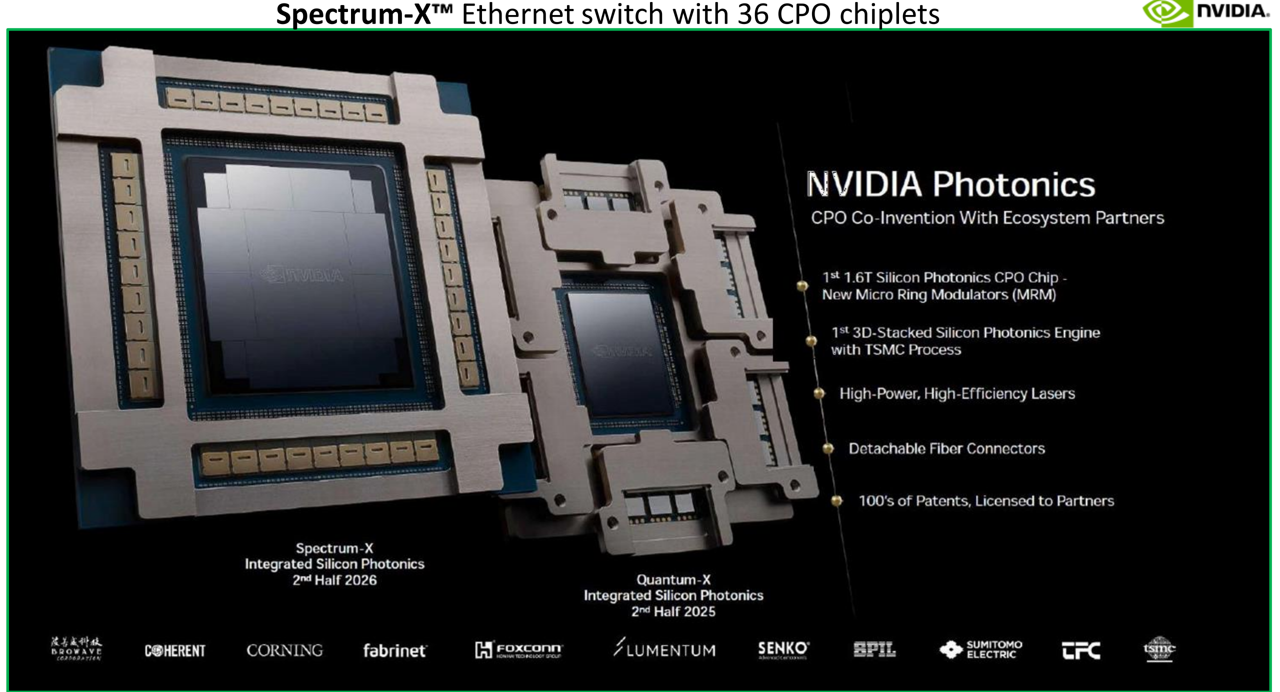
- **Increased** bandwidth (multi-Tb/s)
- **Reduced** power (electrical interconnect)
- **Reduced** latency (electrical interconnect)
- **Reduced** losses (less interfaces)
- **Smaller** footprint (size, cost)

Dr. David Harame Ph., 2025 IEEE 75th ECTC, AI Systems and the Role of Photonics and Co Packaged Photonics

CPO Use Cases Emerging in New Product Announcements

NVIDIA using D2W Hybrid Bonding in new network switch products using CPO

Spectrum-X™ Ethernet switch with 36 CPO chiplets



- Based on TSMC's COUPE technology that uses **D2W Hybrid Bonding**
- Up to **36 Hybrid Bonded Chiplets per switch device**
- Potential major driver for significant Hybrid Bonding capacity expansion through 2030

Broadcom's CPO network switches utilize multiple advanced flip-chip bonding processes

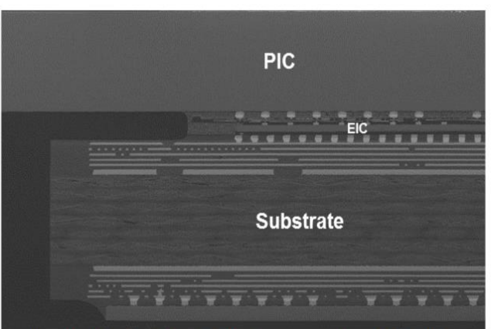
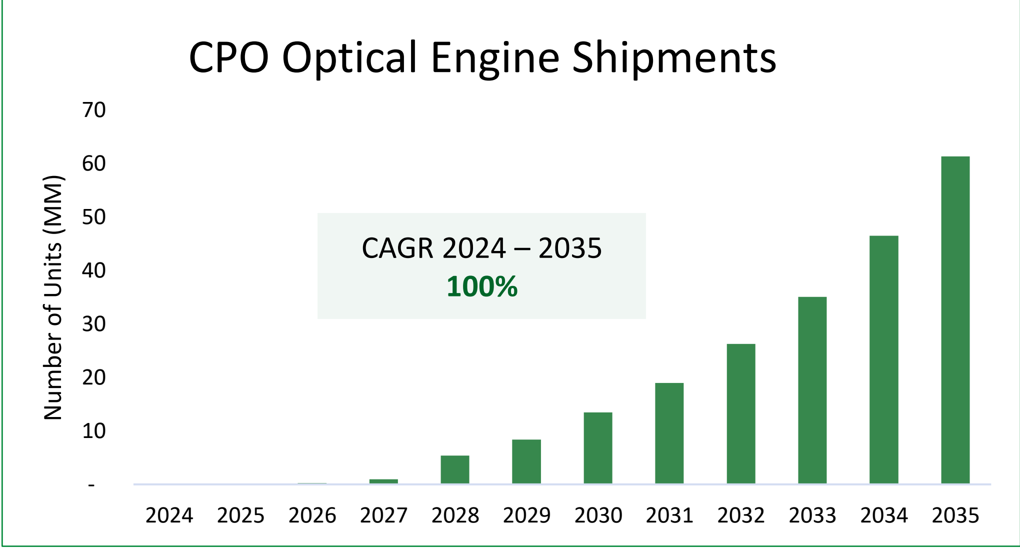


Fig. 9. The x-section of OE structure after TCN 500X

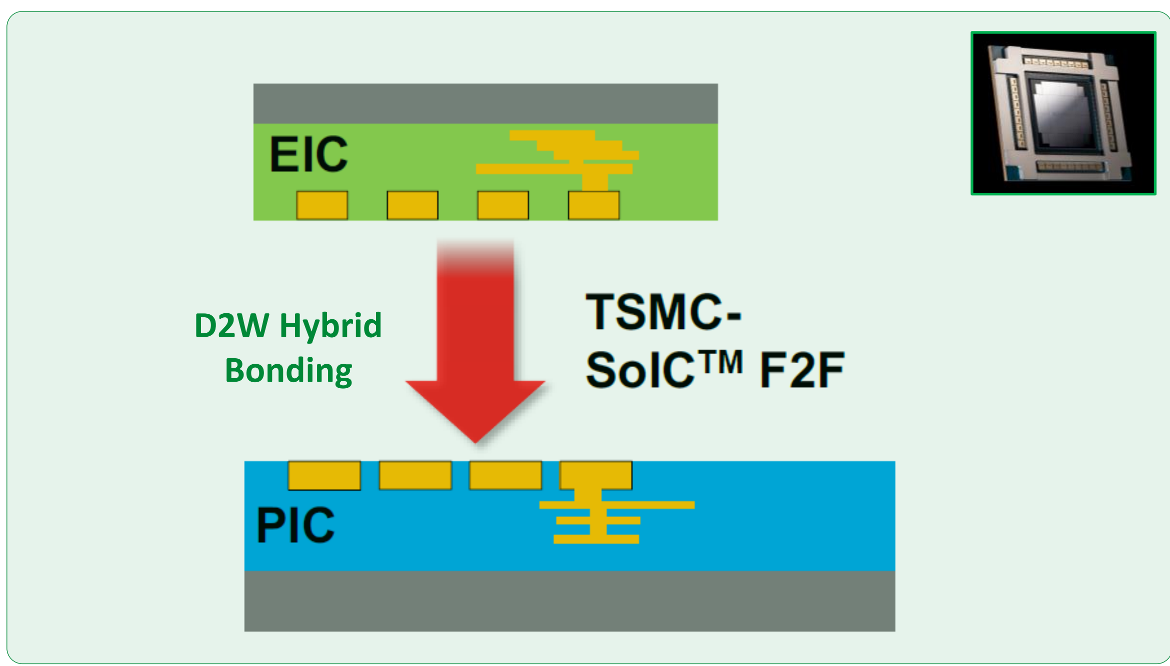
Source: Broadcom

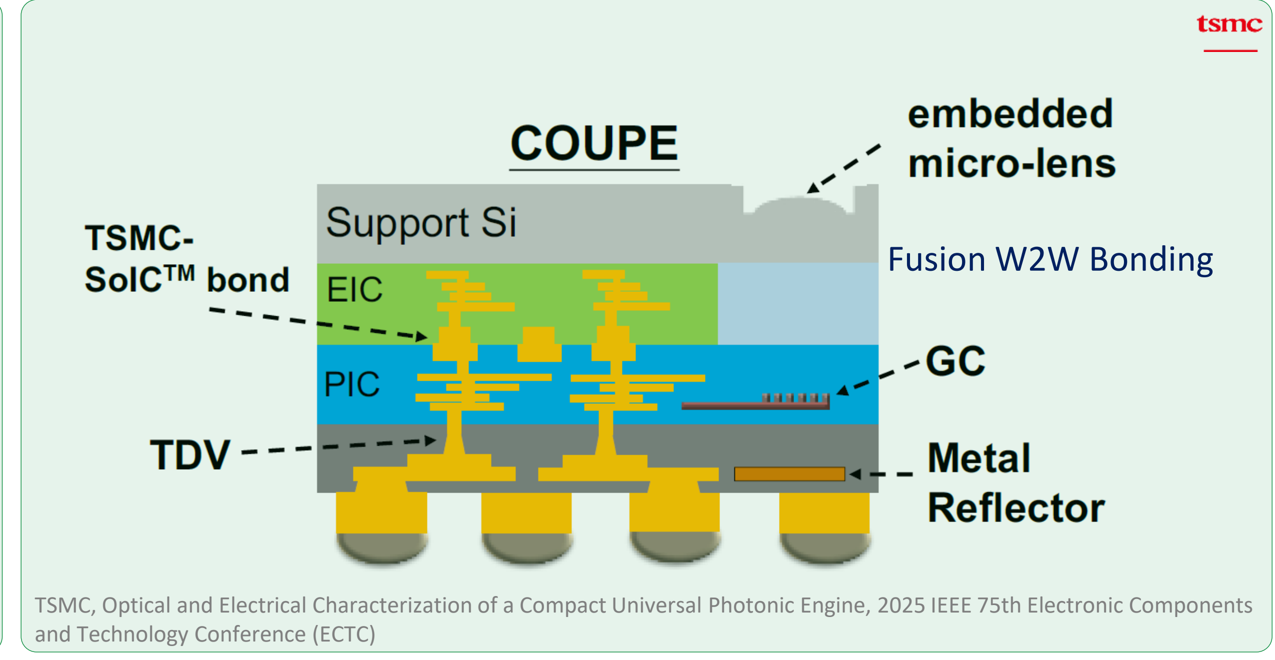


Source: Yole CPO 2025

COUPE architecture demands Advanced Sub-Micron Assembly

TSMC-SoIC™ face-to-face (F2F) technology for EIC and PIC bonding





TSMC, Optical and Electrical Characterization of a Compact Universal Photonic Engine, 2025 IEEE 75th Electronic Components and Technology Conference (ECTC)

Heterogeneous 3D stacking (PIC/EIC) unlocks:

- >100 GHz 3dB bandwidth
- 40% lower energy per bit (vs. electrical I/O)
- 170% speed increase at same power (TSMC-SoIC™)
- Net insertion loss within COUPE reduced to ~0dB

COUPE critical building blocks:

- TSMC SoIC™ bond, HB Chip-to-Chip interface: low impedance, decreased parasitic capacitance, lower energy consumption, improved signal integrity
- TDV structure: excellent RF characteristics
- Embedded Micro-lens and Metal reflector: lower optical losses

tsmc: "Heterogeneous 3D Integration becomes an obvious choice as the general solution for TSMC."

Industry Leading Edge Hybrid Bonding System

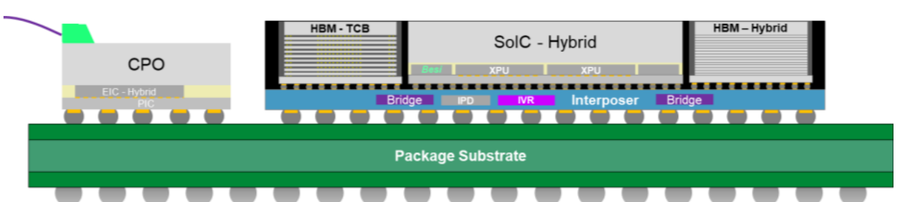
8800 CHAMEO ***Ultra Plus AC***

Key Competitive Advantages:

- Industry's First **HVM D2W Hybrid Bonder**
- Ultra-High Alignment Accuracy of **±100 nanometers**
- High Throughput up to **2,000 Units Per Hour** (UPH)
- Proven High Production Yields
- **ISO 3 Cleanroom** Compliance
- Full Front-End Automation in collaboration with ***Applied Materials***

>100 Systems Shipped

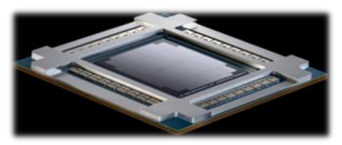
KEY APPLICATIONS:



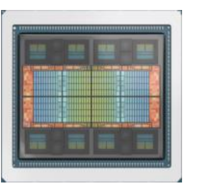
Packaging Technology: CoWoS, SoIC, Foveros Direct, Co-packaged Optics, HBM

Samsung smart glasses (Prototype)

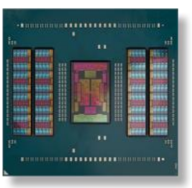
Nvidia Spectrum X Network Switch



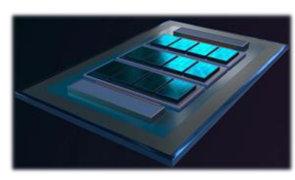
AMD MI325 GPU



AMD Zen 5 EPYC CPU



Intel Clearwater Forest CPU



High Performance Computing; CPU, XPUs, Optical Engine, Displays

Besi Hybrid Bonder – Highest Accuracy and Lowest CoO

Logic roadmap – driven by accuracy

2 — 8800 HYBRID G2 Launch in 2026

50nm accuracy enables even smaller pad pitches

Bump Pitch: <3µm

Accuracy 50nm

Significantly higher UPH decreases CoO for HBM

Higher Die stacking UPH

3 — Roadmap to 25nm and beyond

- Development for 25nm and beyond ongoing
- Enabling transistor to transistor interconnect at 1µm pad pitch by 2030

Bump Pitch: <1µm

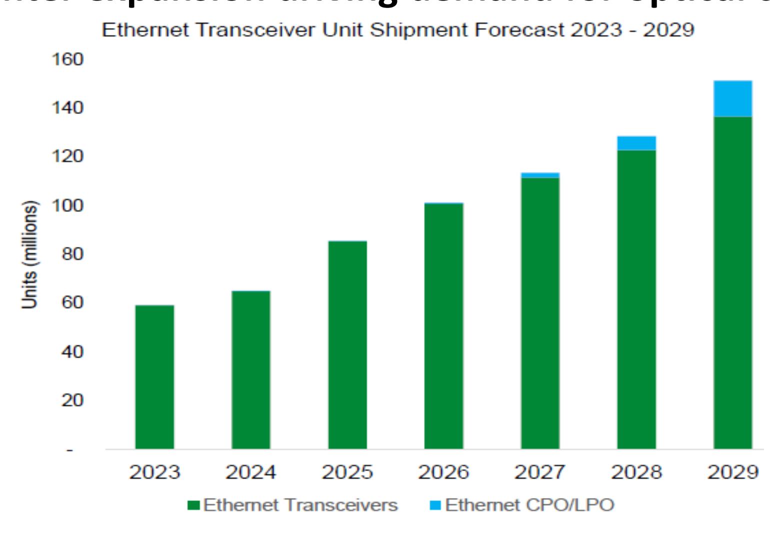
4 — Improving HBM CoO

- Increasing UPH further to enable cost effective stacking ≥16 high
- While achieving high accuracy for advanced memory architectures with custom logic base die

Memory roadmap – driven by throughput

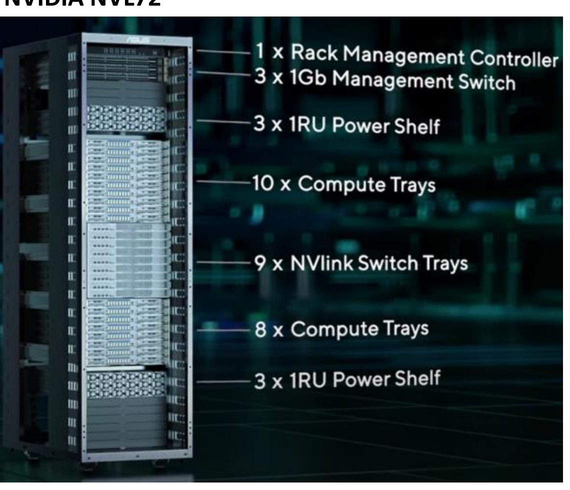
Besi's Multi Module Attach System: Leading Photonics Platform in Rapidly Growing Market

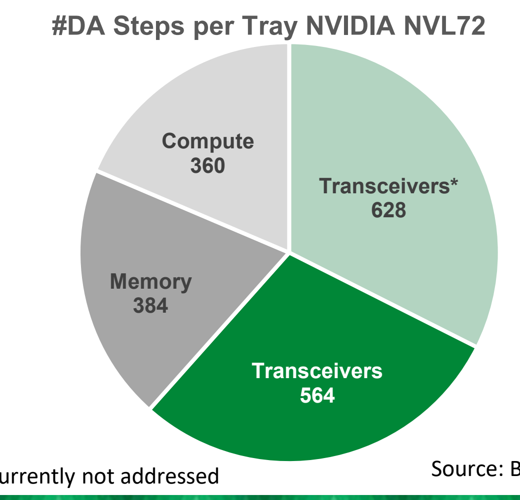
Data center expansion driving demand for optical connections



Optical transceivers in today's AI servers require a significant number of die attach steps

NVIDIA NVL72



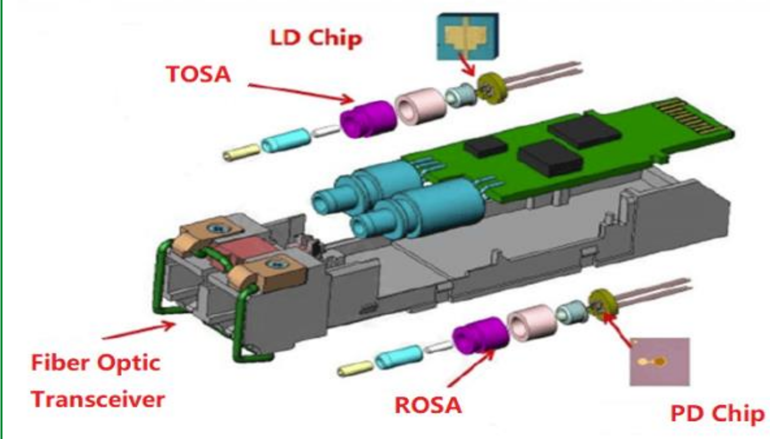


* Currently not addressed

Source: BESI

Besi # 1 player in optical transceiver assembly working with all key players

Typical Optical Transceiver Assembly



Source: Nvidia

fabrinet

molex

eoptolink

2200 Evo Advanced

- Best combination of placement accuracy and productivity
- Ultimate process control
- Global installed base with industry leaders

NEW Evo 1um (2026)

Introducing new **1um accuracy** system to increase optical transceiver market share

Photonics Integration – A Call for Collaboration

- New CPO systems demand **new packaging** and **bonding solutions** that deliver **higher bandwidth** at **lower cost** and **power**.

- Innovation through **co-process**, **co-design** and **co-packaging** will define the next phase of integration.

- BESI brings **Advanced Die Attach**, **Hybrid** and **Fusion bonding** expertise to enable scalable photonic packaging.

- **We invite industry and research partners** to co-develop and qualify next-generation packaging solutions.

Centers of Excellence and Demo Centers

Netherlands

BESI Netherlands (Duiven)

BESI Netherlands (s-Hertogenbosch)

Molding, Trim & Form, Singualtion, Wet processing)

imec (Leuven, Belgium)

(Hybrid Bonding, TCB)

BESI North America (Chandler)

(Multi-Module Attach)

University of Texas (Austin)

(Hybrid Bonding)

BESI Switzerland (Steinhausen)

(Epoxy & Soft Solder Die Attach)

BESI Austria (Radfeld)

(Hybrid Bonding, TCB,
Flip Chip, MMA, DLA-DSA)

BESI Singapore

IME A*Star

(Hybrid Bonding, TCB, Flip Chip,
MMA & Molding)

Thank you

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Two Sides of One Coin

Attocube, Munich, Germany
November 17, 2025

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