From Lithography to Light
Scaling Compute Beyond Shrink

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Setting the Stage
Enabling Moore's Law

ZEISS SMT has driven Moore's Law* for decades — enabling transistor counts to double every two years. This translates into a continuous **roadmap** for feature-size reduction ("shrink").

*rather a self-fulfilling prophecy

However dimensional shrink is slowing down …
… do we start to hit the limits of exponential growth?

pitch (logscale)

Moore's Law (in density) "2x / 2 years"

today

Observed Nodes

Forecast

shrink expectations are shifting

N2 A14 A10 A7 A5

1998 2003 2008 2013 2018 2023 2028 2033 2038

Thomas Stammler, ZEISS Technology Conference 2025

On the horizon a massive demand for powering AI chips …
… and it's not only about training.

Confident
Likely
Speculative

Training Compute (FLOP)

10^{26}
10^{23}
10^{20}
10^{17}
10^{14}
10^{11}

4.2x / year

1.5x / year

compare with Moore's law 2x/2years

Deep Learning Era

2000 2004 2008 2012 2016 2020 2024

EPOCH AI

Notable AI models from https://epoch.ai/data/ai-models

A two-fold challenge: exploding AI demand & slowing shrink → heterogeneous integration / advanced packaging

computing demand or transistor density [a.u.]

requirements for AI data centers

gap

today

Moore's Law 2x / 2 years

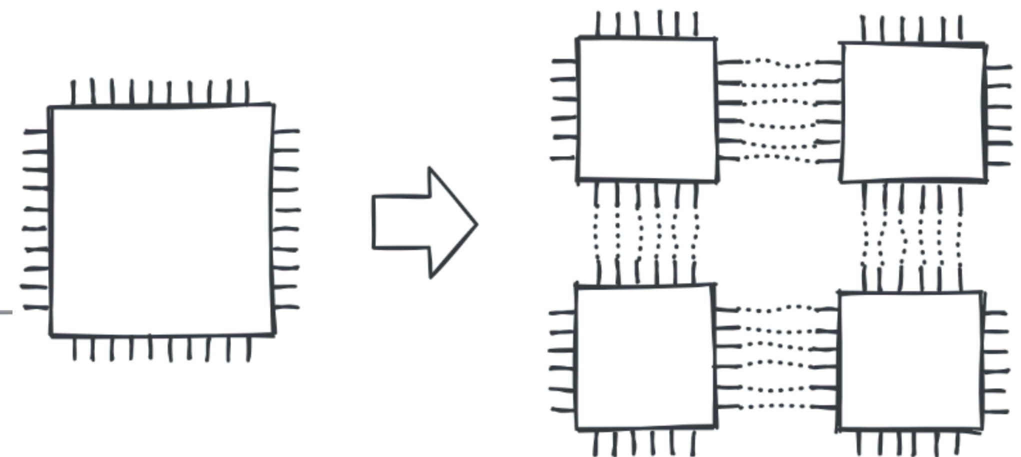
shrink slowing down

1998 2003 2008 2013 2018 2023 2028 2033

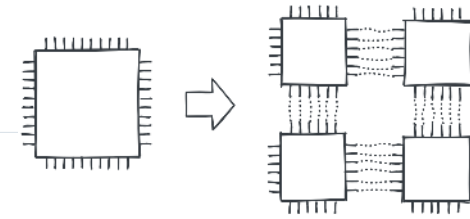
There's an increasing two-fold performance gap

1. exponentially growing demand for AI which by far outpaces Moore's law.
2. traditional dimensional shrink-based improvements are slowing down.

→ we need scale beyond shrink.

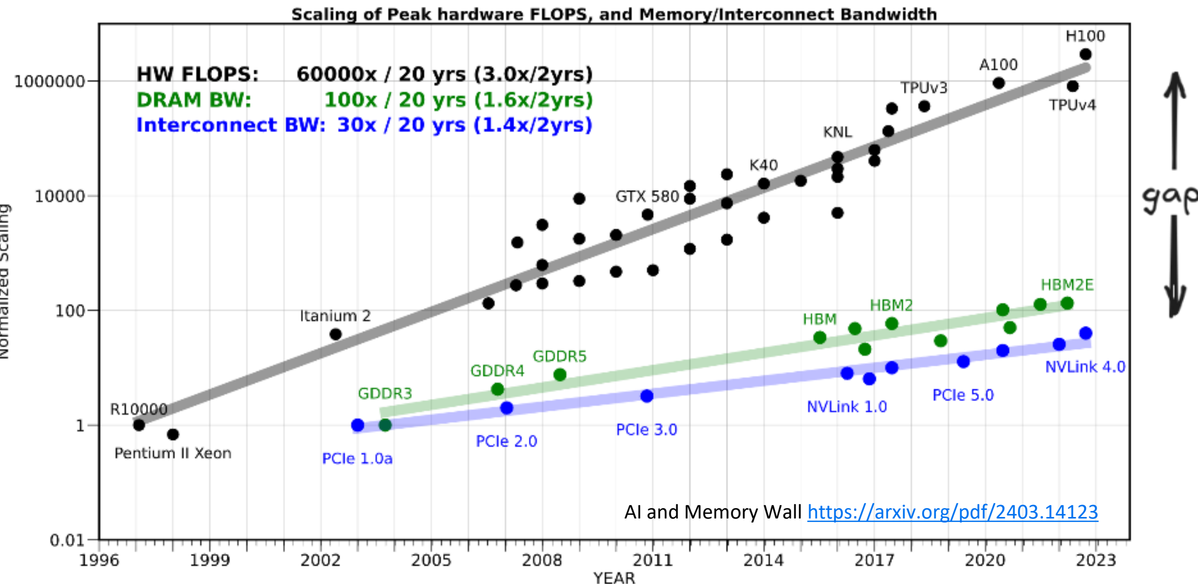


scaling beyond Moore's Law …
… implications of heterogeneous integration



AI Computing is fundamentally a data management task.

The gap widens between processing and datacom BW.



Chiplet integration with advanced packaging demands ultra-fast, energy-efficient communication.

Limits of Electrical Links:

- **Bandwidth bottleneck** (+ "beachfront-limited"):
- **High energy per bit** → scaling increases power and heat.

Photonic Links Advantage:

- **Massively higher bandwidth**
- **Significantly lower energy per bit**

Switching from pluggables to CPO cuts energy use by ~4×.

→ Only photonics can deliver the speed and power efficiency needed for next-gen AI and HPC systems.

From Moore's Law to More Ways: scaling compute for AI

A cross-technology plan — lithography, packaging and photonics

EUV ← Shrink

Advanced Packaging

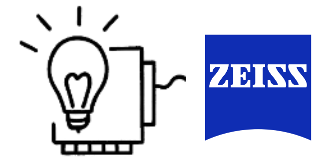
on-package optical I/O

ZEISS SMT main business but not covered today

X-ray inspection

waveguide writing
PIC Testing

From Moore’s Law to More Ways: scaling compute for AI
Ambition, scope and approach with on-package optical I/O.



We prepare technology for ZEISS as an *equipment provider* for on-package optical I/O.

Guiding Principles

Material & Platform Agnostic
Flexible approach across technologies.

Leverage Existing ZEISS Capabilities
Accelerate development for HVM solutions by building on proven technology and stages.

Manufacturing Technology
Deliver robust solutions for high-volume production.

Metrology & Functional Testing
Ensure precision and performance at scale.

Assembly Support
Facilitate seamless integration into customer workflows.

Scope

1. ***Co-packaged optics***
2. ***chiplet communication on large photonic interposers***

Approach

Leverage lithography relationships with leading customers to capture requirements and gain insight into photonics roadmaps.

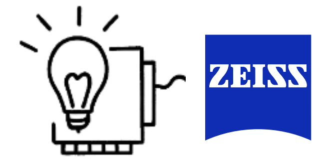
Actively partner with other companies across the value chain to combine strengths, create synergies, and drive innovation.

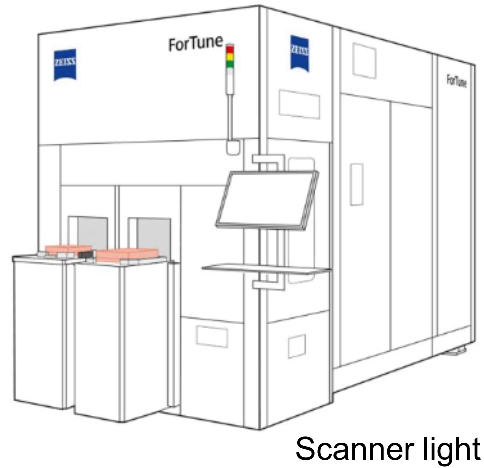
Collaborate with R&D partners through joint projects to accelerate technology understanding.

Develop demonstrators and prototypes to enable rapid feedback from customers and partners – “fail fast”.

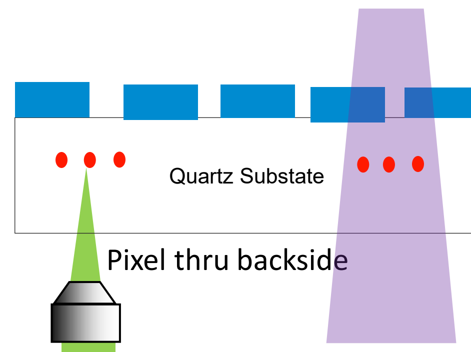
3D waveguide writing – detour – photomask tuning …

… enabling laser direct write beyond photomasks

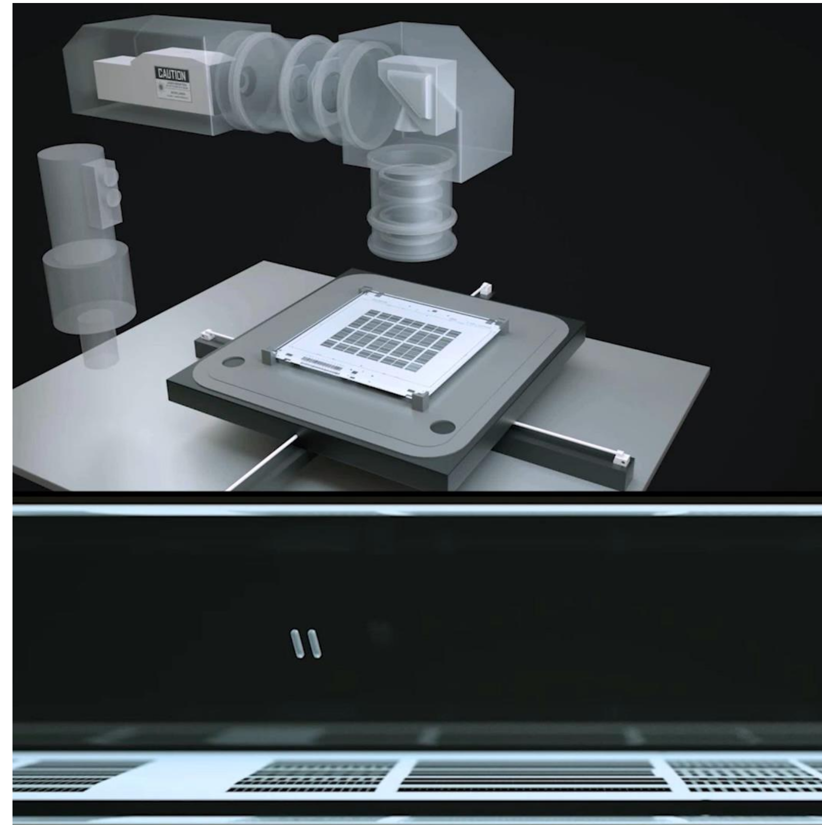




Scanner light

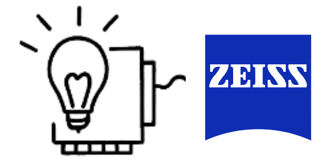


- overlay control
- CDU Control



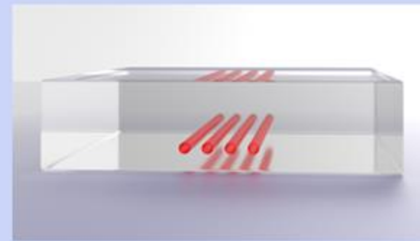
- The ZEISS ForTune System generates pixels in substrates to improve critical-dimension-uniformity (CDU) and overlay by using ultrashort laser pulses
- Well established technology for 15+ years
- installed base at mask shops and wafer fabs of major device makers (memory and logic)

3D waveguide writing – retrofitted mask-tuning platform
Laser direct write enables precision 3D waveguide writing in glass

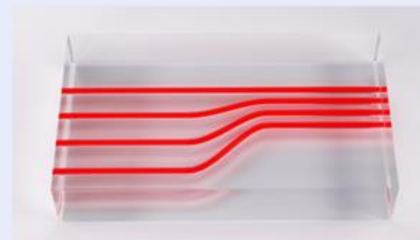


LDW 3D waveguide writing

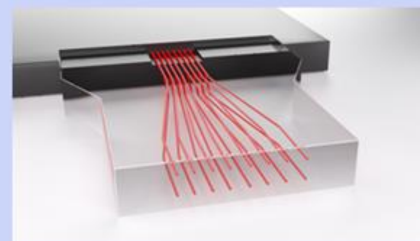
Straight WG



2D curved WG



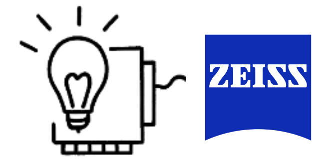
3D WG



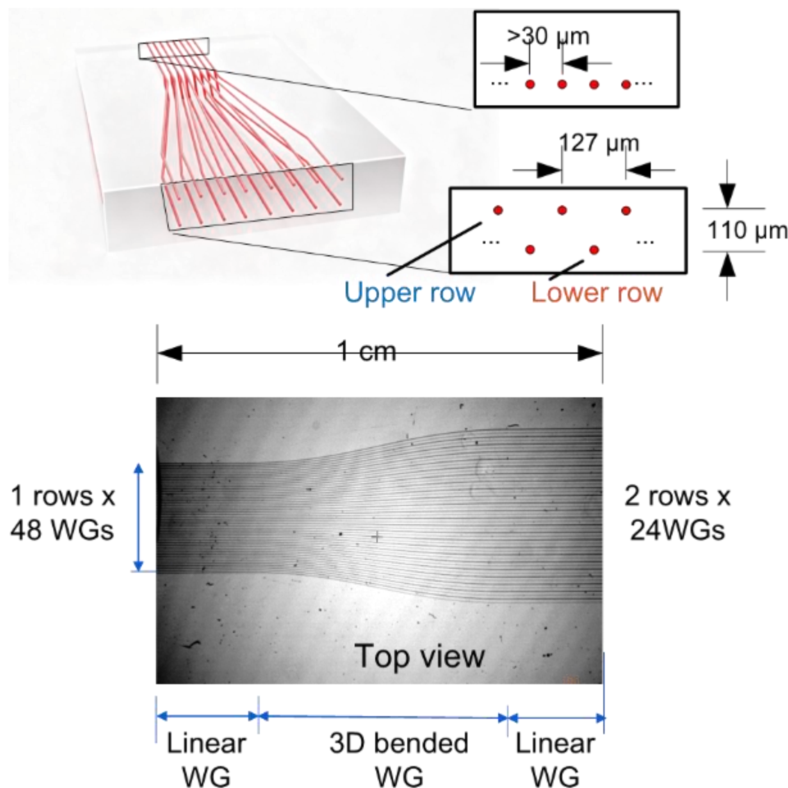
Industrial ZEISS platform with NIR wavelength ultra-short pulse laser adapted for waveguide laser direct writing (LDW) in glass proof-of-principle demonstration.

- Mode field diameter compatible to optical fibers
- Writing Speed → HVM ready

3D waveguide writing – proof of concept: 3D arrays
Performance metrics

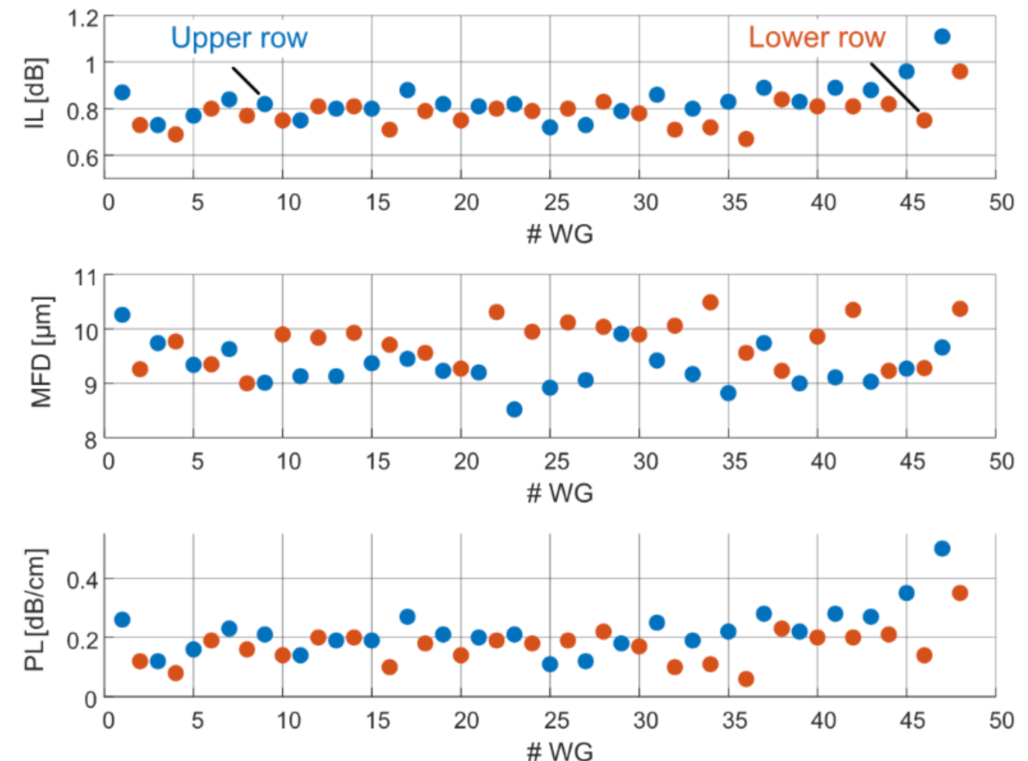


Schematic of 3D waveguides. On one side of the sample, the waveguides are arranged in one row. On the other side of the sample, a two-dimensional array is formed with a pitch of 127µm and a vertical distance between the two rows of 110 µm.



Measurement results of all 48 waveguides.

- **Top:** insertion loss (IL) incl. free-space coupling loss
- **Middle:** mode-field diameter (MFD) of waveguide
- **Bottom:** estimated propagation loss (PL)

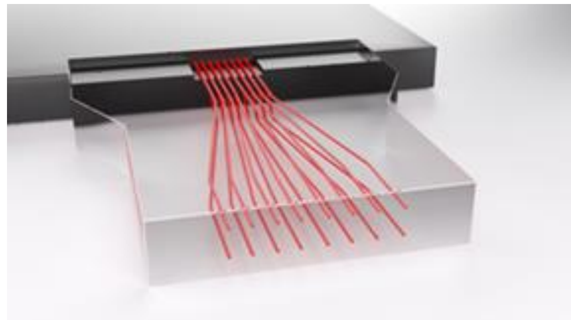


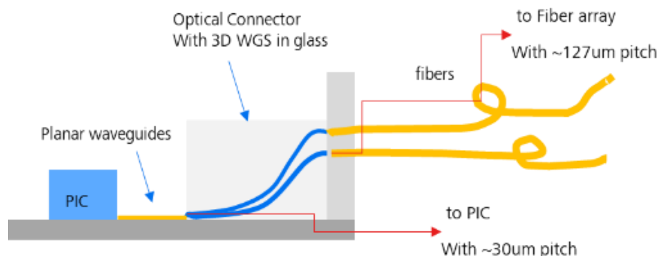
3D waveguide writing – scaling connectivity with light
Optical connectors, glass interposers, TGV, and refractive-index tuning

Optical Connector

3D routing – reduce beachfront in Fiber to PIC Coupling.

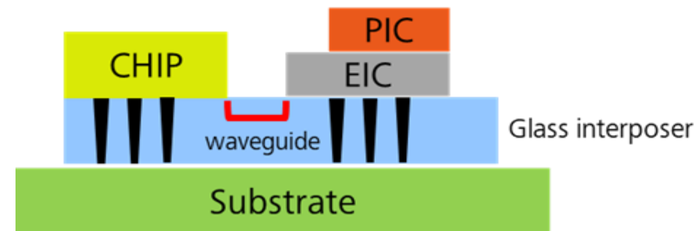
Write waveguide on package to match exactly the (edge or grating) coupler.





Glass interposers or panels

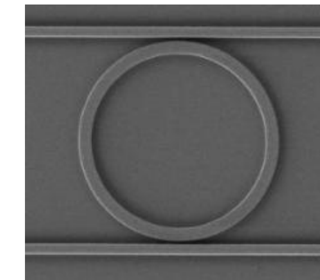
Waveguides in glass for optical connections including 3D routing.



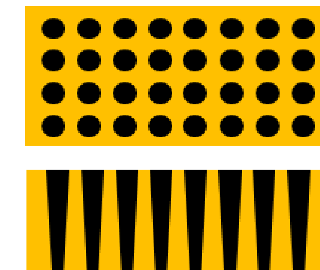
Further applications

Manipulate refractive index in glass or Si:

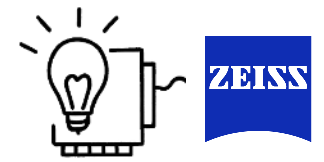
→ tune / optimize / correct photonic structures



Through Glass Vias (TGV) by Laser Selective Etching



PIC Testing
State of the art functional testing



Cascade Microtech

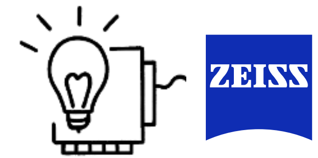
Injecting light into waveguides using fibers

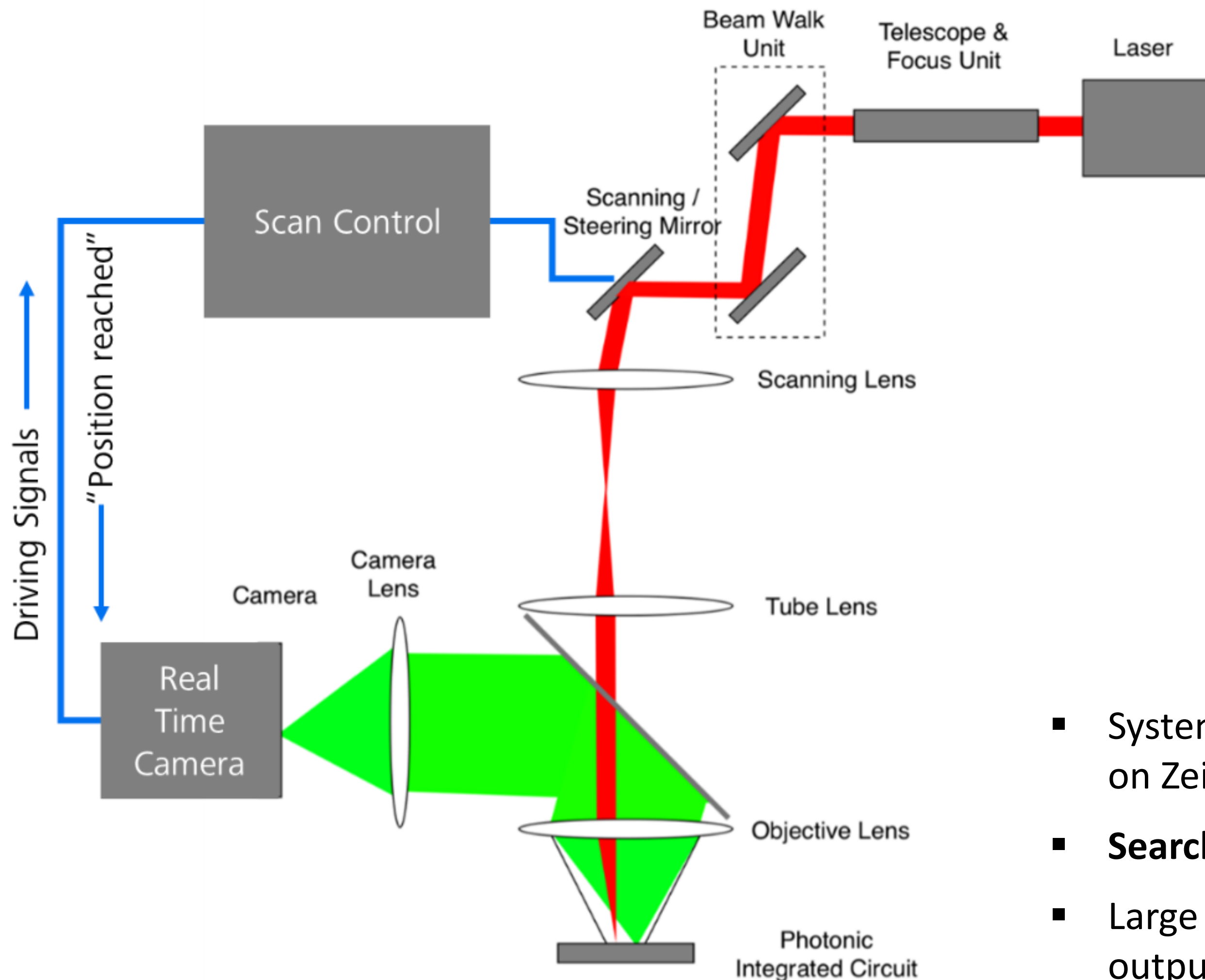
Required Position Accuracy:
< 500 nm

Fiber Alignment Speed:
Slow, ~ a few hundred milliseconds

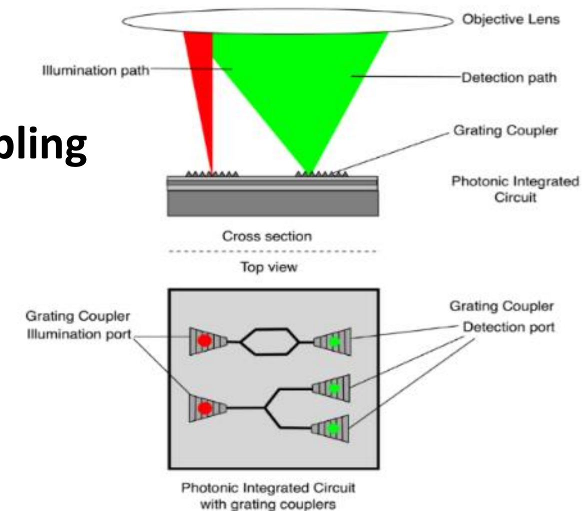
Full Wafer Test Duration:
Several hours

PIC Testing – high-throughput functional testing of PICs
Ultra-fast free-space optical coupling



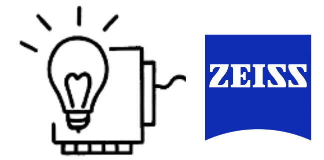


Top Side Coupling



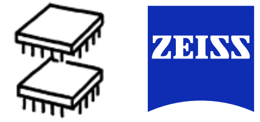
- System for functional testing of photonic integrated circuits based on Zeiss LSM microscopy systems
- **Search and coupling of light into PICs in ~ 10ms**
- Large working distance – can be combined with electrical input and outputs via e.g. probe cards

PIC Testing – Status …
… it’s still a lab setup.



- Demonstrator set up including soft- & firmware for in-situ scan control and experimental validation
- Very encouraging feedback from several leading customers
- Customer test chips expected in the next weeks

3D inline X-ray inspection – challenges in advanced packaging
Process-control calls for measuring and inspecting *inside* the package.



Advanced 3D Integration

- Last-processed layer no longer on the surface
- Sub-10µm interconnect structures require more process control
- Ideally, non-destructive testing on many samples to detect, measure and counter-act on
  - Die-overlay
  - Cold-joints
  - Chip-gap and –tilt
  - Bridging
  - Missing bumps

Solder Bump

Fatigue Cracks

TSV Voids, Seams

100 um

Micro-bump Voids

50 um

Memory

Logic

Analog

Silicon Interposer

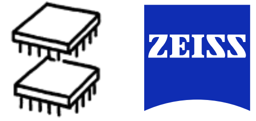
Micro-bump Short

BGA Laminate

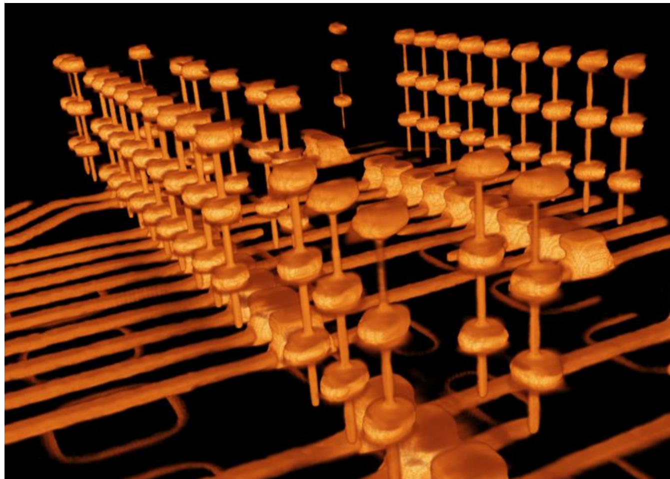
Broken Vias

PCB

3D inline X-ray inspection – ZEISS NLX-100 system
A system designed for supporting semiconductor process control needs



- **Fully-automated X-ray system** for inline wafer inspection
- Consistent **high-quality 3D-imaging** across the wafer
- ZEISS X-ray source for **high throughput & high resolution**
- **Automated** data analytics
- **XGuard** shielding & dose control for protecting X-ray sensitive areas like HBM
- **Optical alignment** to minimize X-ray dose



Summary

Beyond Shrink: New Scaling Paradigms and Scope

Advanced Packaging & Photonics

Co-packaged optics: Key to scaling bandwidth, reducing energy, and latency.

Large photonic interposers: Enable heterogeneous integration (CPUs, GPUs, NPUs, HBM).

ZEISS ambition: Equipment for on-package optical I/O industry.

Examples: Tech. Demonstrators

3D Waveguide Writing:

Laser direct-write for photonic integration in glass. Enables high-density, low-loss optical connections with 3D-routing.

High-Throughput PIC Testing:

Free-space optical coupling for rapid, precise photonic chip testing.

3D Inline X-ray Inspection:

Automated, high-resolution process control for advanced packaging.

(further demonstrators for wafer warpage correction and particle removal are in the pipe)

Approach

Leverage customer relationships

… to capture requirements and gain insight into photonics roadmaps.

Actively partner with companies

… across the value chain to combine strengths, create synergies, and drive innovation.

Collaborate with R&D partners

… through joint projects to accelerate technology understanding.

Seeing beyond