光电子集成
晶圆级测试的内容、方法和技术挑战

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关于EXFO

95+
of leading service providers using EXFO

No.1
in optical test solutions

250+
assurance systems deployed

5000+
Certification & Recognition

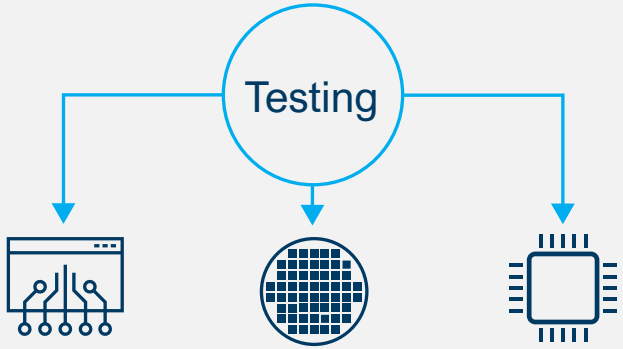
40
years of pioneering essential solutions and technologies

1,900+
employees in 25 countries and customers in 120 countries

为什么PIC产业中测试非常重要?

1

Testing is required to validate & enhance PIC from wafer, die, assembly to module.



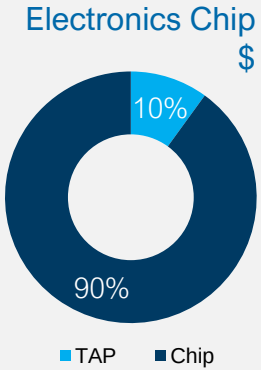
Design
Wafer / Die
Full characterization
Optical & Electrical

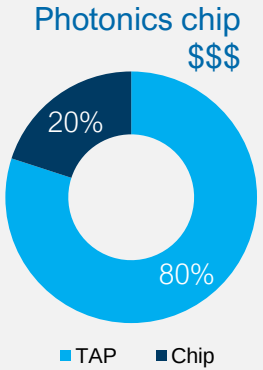
Production
Wafer / Die
Find known good dies (KGD)

Deployment
Assembly / Module
Final tests

2

Known Good Dies (KGD) are essential to make TAP (Testing, Assembly, Packaging) viable.

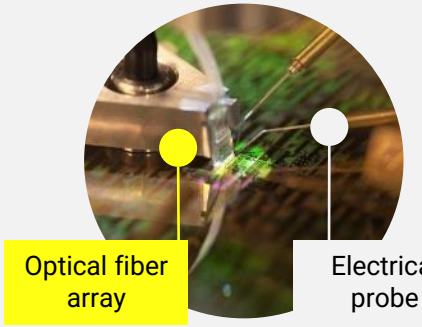




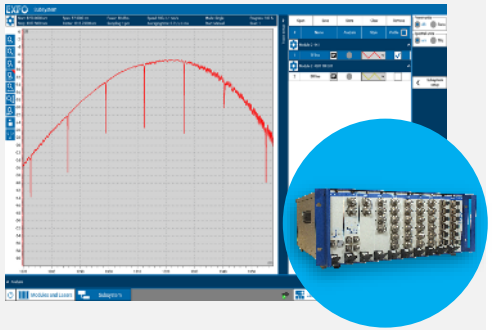
GOAL **Efficient testing to find KGD**

PIC 晶圆级测试及挑战

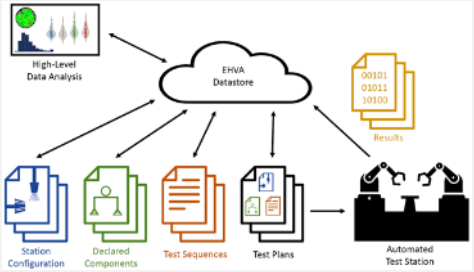
1 Optical coupling and electrical probing

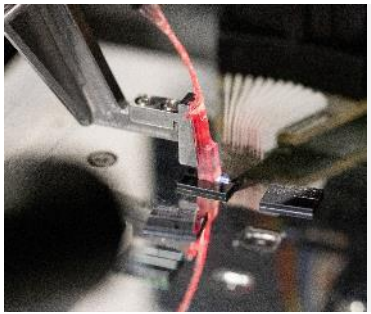


2 Optical and electrical testing



3 Data management and analysis





Bottlenecks

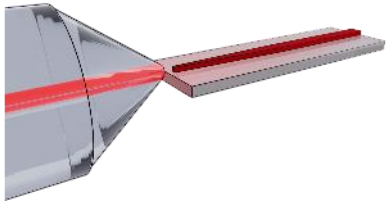
- Accuracy and repeatability
- Speed and efficiency
- Data intelligence
- Dealing with complexity
- Flexibility / Scalability
- Ecosystem

光耦合与测试

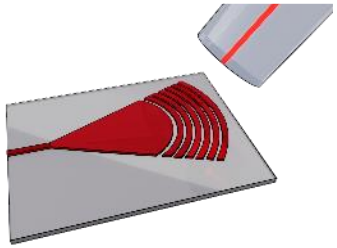
PIC requires edge coupling
for product performance and efficiency

Wafer-level edge coupling
optimizing both accuracy and efficiency

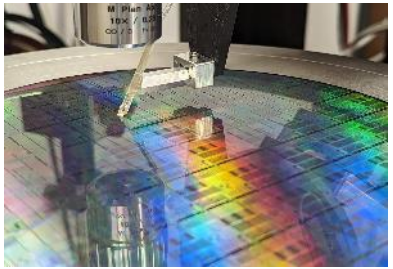
edge coupling

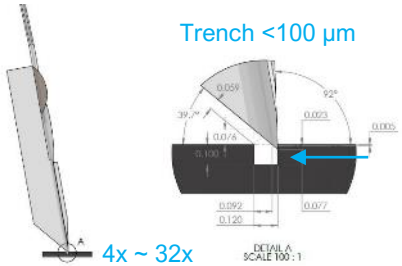


surface coupling



Wafer-level edge coupling





Edge coupling vs. surface coupling

- High coupling efficiency 1 dB or lower (vs. >3dB)
- Broad bandwidth 100 nm (vs. 30 nm)
- Low PDL ~0 dB (vs. 1~3dB, more if TE/TM only)
- Needs cleaved facet, spot-size converter
- Challenging to probe at wafer-level

OPAL-EC enables edge coupling on wafer

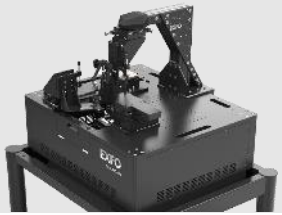
- Save time and cost versus singulated dies (separate dies, pick & place)
- Best accuracy and repeatability with low dependency in loss, bandwidth & PDL
- Multi-port for parallel testing, phase arrays & sensors

从晶圆至DIE的可升级探针测试台

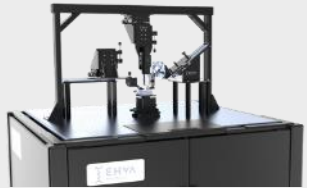
CIOE Demo
Booth 10B53

OPAL EC
Wafer testing
(up to Ø 300mm)

OPAL MD
Multi-die testing
(100x100 mm²)

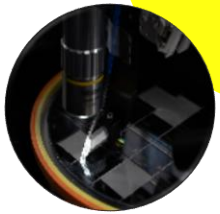


OPAL SD
Single-die testing
(50x50 mm²)



All form factors

300mm wafer, bar, single & multiple dies
Stretch-tape



Modular design

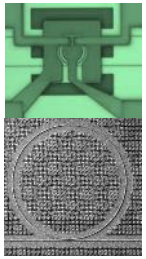
Up to 4x Optical and Electrical probes
Scalable SD, MD to EC

Multi-port wafer-level edge coupling + surface coupling

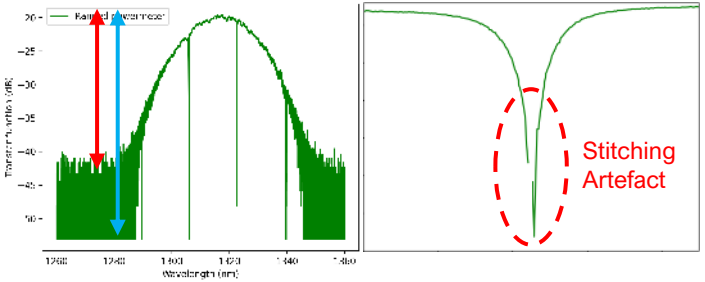
Automated stations with PIC dedicated software

光测试挑战：
微腔（RING RESONATOR）测试（用例）

High Q-factor Ring Resonators testing challenges

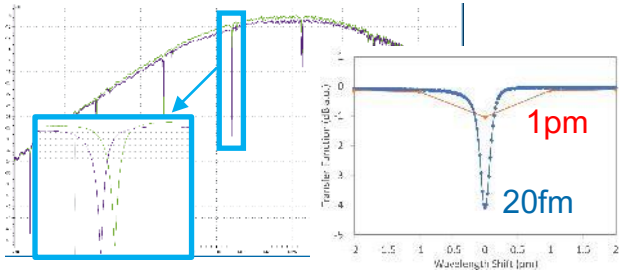


>1,000,000 Q-factor



Limited dynamic range and resolution

High-performance testing for Ring Resonators



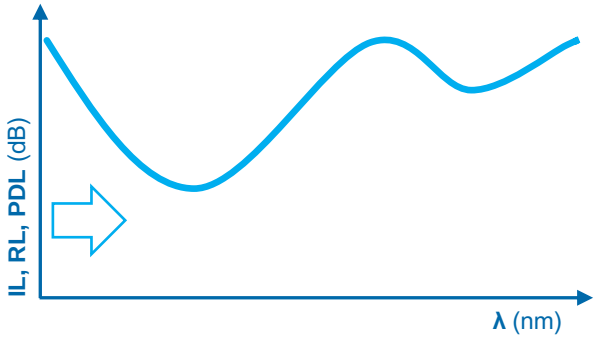
>70dB dynamic range and 20fm resolution

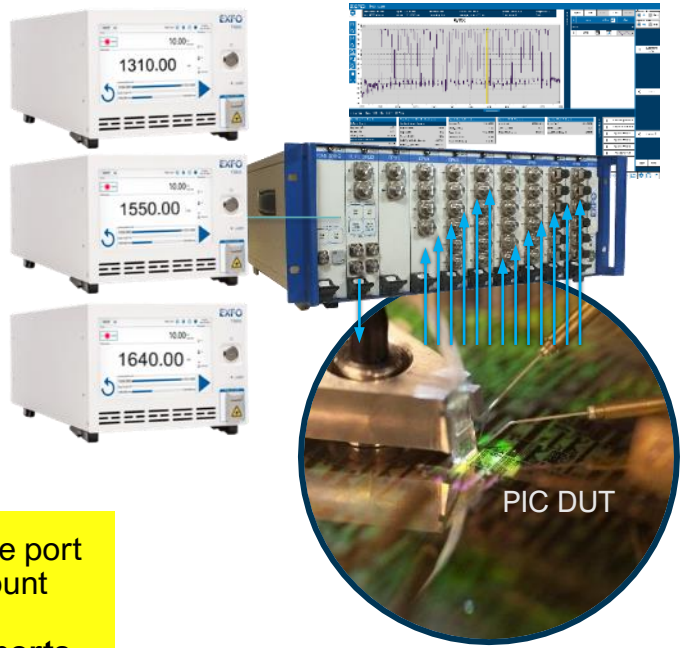
- Wavelength range C+L bands
- High resolution, needing <0.1pm
- Large power dynamic range >60dB
- Power contrast tracking 10dB/pm
- Speed and repeatability

- Femtometer resolution 20fm
- >70dB dynamic range in a single scan
- 200 nm/s scan speed
- Slope tracking 10dB/pm, 100nm/s
- Support >6,000,000 Q-factor (future proof)

CIOE Demo
Booth 10B53

高性能器件测试平台 （CTP）





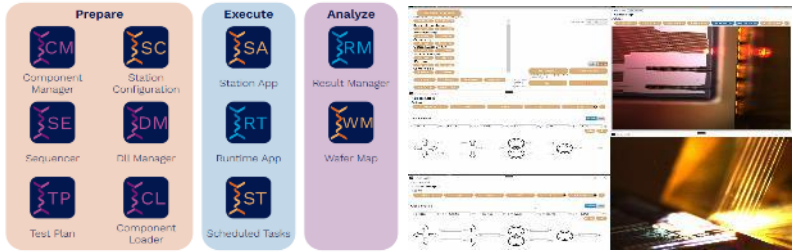
Full-band	Femtometer resolution	Dynamic range	Scan speed	Large port count
1240 nm ~ 1680 nm	**20 fm**	**>70dB**	**200 nm/s**	**96 ports**

Combine all advanced testing capabilities within a single platform.

生产与批量测试

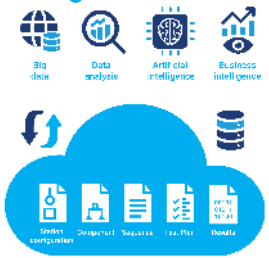
Wafer CAD files
Chip parameters
Test plans

Single software platform



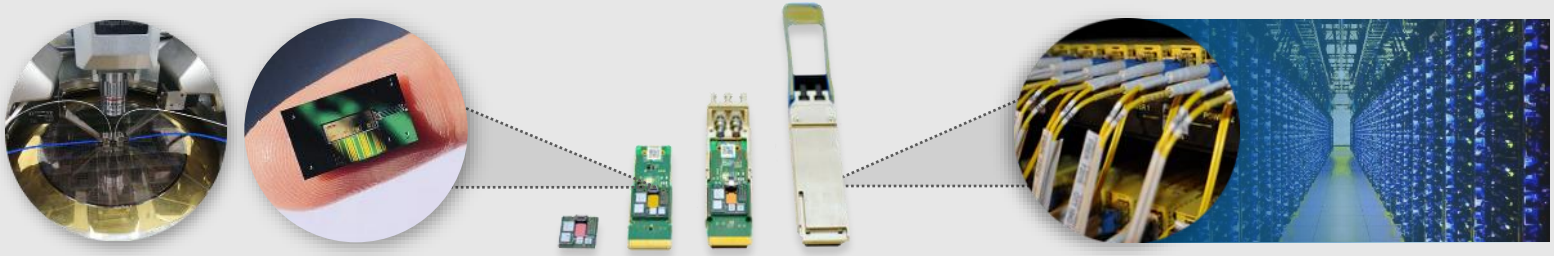
- PIC focused SW, multi-user single database
- Smart test plans, python script manager
- Automated from CAD file to analysis
- Flexible and scalable, EXFO or third-party
- Big data, AI / ML to reduce tests

Integration **Control** **Automation**



更进一步 – PIC光收发器测试生态系统

Supports **one PIC transceiver ecosystem**, from **Lab to Fab, Fab to Live**



PIC testing

Optics and Module testing

Traffic and System testing

CIOE Demo
Booth 10B53

结论

01 AI is driving PIC from prototypes to production and the industry needs efficient testing to characterize and validate large batches of wafers.

02 Wafer-level edge-coupling and high-performance testing are critical to efficiently identify KGD and ensure quality starting from the wafer level.

03 A single software interface provides an automated flow from CAD files to analysis and offers scalability and flexibility to integrate different probes and instruments to support more complex and volume PIC testing.

04 AI and machine learning can be used to predict and skip bad circuits to optimize test time and save costs.

EXFO solutions support **the entire lifecycle** of new technology development and introduction **from lab-to-live.**

谢谢！