

*PDK Framework:  
Combining Multiple Foundry  
Platforms in One Design*

*EPIC Online Technology Meeting on  
Photonics Hybrid Integrated Circuits*

Andrzej Połatyński

16 September 2024

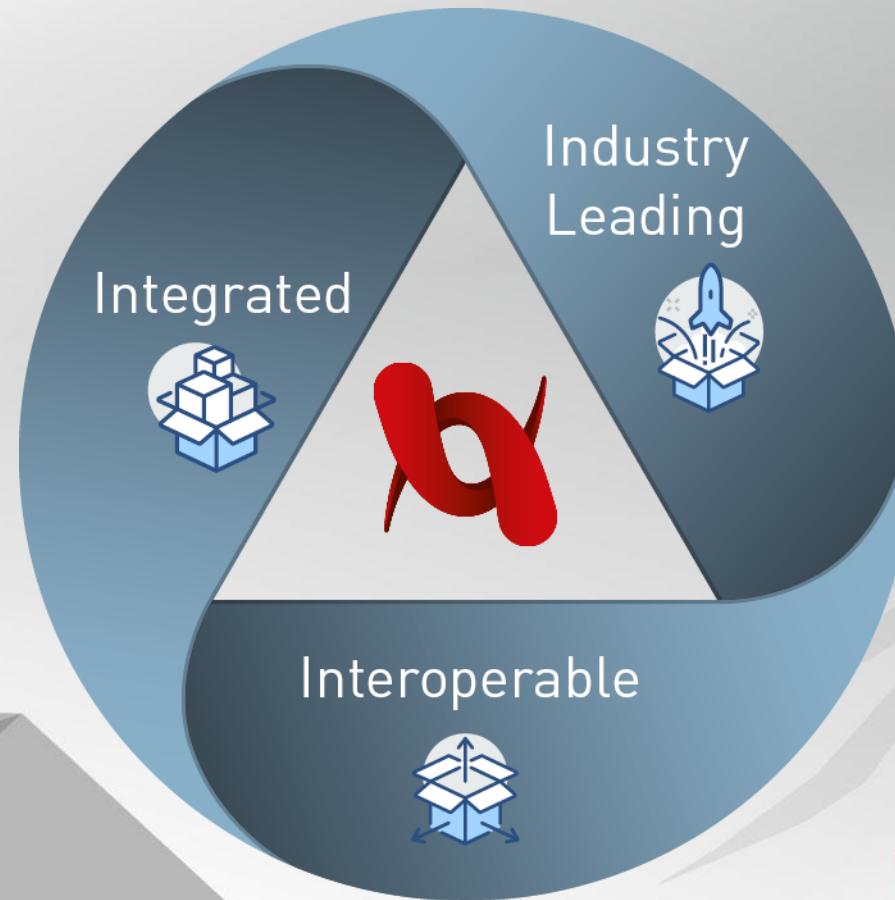


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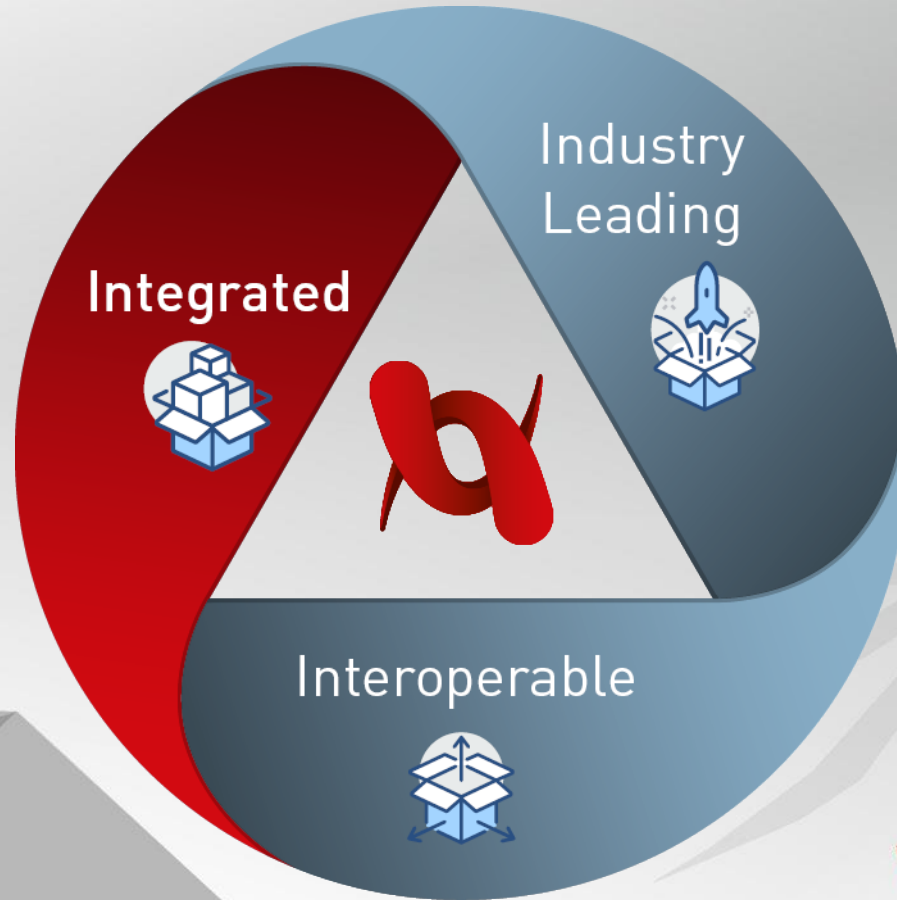
- ➔ Market leader with 25+ years of experience
- ➔ Regional offices in Europe and North America
- ➔ Global network of resellers and representatives

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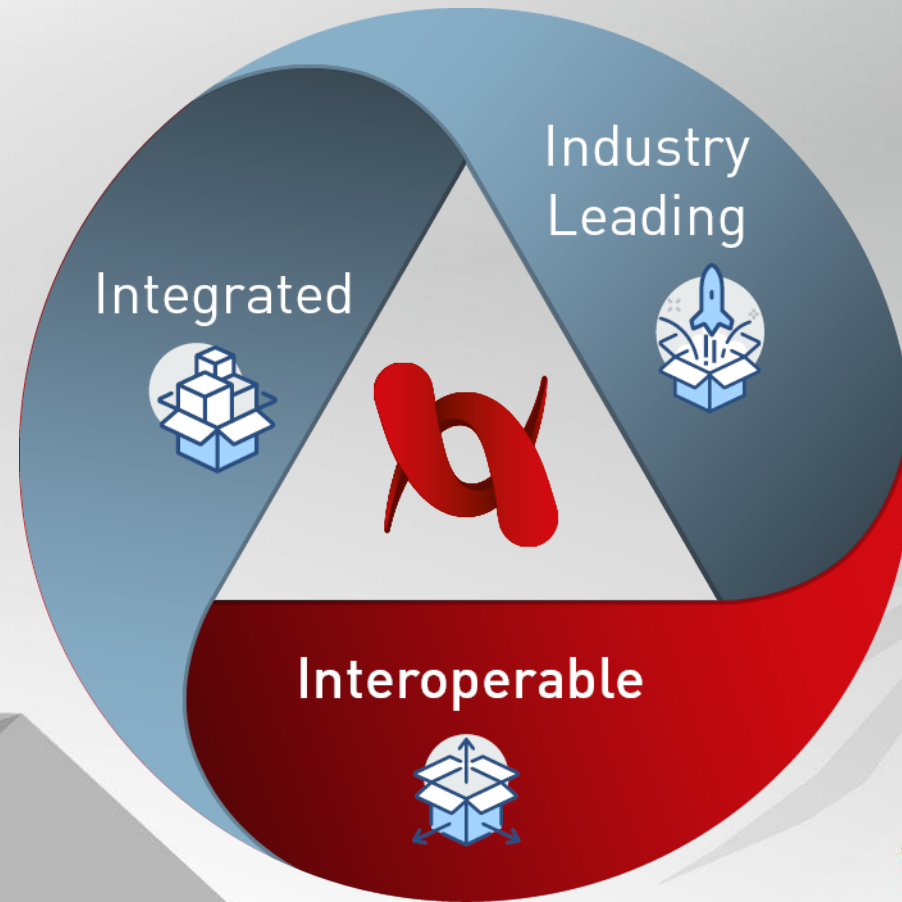
- ➔ We **integrate** efficient simulation techniques and professional design functions for devices, components and systems.

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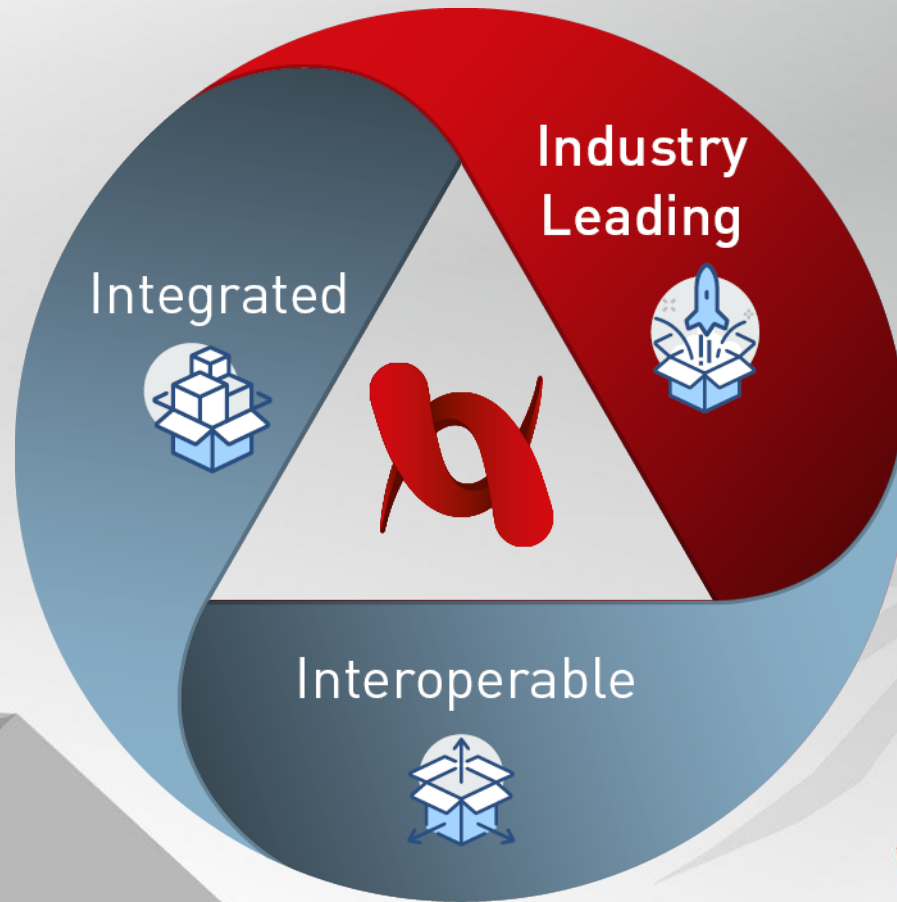
- ➔ We enable **interoperability** with 3rd party simulation, design and programming software, and test & measurement equipment.

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## SOFTWARE AND SERVICES

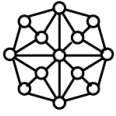
for Photonic Design & Analysis

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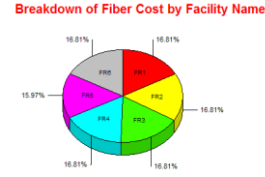
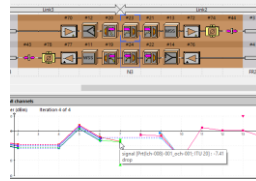
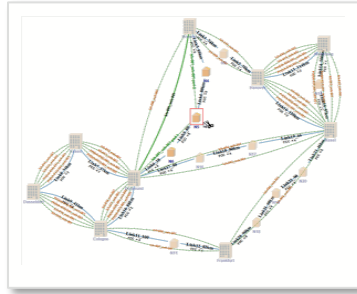



- ➔ We seek **industry leading** solutions to chart new frontiers via forward-looking industrial and research collaborations.

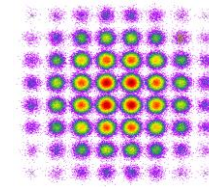
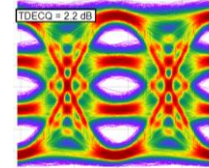
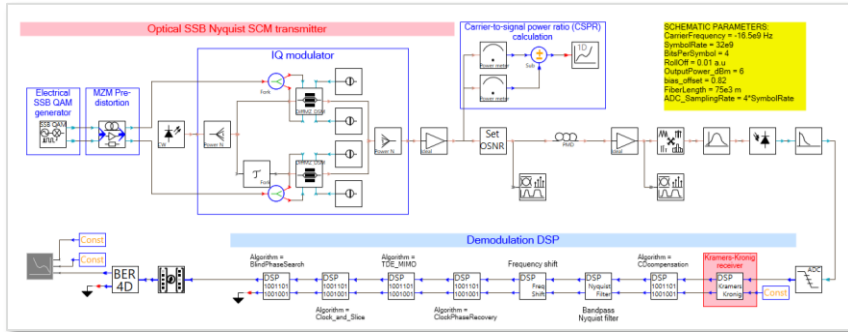
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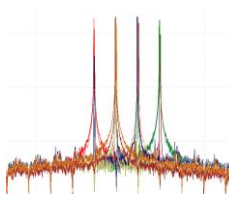
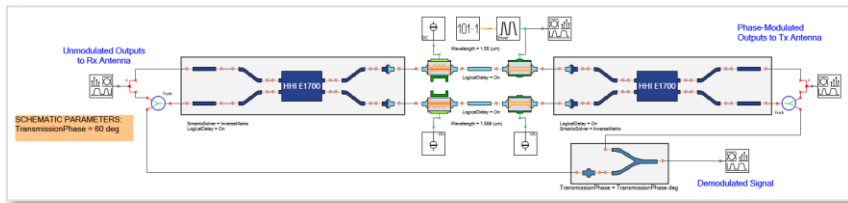
**Link Engineering**

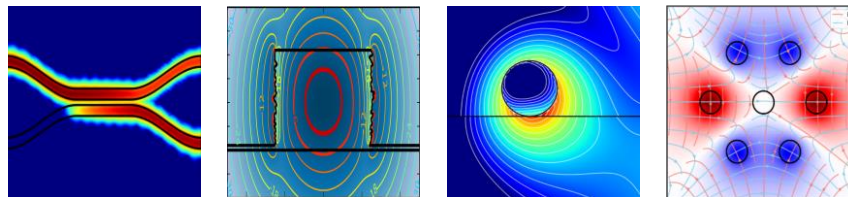
**Transmission Design**



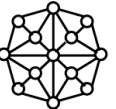

**Component Design**






**Device Simulation**



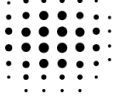
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## Link Engineering

VPI Link Designer    VPI Link Configurator




## Transmission Design









VPI Transmission Maker    VPI Lab Expert    DSP Library    QKD

Optical Systems




## Component Design




VPI Component Maker Fiber Optics    VPI Component Maker Photonic Circuits

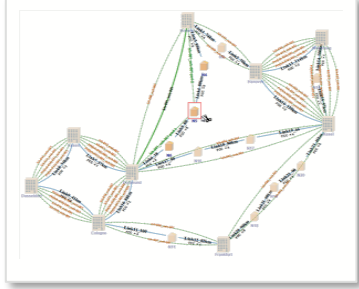
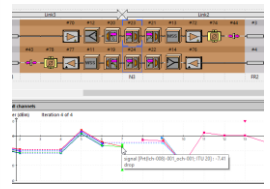
PDK<fab>



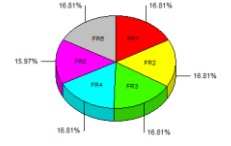
## Device Simulation

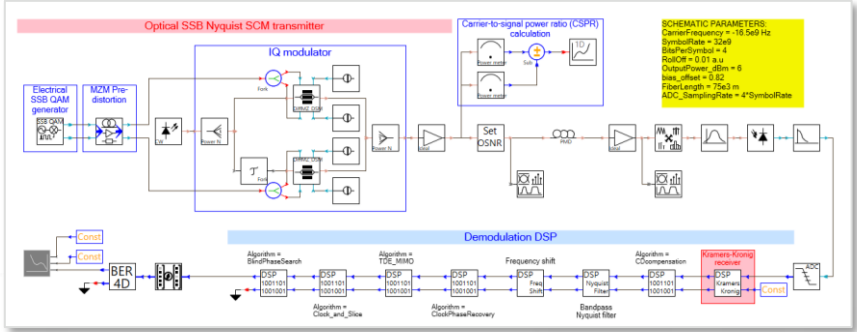


VPI Device Designer

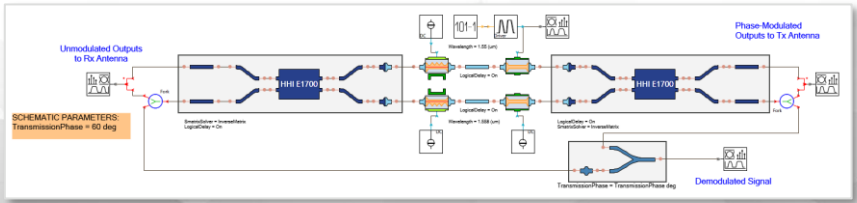



### Breakdown of Fiber Cost by Facility Names

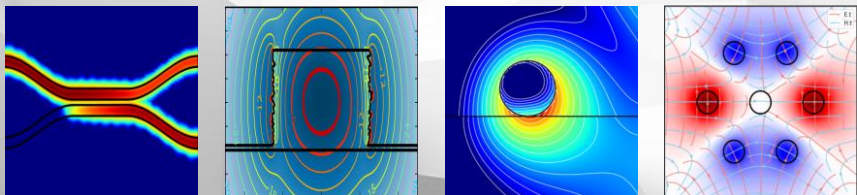




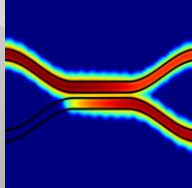
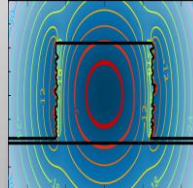
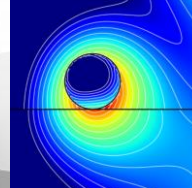
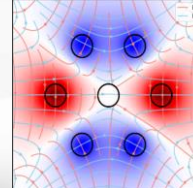
Schematic parameters: Carrier Frequency = 10.569 Hz, Symbol Rate = 2500, Bits Per Symbol = 4, Roll Off = 0.01, Output Power = 0 dBm, Bias Offset = 0.02, Fiber Length = 7562 m, ADC Sampling Rate = 4 \* Symbol Rate.

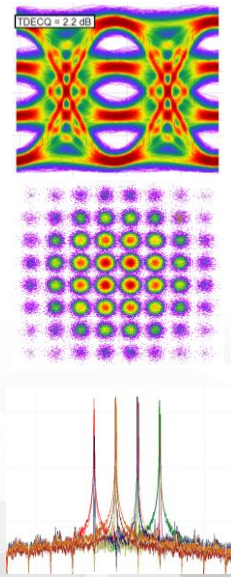


Schematic parameters: Transmission Phase = 90 deg.

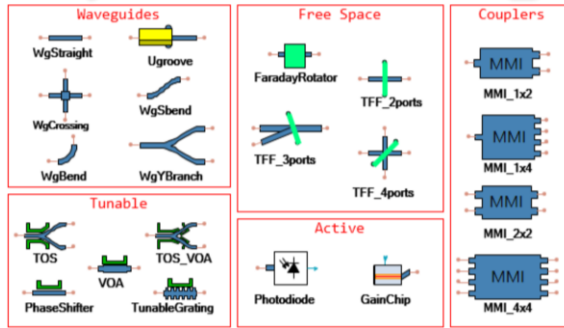
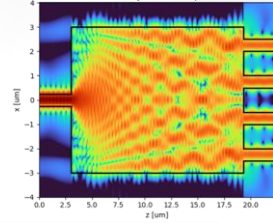


Schematic parameters: Transmission Phase = 90 deg.

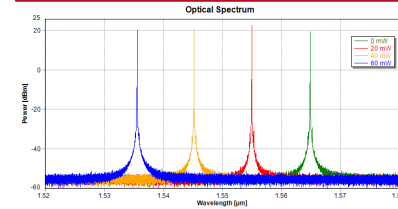
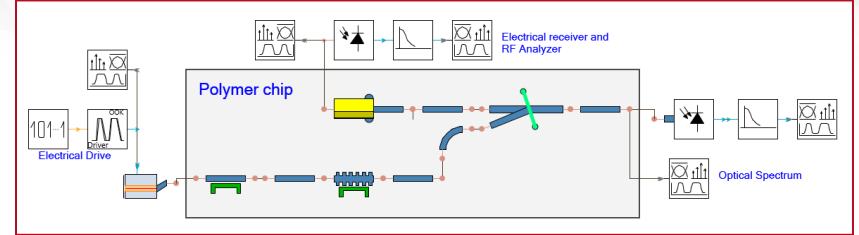







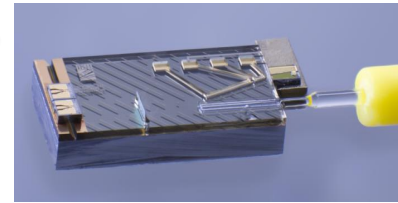
```
#SMATRIX MMI1x4
T(port1->port1) = 0.0003107964689502117;
T(port1->port2) = 0.21883528398098038;
T(port1->port3) = 0.2424987845519379;
T(port1->port4) = 0.24249878456378737;
T(port1->port5) = 0.21883528398970601;
T(port2->port1) = 0.21821821167389227;
T(port2->port2) = 0.0009396225655342919;
...
```



## VPI circuit simulation view



## Assembled Transceiver



Parameters, Tolerances



BB Library, Processes



Simulation Models



Standardized xPDK file format

```
<bb name="mySOA">
<bbtype>soa</bbtype>
</bb>

<bb name="myParam">
<parameter name="MinL" type="int" min="1">5</parameter>
<parameter name="MaxL" max="100"> 5.0 </parameter>
<parameter name="Rangel" min="1" max="100"> 5.0 </parameter>
<parameter name="IntSet" type="int" allowedValues="1 2 5 6 10">5</parameter>
<parameter name="StringSet" type="string" allowedValues="a1 b2 c5 6 10">c5</parameter>
<parameter name="noexpr" type="double" min="1"/>
</bb>
```

[http://www.pdaflow.org/xpdk/docu/xPDK\\_BB.php](http://www.pdaflow.org/xpdk/docu/xPDK_BB.php)

Layout Extraction

Layout Design

Electronic/Photonic Co-Simulation





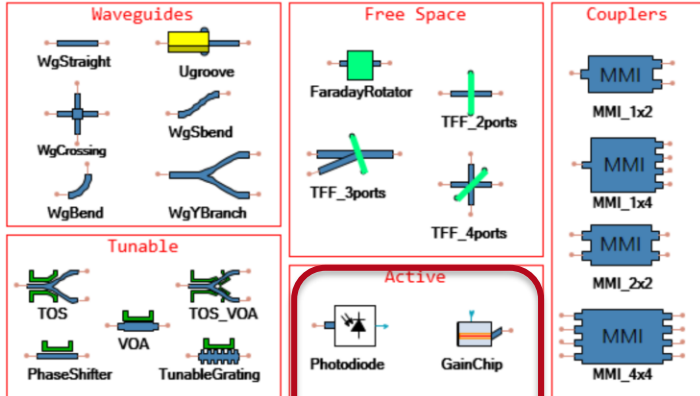
# Various PDK approaches for hybrid PIC design using PDKs

*Based on existing foundry PDK implementations*

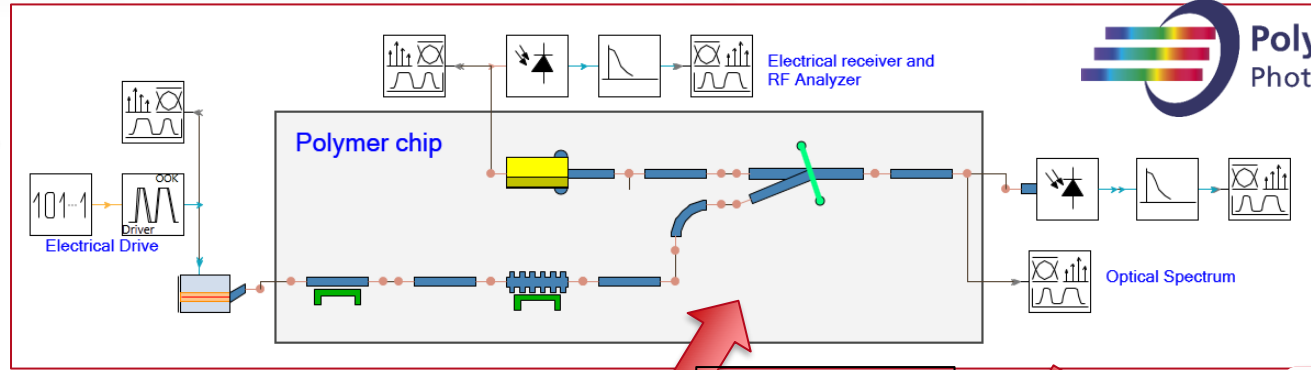
# From PDK library to Assembled Chip

## Polymer-based Hybrid Tunable Laser

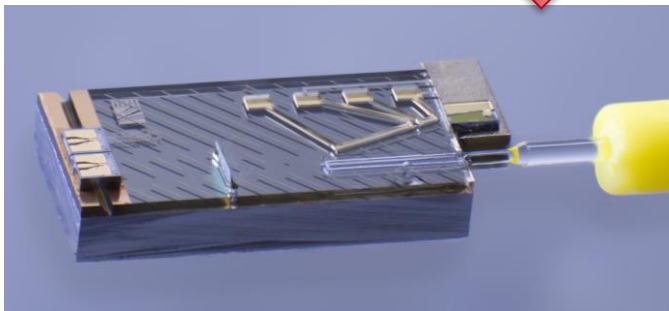
### List of HHI Polymer-based Building Blocks



### VPI circuit simulation view



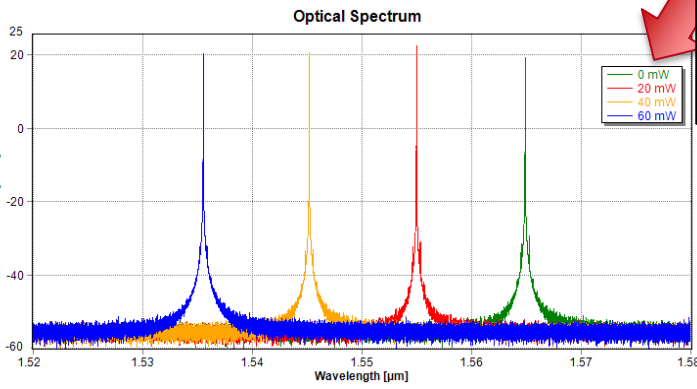
### Assembled Transceiver



Fabrication processes and assembly

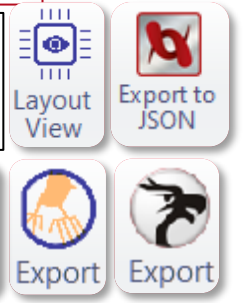


???

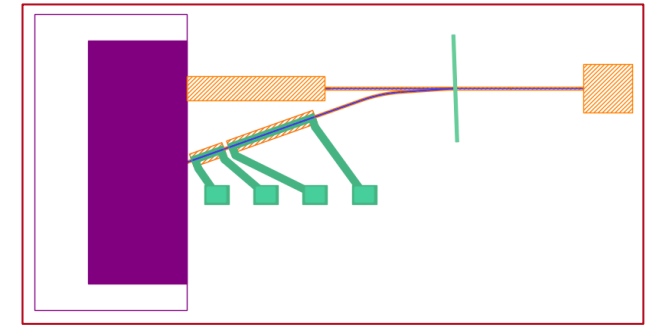


Optimization and Tolerance Simulation

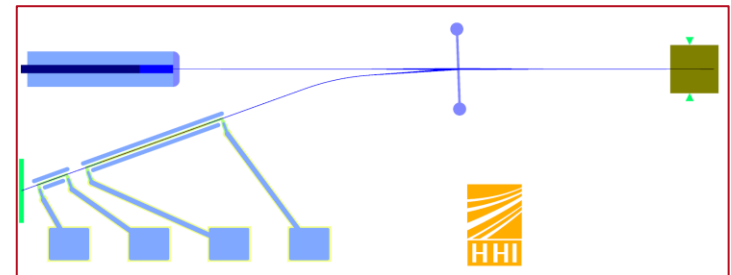
Export netlist or layout file



### VPI layout view



### Exported GDS (in Klayout)



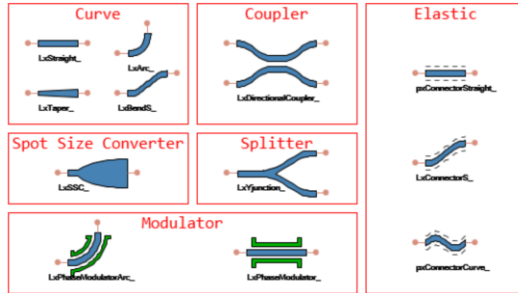
GDS extraction using given layout tool



Needs the laser integration

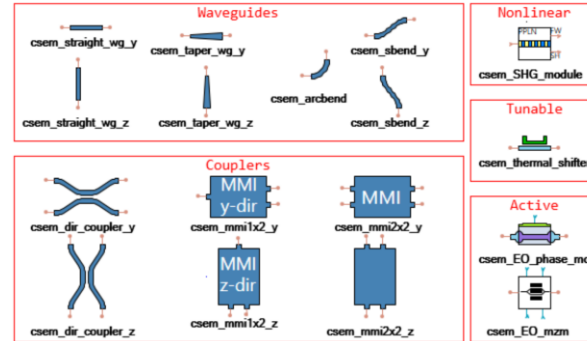


SiN LioniX PDK



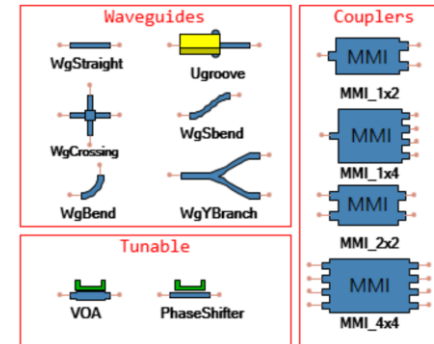
## ELENA<sup>IX</sup>

List of PDK CSEM LNOI Building Blocks

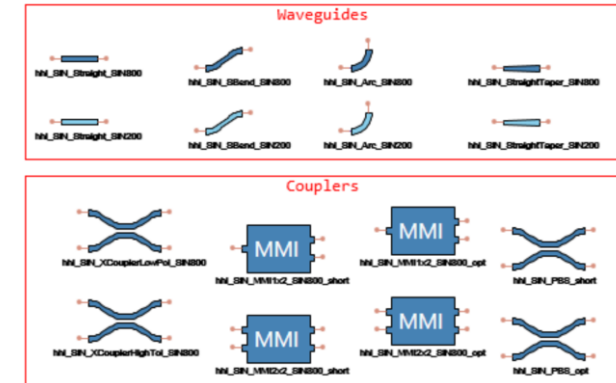


PolyChrome Berlin  
Photonics for Sensing

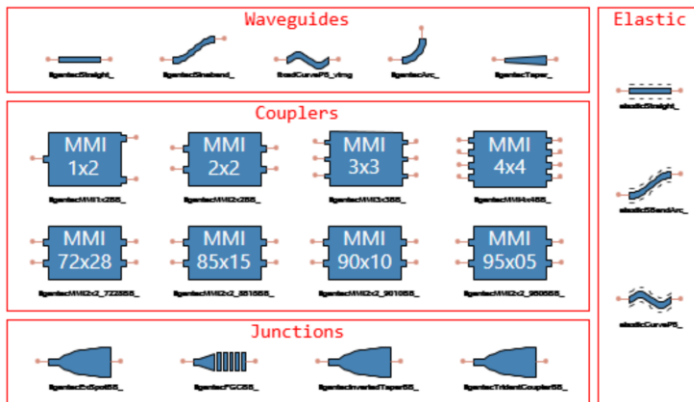
HHI Polyboard VIS PDK



HHI SiN VIS PDK



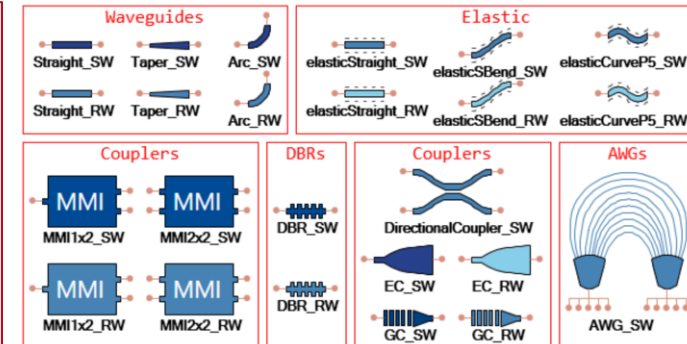
SiN LIGENDEC Building Blocks



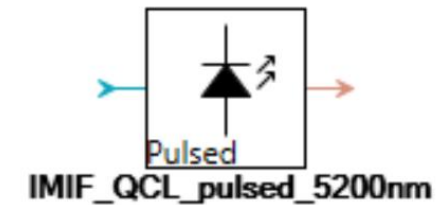
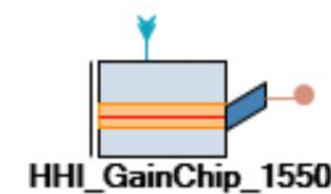
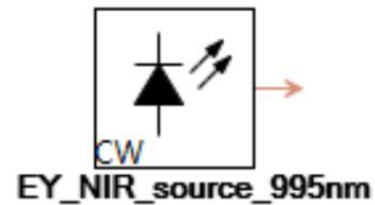
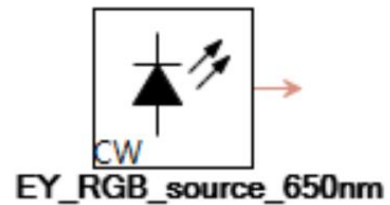
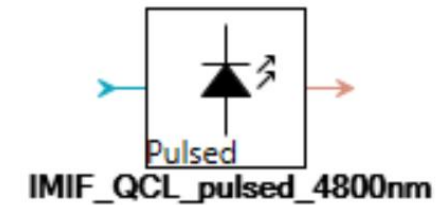
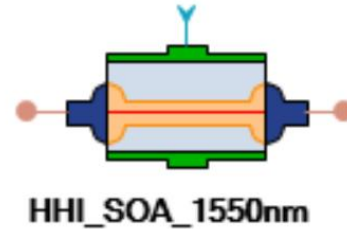
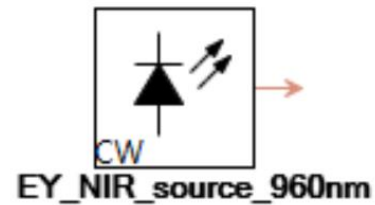
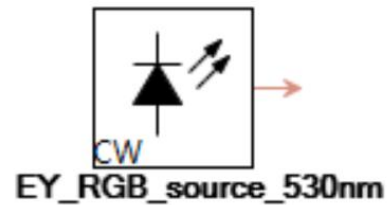
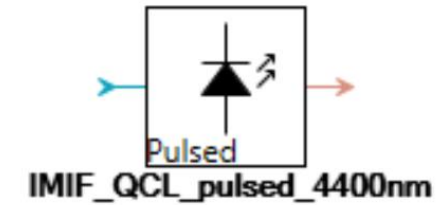
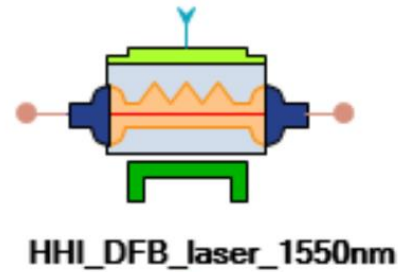
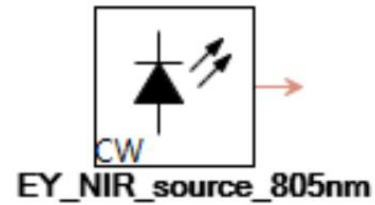
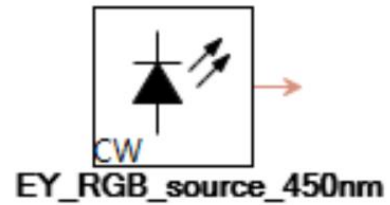
### Hybrid integration vs design:

- BBs offered by chosen foundry
  - InP lasers @1550 and @1310 nm
- External light sources
  - Pluggable and bare chip lasers @visible
  - QCLs for mid infrared platforms

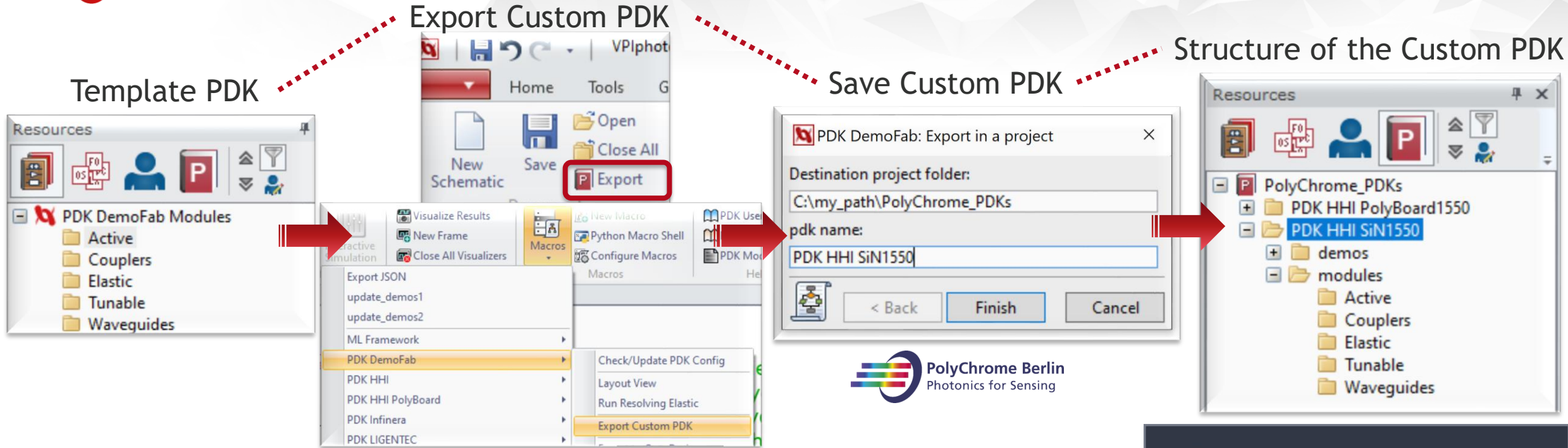
MIRPIC Ge-on-Si PDK



# External foundry-dedicated lasers



**Challenge:** Laser interface optimized for a given platform.  
Other platform choice → new interface modules required.



## Custom PDK contains:

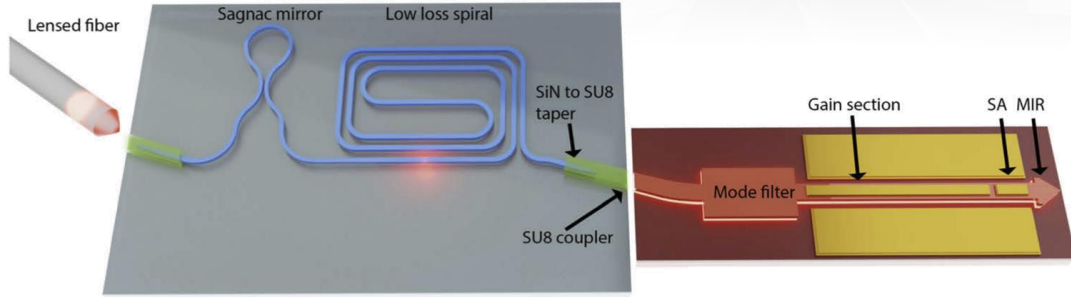
- ✓ Module templates and basic demos
- ✓ Exemplary layout templates
- ✓ Generic PDK toolbars and macros
  - Layout/GDS export
  - Elastic connectors
  - Arbitrary and relative port locations

## Main advantages:

- ✓ IP protection
- ✓ Flexible development process
- ✓ Easy to share



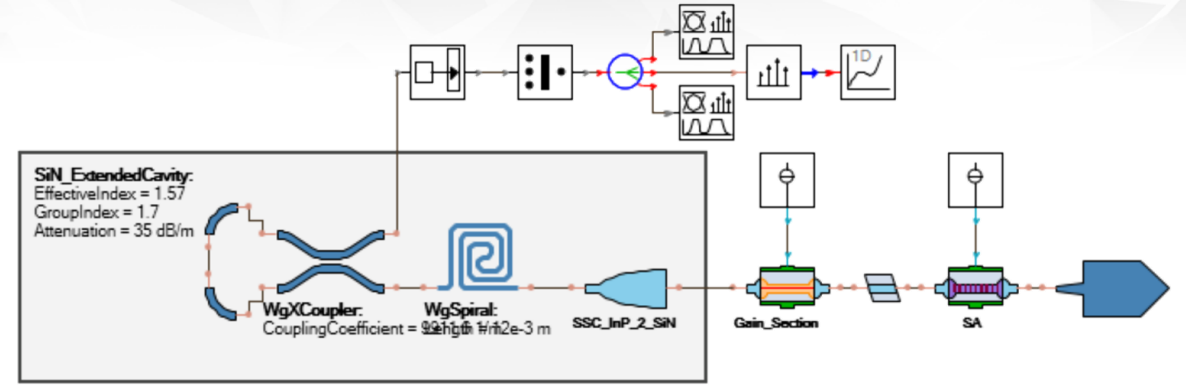
# Hybrid integrated mode-locked laser



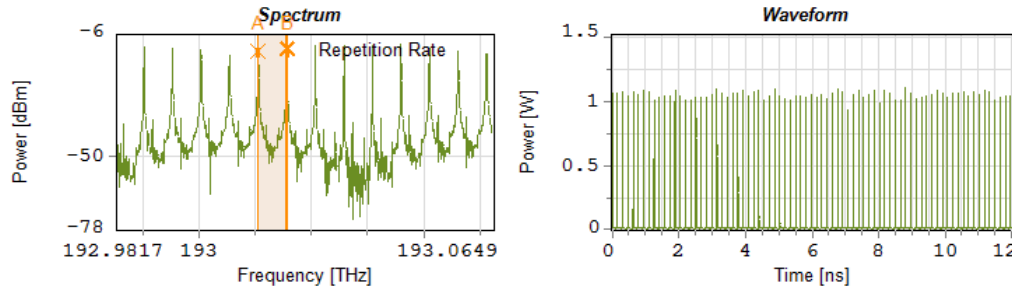
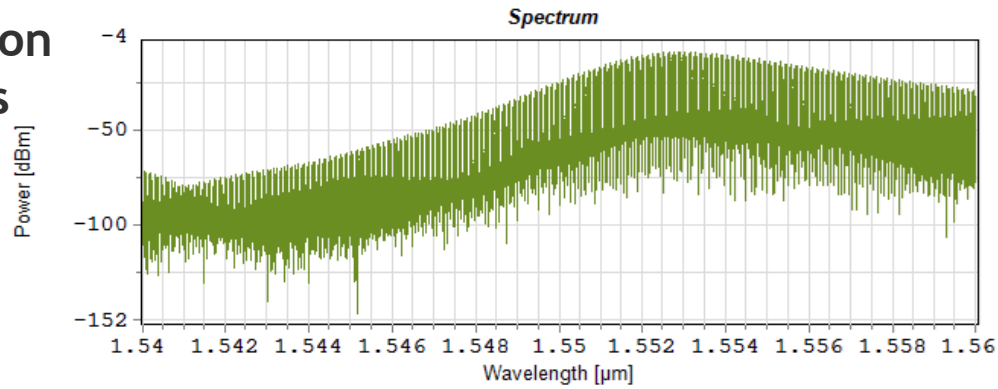
SiN extended cavity

III/V RSOA

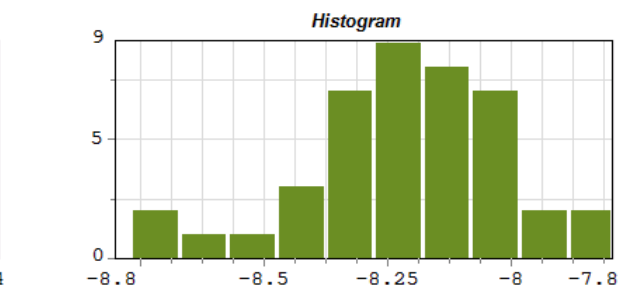
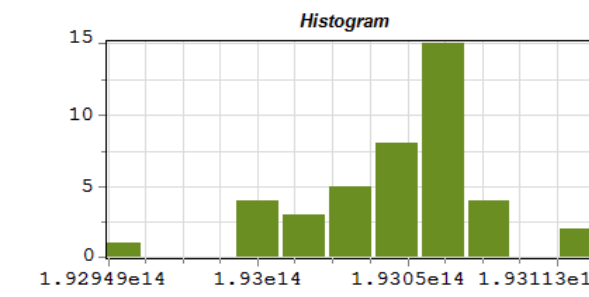
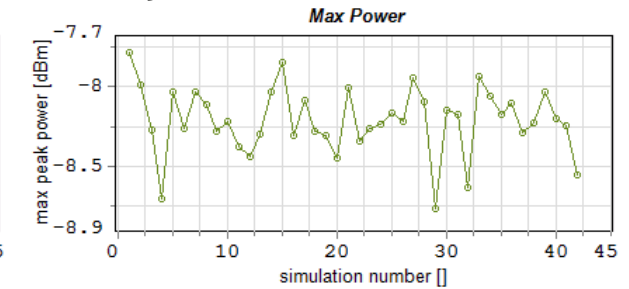
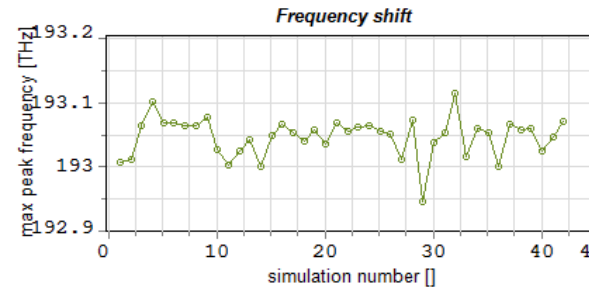
References:  
 [1] E.Visser et al., "Hybrid integrated mode-locked laser diodes with a silicon nitride extended cavity", Optics Express, vol. 29, no. 10, pp. 15013-15022, April 29, 2021.



## Simulation results



## Tolerance Analysis



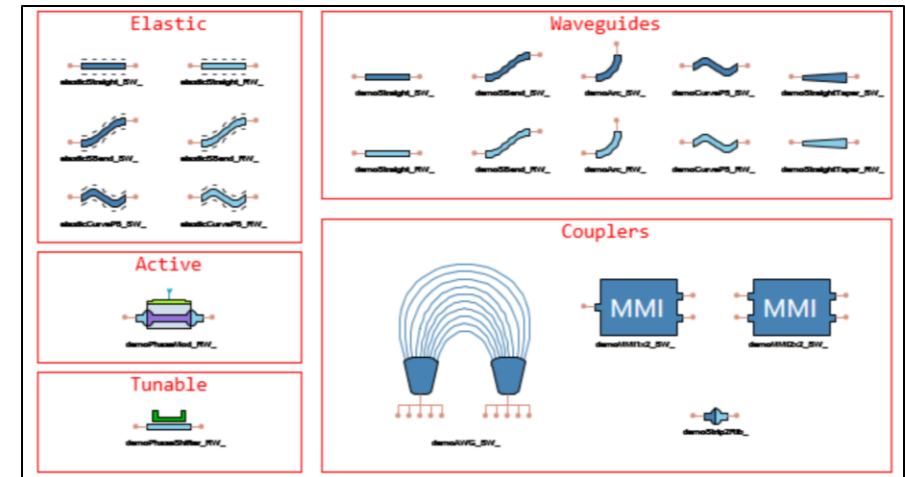
## What can you do for us?

- ✓ Develop PDKs with us!
- ✓ Provide feedback on your design needs!

## How can we help you?

- ✓ Enable various strategies to design hybrid PICs
- ✓ Use bidirectional design workflow:
  - Devices ⇔ Circuits ⇔ Systems
- ✓ Custom PDK integration framework
  - ⇒ Easy to build, use, and share PDKs
- ✓ Design acceleration via automated export of the layout
- ✓ Personalized support with your custom PDK development

## Build your PDK with us!



## Contact us to learn more about:

- *Simulation and Optimization of PICs*
- *Design workflow from Devices to Systems*
- *Support of fabrication tolerances*
- *Schematic-driven layout-aware design methodology*
- *Electronic/Photonic Co-Simulation*
- *Design of custom PDKs*

## Contact Us!

*Presenter: Andrzej Połatyński*  
*andrzej.polatynski@vpiphotonics.com*

*Product enquiries: Sales@VPIphotonics.com*  
*Technical support: Support@VPIphotonics.com*

**VPIphotonics.com**

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