Yield and manufacturing challenges for microLED micro-displays

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TECHNICAL PROBLEM STATEMENT

AR display

Resolution

<3um sub-pixel pitch

Fail:
LCOS
DLP

Brightness

> 1Mnit @ D65 white point

Fail:
microOLED
LCOS

Power consumption

<1W @ usage scenario

Fail:
DLP

Image quality

- 16bit/color
- De Mura / Gamma
- Lifetime degradation

Fail:
Laser scanning

Cost-effective volume manufacturing

BOM like mobile phone display

Specs for AR and automotive HUD are similar.

INTEGRATION

CMOS + MICROLED

µLED on CMOS

Pixel pitch >8µm

Pixel pitch <8µm

Die-to-wafer transfer

Full-wafer 'monolithic integration'

Individual die per pixel

One die per display

D2W Bumping (e.g., In, Sn)

D2W hybrid bonding

W2W hybrid bonding

Sequential 3D

Metal bonding

Dielectric bonding

TFT on LED wafer

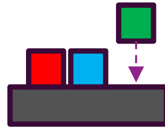
- The challenge is not in realizing the best microLED but a yielding integration flow with the CMOS driver
- The CMOS driver for microLED displays requires advanced node CMOS (<45nm) 300mm wafer
- Any process flow not on 300mm wafer will require CMOS wafer downsizing and therefore a massive yield loss → Die cost$$

INTEGRATION CHALLENGES

HOW TO MAKE RGB?

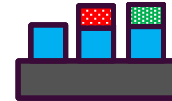
- In all routes shown below, demo's have been shown.
- There are intrinsic limitations with every approach assuming equal via-pitch.

I. Pixel die transfer



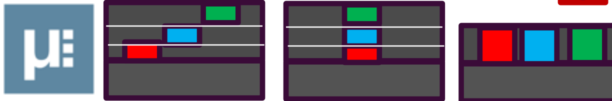
II. Dynamic pixel tuning

III. Color down conversion



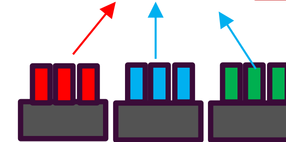
1. Quantum Dots
2. Perovskite
3. Nano-phosphor

IV. Wafer level Pixel side-by-side integration



1. Stacking Epi by growth
2. Stacking Epi by bonding
3. **Stacking LED**
4. Templated growth (e.g., Nanowire)
5. Epi-etch back and overgrowth
6. Etched nanopillars

V. Optical combiner



1. Primary waveguide combiner
2. Secondary waveguide combiner
3. Prism combiner

PERFORMANCE??

LIGHT EXTRACTION EFFICENCY

Compare: blue laser scanning has WPE (+/-20deg) ~10%

Parameter	B	G	R GaN	R AlInGap	Dependency
Resolution [ppi]	10000	10000	10000	10000	Process
IQE [%]	90	60	30	60	Planar epi-material
LEE [%] top MESA	<9%	<9%	<9%	<5%	Refractive index epi; assume random dipole emitter
LEE [%] waveguided	?	?	?	?	pitch vs. MESA size
Radiative recomb. [%]	?	?	?	?	Mesa size, passivation
Target WPE[%] all angle	?	?	?	?	
Target WPE[%] +/-20deg	**<2.5**	**<1.5**	**<1**	**<1.5**	Focusing structure. Max. 30-35% of light within APEX

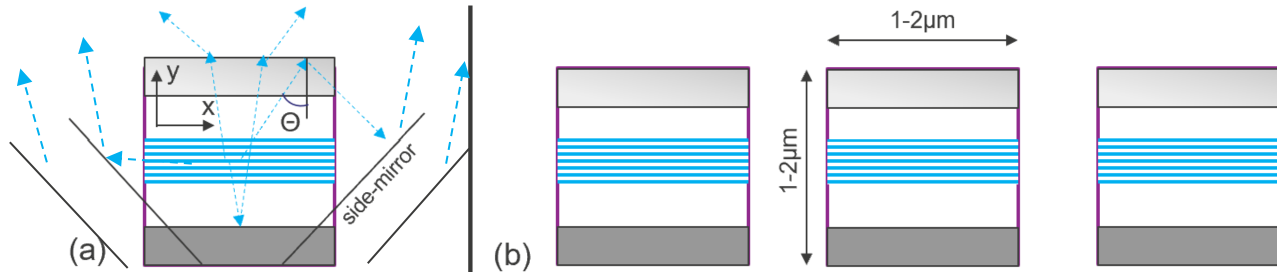
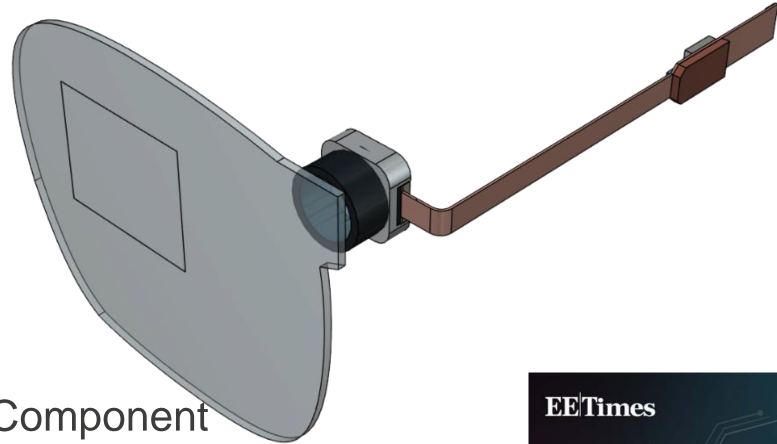


Figure 1. Light-outcoupling in a planar microLED (a) small pixel vs large pitch (b) tight pitched array

MICLEDI results

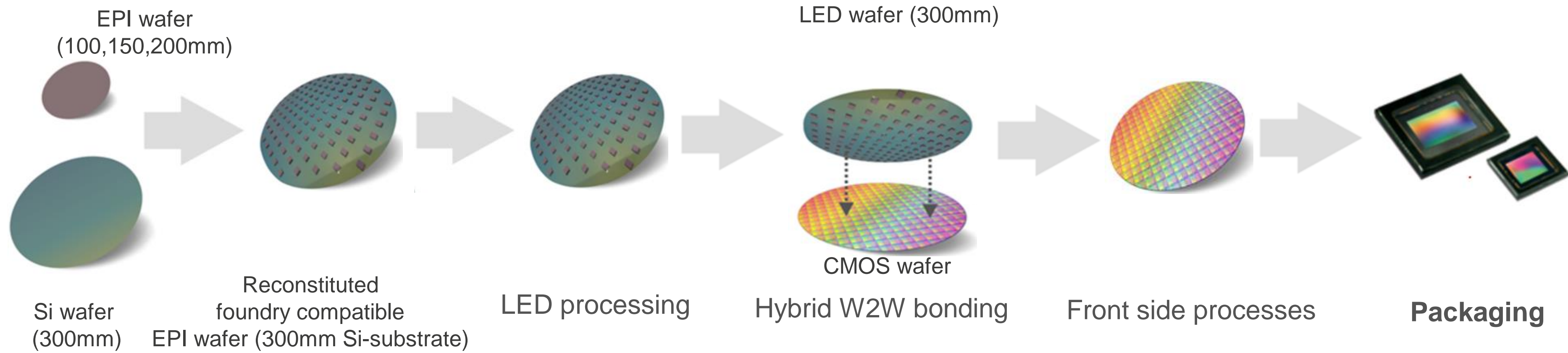
COMPANY OVERVIEW



Company:	Micledi Microdisplays
Vertical:	AR and automotive
Product:	MicroLED Displays
Business model:	B2B Fabless Hardware Component Sales
Technology IP:	Spin-out of IMEC in 2019
USP:	**Volume manufacturability in 300mm foundry**
Financials:	30MEUR raised

LED PROCESS FLOW FOR W2W BONDING

MICLEDI HIGH LEVEL OVERVIEW

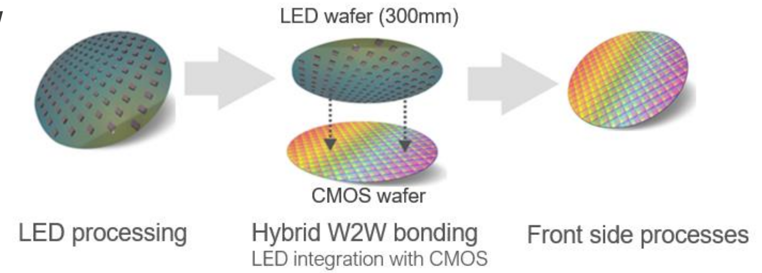


= eWLP packaging		= 3D BSI imager			
Issues solved by MICLEDI	• Defectivity • No 300mm epi • Residual stress	• CMOS compatible LED process flow	• CMOS/LED tight pitch integration	• LED performance • Beam shaping • Cross-talk suppression	• Driving • Calibration

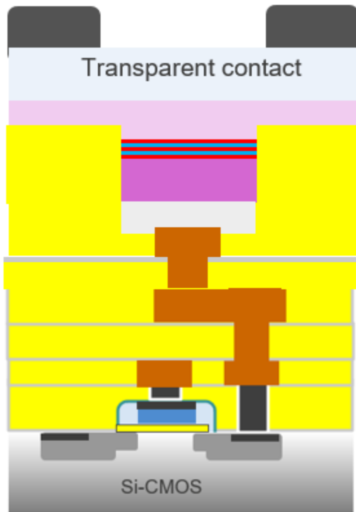
Generic solution to integrate tight pitched (<3um) compound semiconductor with advanced Si-CMOS node

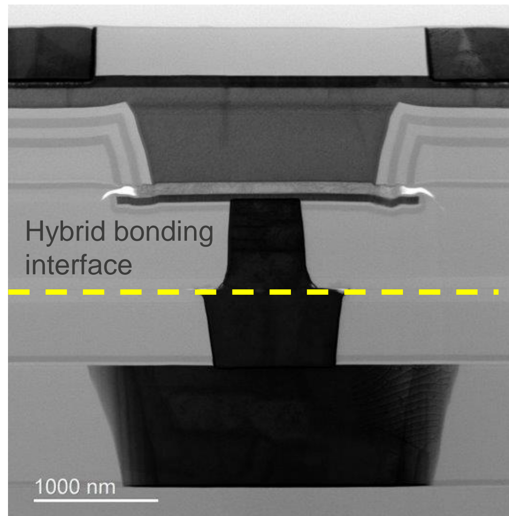
DISPLAY INTEGRATION

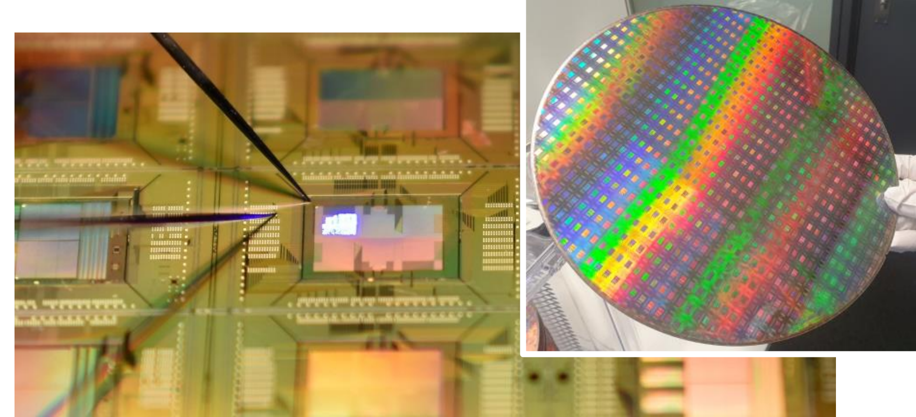
300MM CMOS FAB COMPATIBLE PROCESS FLOW



The challenge is not in realizing the best microLED but a yielding integration flow with the CMOS driver







W2W hybrid bonding of CMOS with GaN LED on 300mm production tools

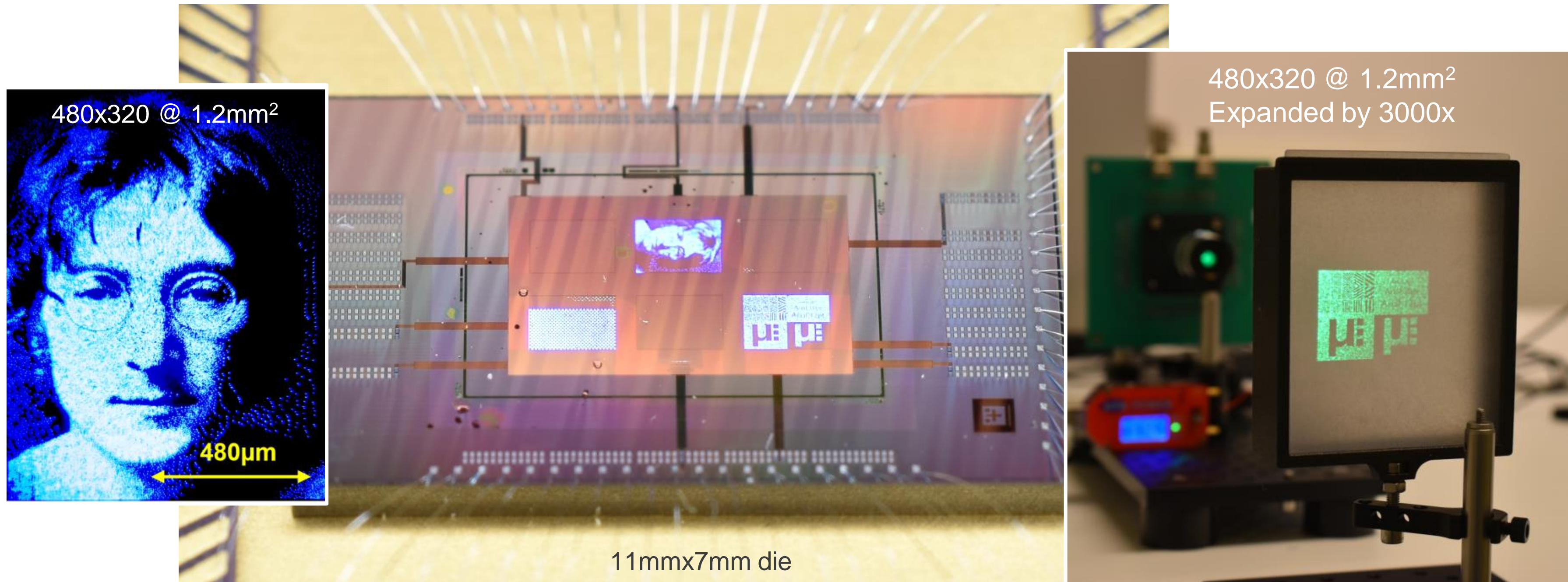
- Pixel pitch 3µm hexagon = 9150ppi
- overlay variation < 200nm across 300mm wafer

Steudel et al, SID 2022

DISPLAY TEST STRUCTURES

480x320 passive matrix sub-arrays with 3um hexagon pitch

- 1.8Mnits@525nm and 600knits@450nm at 4.5V
- WPE > 1.1% @450nm within +/-20deg
- fill factor (up to 63%)

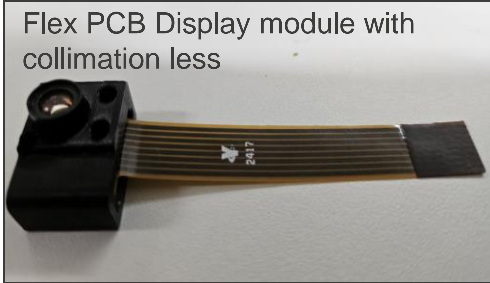


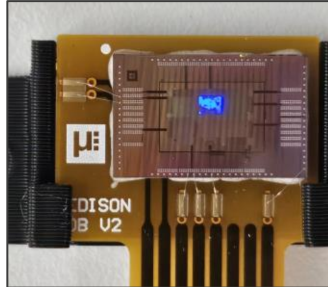
*Dithering image of John Lennon

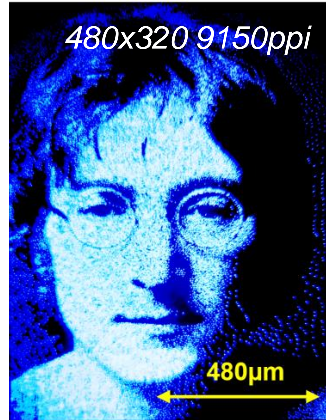
DEMO WAVEGUIDE INTEGRATION

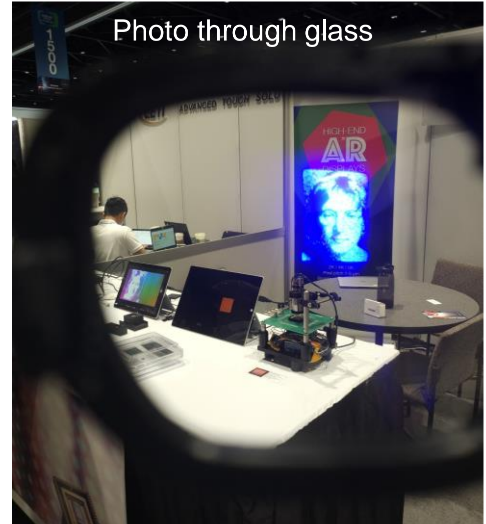
WAVEGUIDE: FOV=30˚

Very bright and sharp even against the light







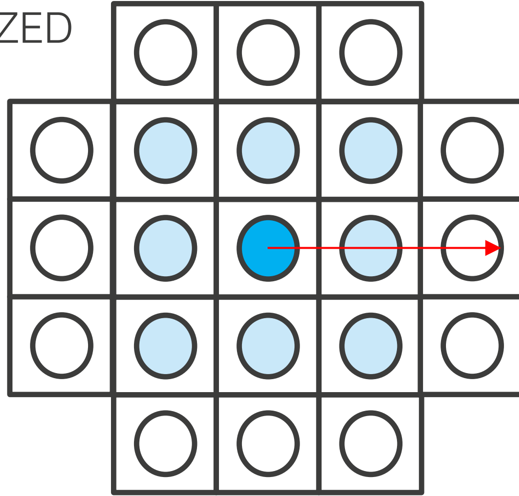


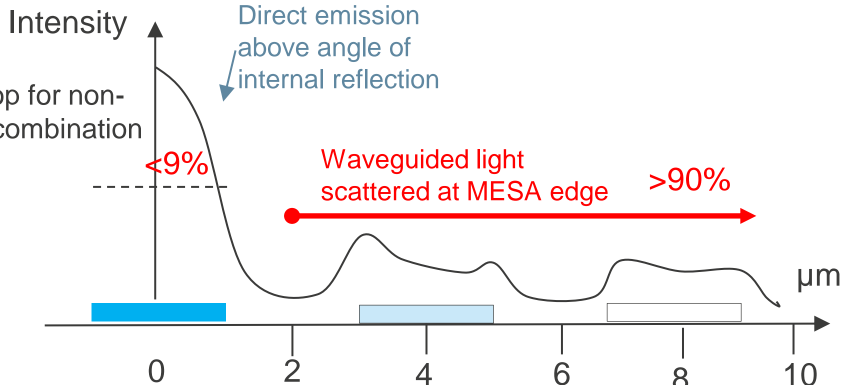
OPTICAL CROSSTALK

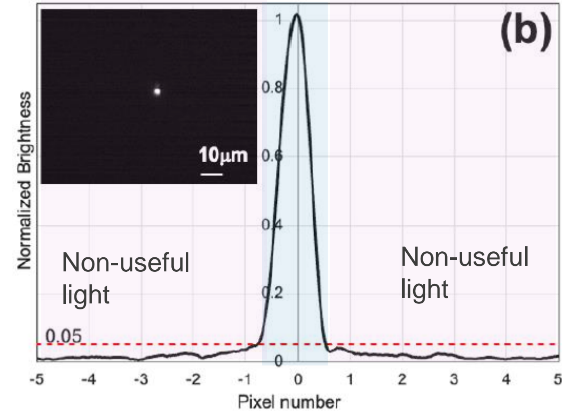
- Worst case, measured WPE can be 3-4x larger then ‘’real useful’ WPE if optical crosstalk is not eliminated.
- Crosstalk data is hardly ever shown.
- Cross-talk is less problematic in microLED for FPD but significant for microLED on CMOS

UN-OPTIMIZED

MESA = 2μm
Pitch = 4μm







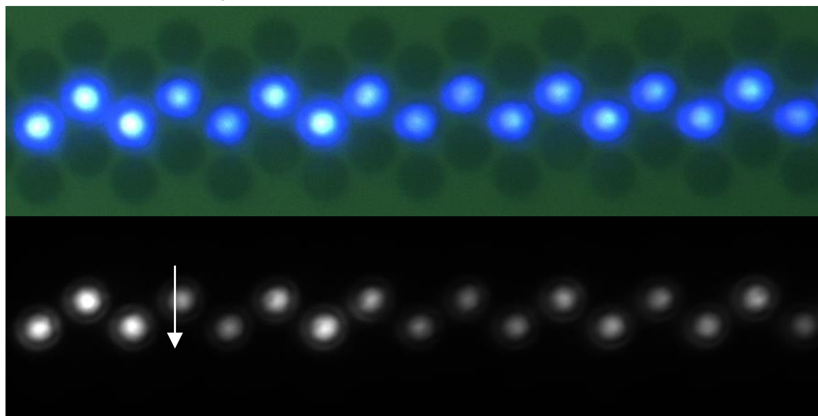
Example Literature reported data (crosstalk = -13dB) → Non-useful light integrated over 2D circle amounts to 45% of total light. Hence, reported WPE value is at least 1.8x overestimated.

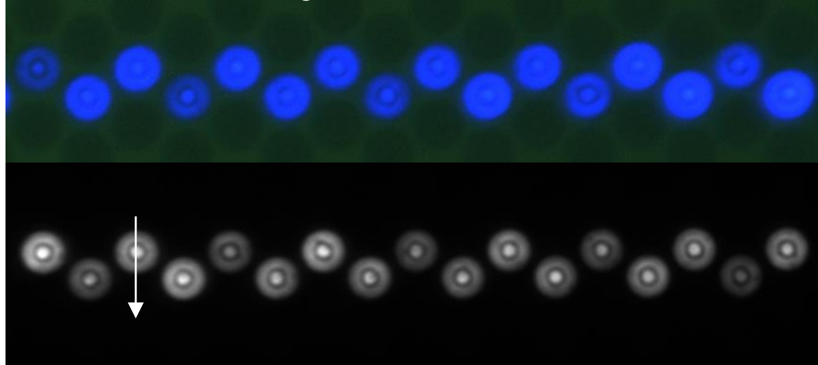
Qiming Li et al, SID 2024 Digest, pp.104-106

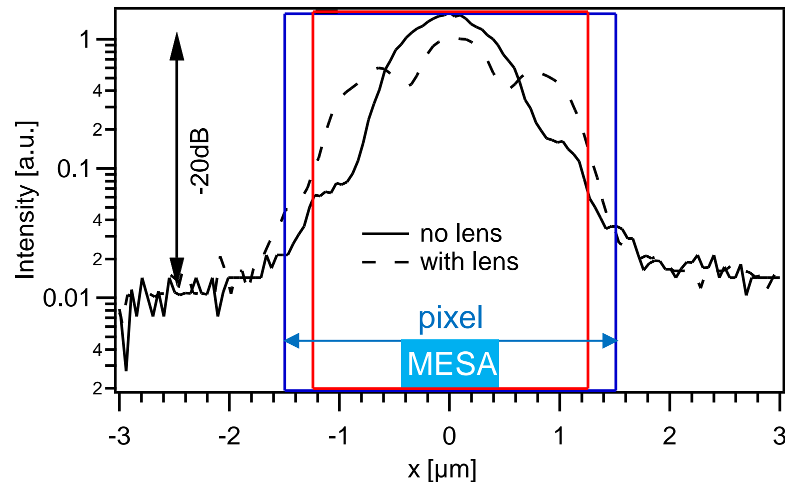
LIGHT COLLIMATION /CROSSTALK

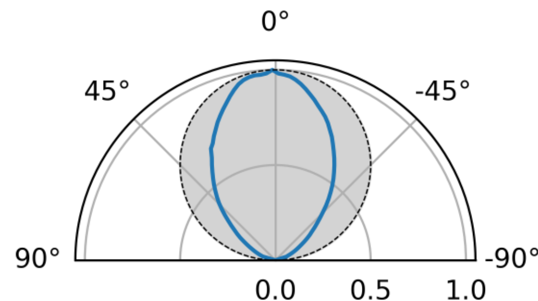
20dB cross-talk achieved

MESA: D=1µM





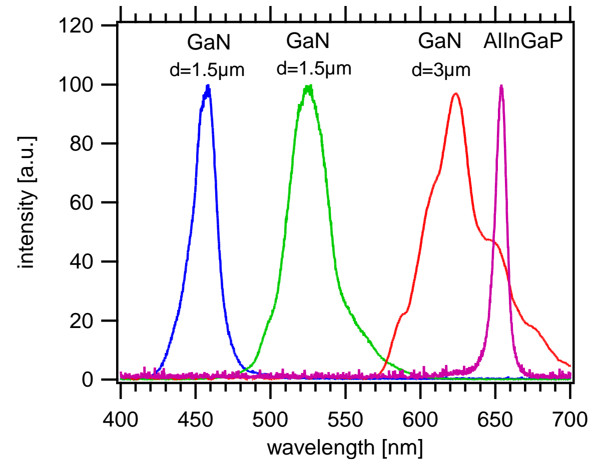




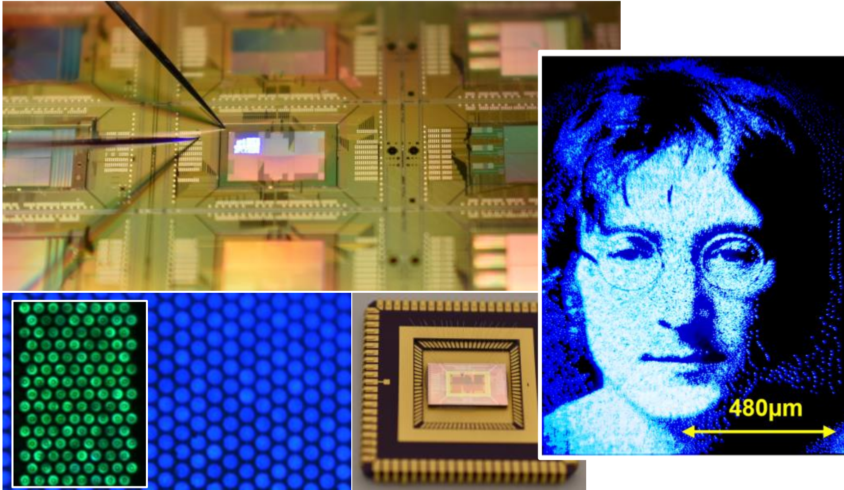
PRODUCTIZATION

FIRST PRODUCT GENERATION

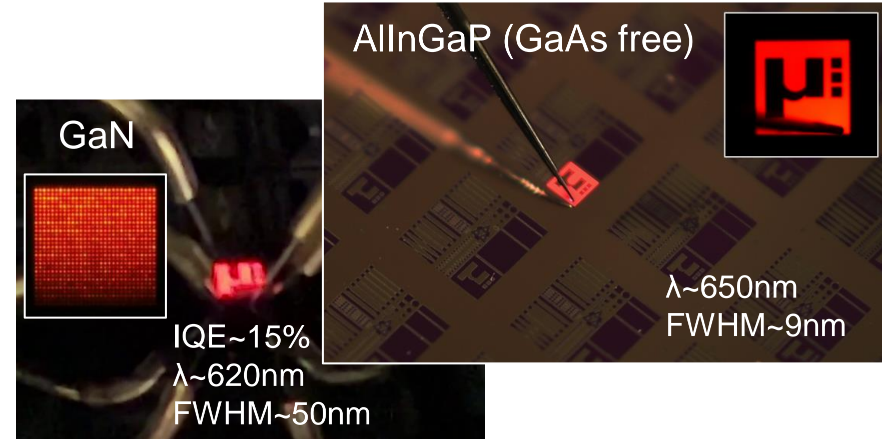
- Proven process flow for 9150ppi microLED array on 300mm full-automatic manufacturing tools
- 300mm Foundry transfer started
- ASIC design started: product prototype sampling Q4/2025



300mm full integration flow



200mm short-loop for material evaluation



SUMMARY

- The biggest challenge in microLED on CMOS is a **yielding high-volume manufacturing process**; question mark about final performance at <3um pitch
- **300mm process integration** is 2-5x cheaper than integration on 100-200mm wafer
- **Epi defectivity determines final die yield** – Solution is to Improve defectivity and implement KGD epi selection. Good enough epi-defectivity values on Si-substrate possible but questionable on sapphire or GaAs substrate
- If the **pixel pitch** gets too small (<<5um), most light below the angle of internal reflection is lost
- **Do not trust WPE numbers if you have not measured crosstalk**