TOKYO ELECTRON

Optimizing Semiconductor Equipment to Address Optical Device Manufacturing Challenges

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- Optical Device Growth
- Optical Device Process Challenges
  - AR/VR Waveguides
  - Photonics waveguides
  - Micro LED
  - Metalens
- Manufacturing Challenges
- TEL Tool Solutions

Optical Device Applications Growth

AR/VR Next human-data interface

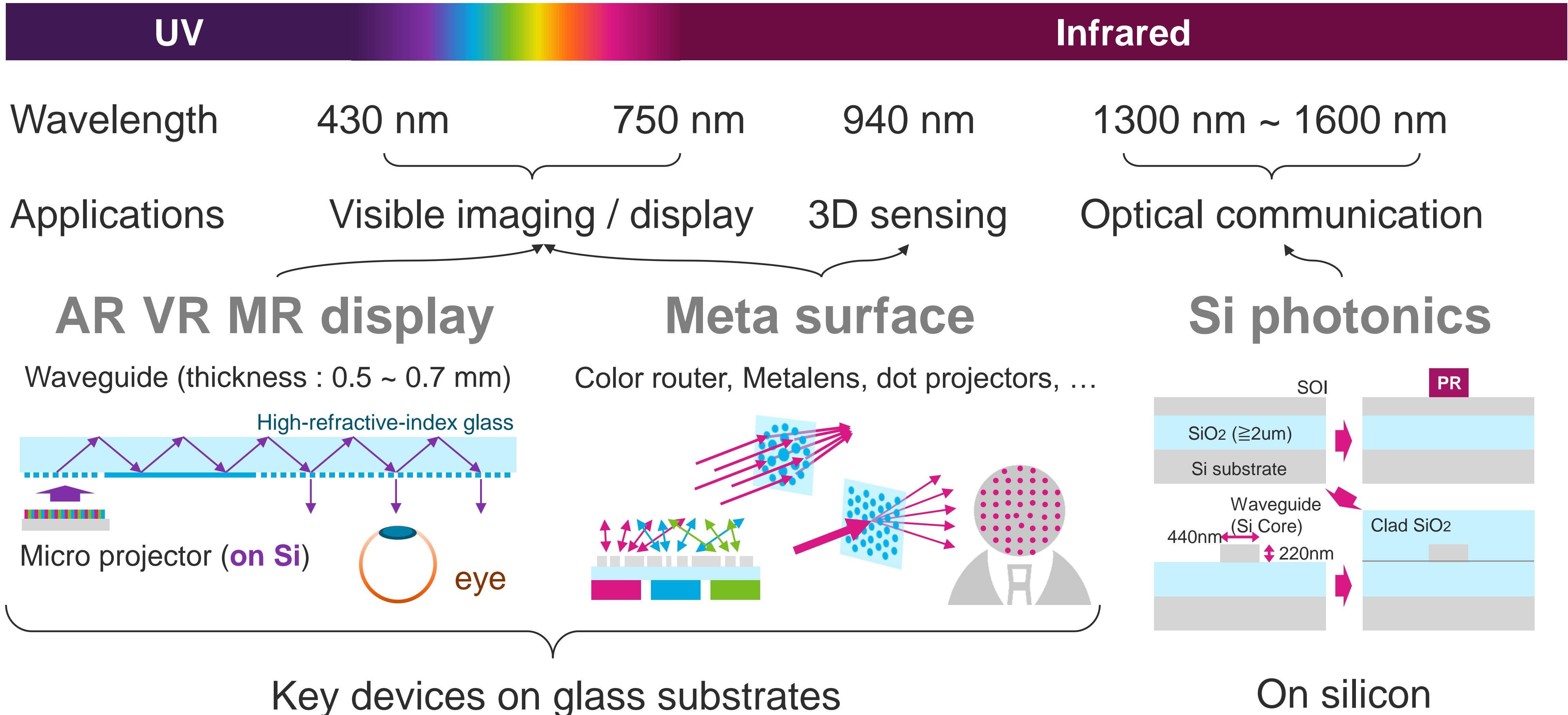
Sensors

Communications & Data Centers

Expanding applications driving growth and increasing manufacturing capacity requirements

TEL "MAGIC" to Address More-than-Moore

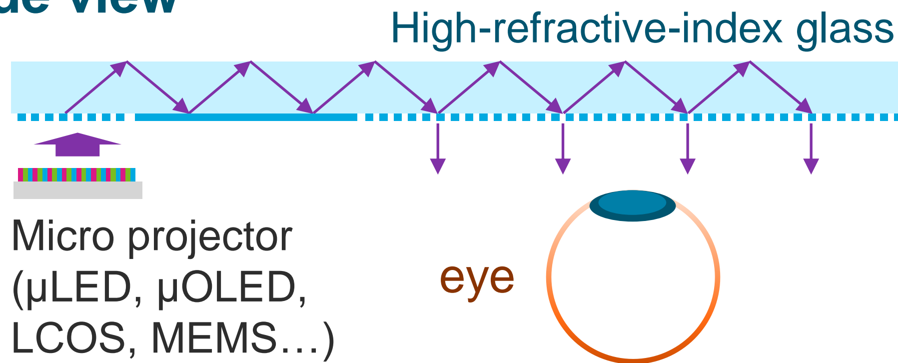
Optical Wavelength and Photonics on Wafer Opportunities



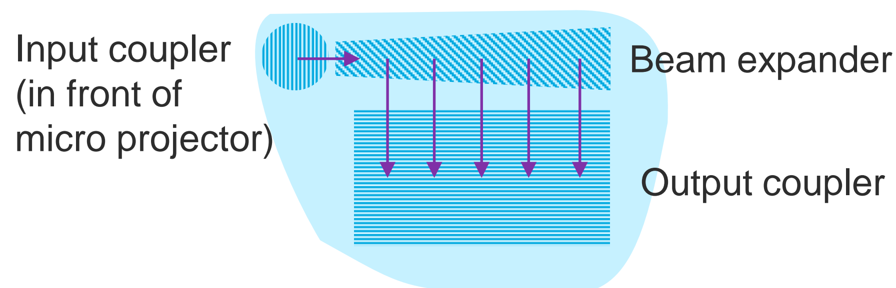
Optical Architectures of AR Waveguides

Typical AR Optical Architecture

Side view



Top view



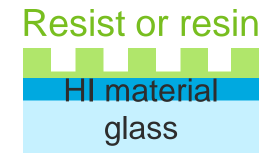
Grating Formation Methods

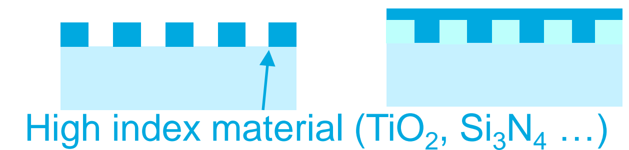
Materials & Patterning

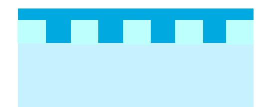
Photolithography
Or NIL (nanoimprint)

Etched film

Gap-fill







High index material (TiO_2, Si_3N_4 …)

Shape

Binary

Few-step

Blazed

Slanted

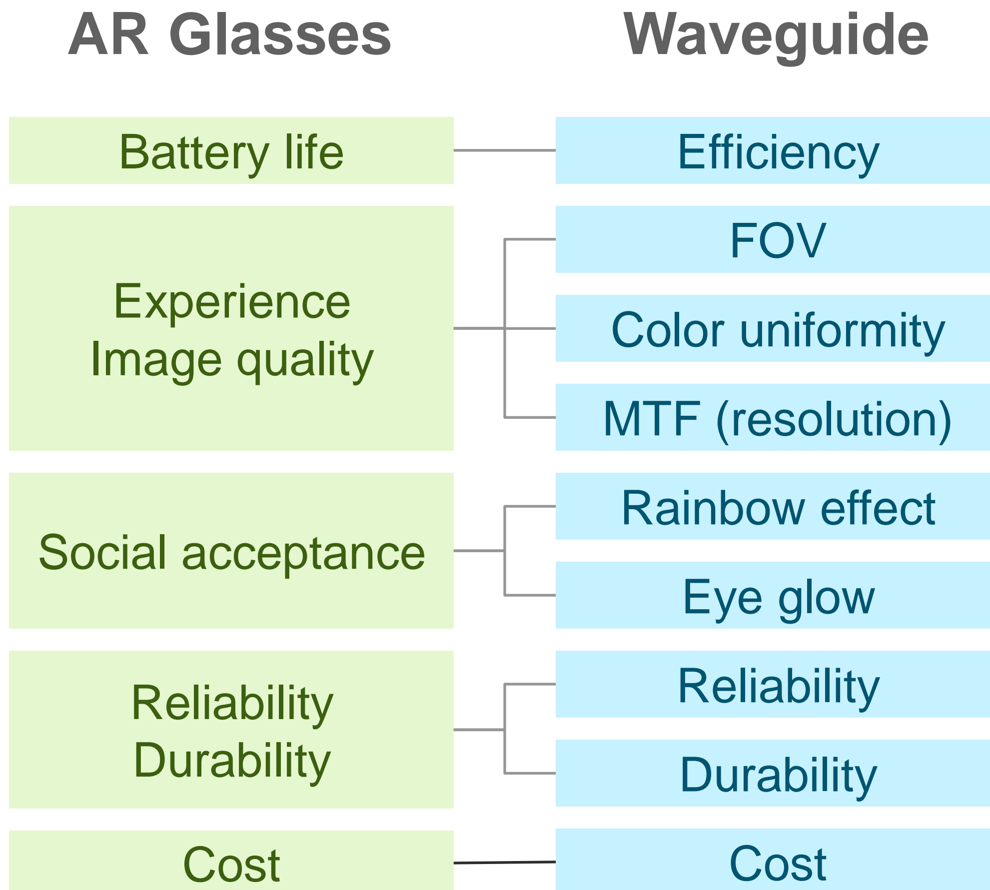
Geometry

Grating pitch : 200 to 400 nm
CD of structures : typically 50 nm

Lithography

Nanoimprint as mask for etching, photolithography etc.

Design Tradeoffs of Waveguides for AR Glasses



Ideal Product

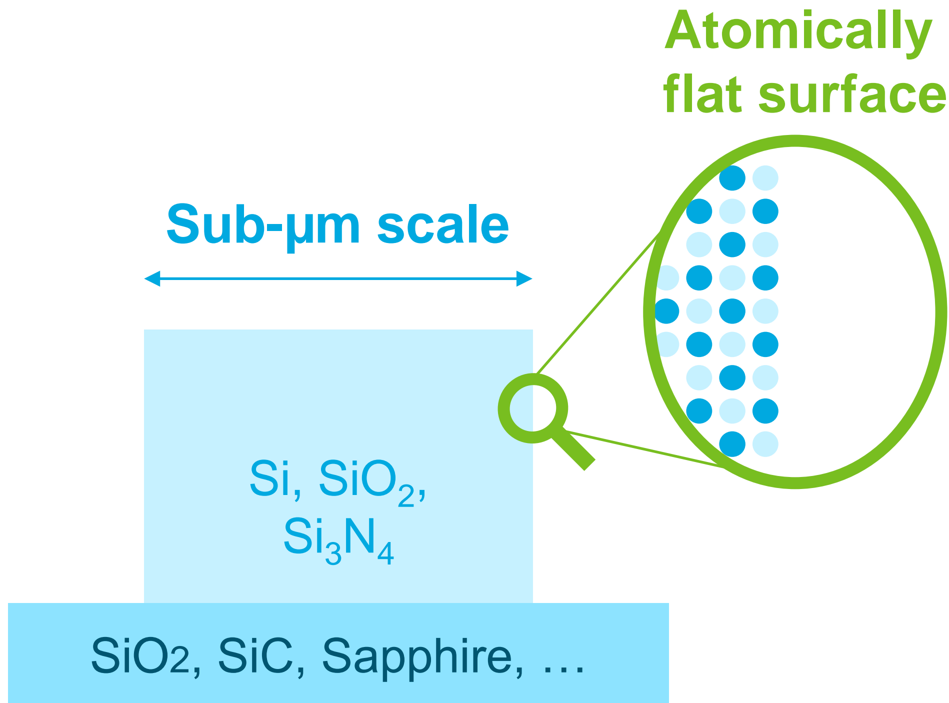
- Lightweight, stylish, lower cost, long battery life

Challenges

- Film quality – high RI with no crystallization
  - Precursor chemistry
- Waveguide profile control – uniform profiles and depths
  - Slant
  - Binary/multi-depth gratings

Scalable deposition and etching of high-RI materials will open pathways for AR waveguide manufacturing

Key Process Technologies for Photonics Waveguide Formation



Challenges

- Quality conformal coating & passivation
  – ALD, LPCVD, PECVD
- Waveguide profile control
  – Uniformity and surface roughness
- Low damage etching
- Precise surface trimming and smoothing
  – ALE, wet cleaning
- Target LER <1nm

High quality deposition and atomic scale etching required to meets photonic waveguide requirements

Key Challenges in µLEDs

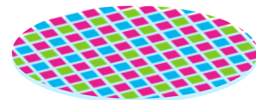
Typical µLED structures

Front-side coating / lens (improve directivity)

Mitigation of side-wall damage

Back-side reflector

Transfer / reconstitution



CMOS backplane

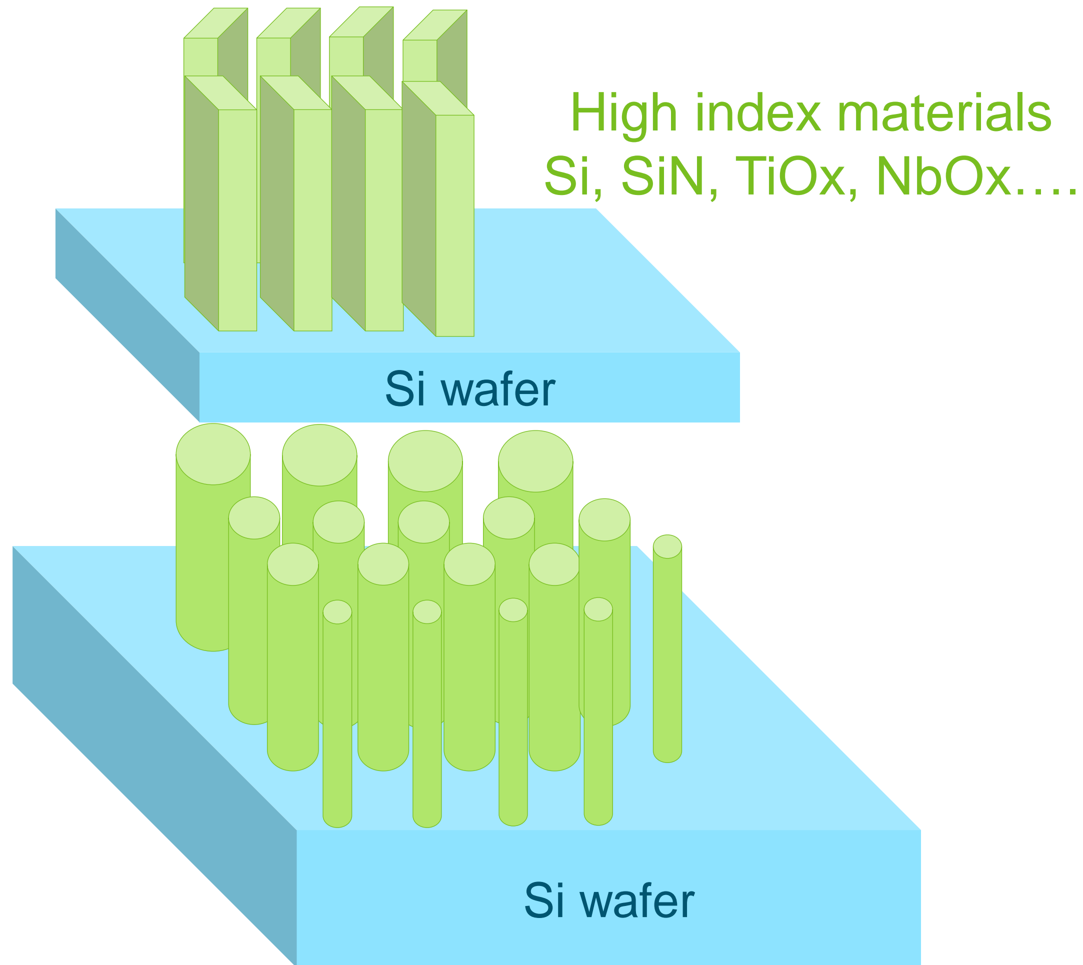
µLED wafers (typically, smaller size)

Challenges

- Mitigation of side-wall damage
  - Dry etching of III-V materials
  - Wet cleaning
  - Removal of damaged layers
  - ALD / CVD for passivation (such as SiN)
- Optical-quality thin-film formation
  - Conformal formation of multi-layer reflectors
  - Spin-on films for gap fill and other purposes
- Bonding / Test & Repair
  - Die (from 6 or 8 inch) to Wafer (12 inch)

Micro LED high brightness, contrast and efficiency make it an ideal candidate as micro projectors in AR-glass architecture once technology matures

Metalens Process Challenges



Challenges

- Uniform high-index film deposition
- High aspect ratio pillars – profile control
- High density to low density features – loading effects
- Large size metalens (mm or cm scale):
  - High data density (nm structures on a 4-inch/8-inch/12-inch wafer) – see table below
  - Photomask fabrication
  - Uniform etch across
  - Fabrication on a non-Si substrate, e.g. SiO_2, sapphire, soft material

Design file size increases rapidly with metalens size

Special compression algorithms needed

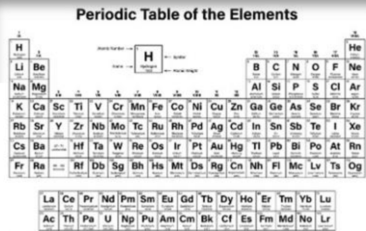
Device diameter	Meta-element count	Uncompressed file size (B = Byte)	METAC file size
10 µm	150	19.8 kB	9.1 kB
50 µm	3,614	157.9 kB	44.5 kB
100 µm	14,068	501.4 kB	94.1 kB
500 µm	1,053,822	30.3 MB	972.1 kB
1 mm	3,204,089	91.2 MB	1.9 MB
5 mm	73,194,422	2.2 GB	11.0 MB
10 mm	291,697,949	8.8 GB	23.3 MB
50 mm	6,853,721,364	205.7 GB	131.1 MB

Source: Optics EXPRESS, Vol 26, 2, Pp.1573-1585

Manufacturing Challenges and TEL Tool Solutions

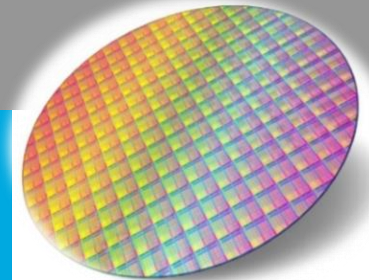
Optical Device Manufacturing Challenges

Materials



- Optical quality films:
  TiOx, SiN, SiOx
- Metamaterials:
  GaN, TiOx, MbOx…
- Optics: BTO, NbN, NbO

Substrates



- SiC, glass, sapphire
- 4”, 6”, 8”, 12”
- Rectangle, square

Diverse Devices

- Waveguides
- Display:
  LED, μLED, OLED, LCOS
- Sensors: CIS, LiDAR

Cost & Reliability

- Strict reliability standards
- Cost Effective

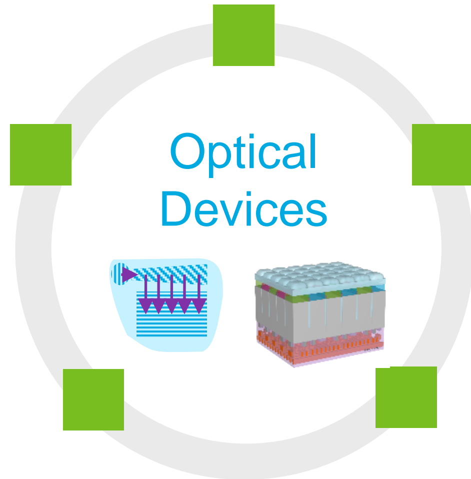
TEL

Wafer Bonder/Debonder

Synapse™ Series

Coater / Developer

Coater / Developer
CLEAN TRACK ACT™ 8 / LITHIUS Pro™



Deposition

Diffusion / ALD / LPVCD / PECVD
TELINDY PLUS™ / NT333™
ALPHA-8SE™ i / MZETA™

Etch

Dielectric and Conductor Etching
Tactras™ / UNITY™ Me

Surface Preparation

Batch Spray Cleaning
ZETA™

Cleaning System
CELLESTA™-*i* / EXPEDIUS™-*i*

Solutions Offered

- Glass wafer handling/processing capability
  - Thickness, weight, conductivity
- Scalability from ≤200mm to 300mm capable
- Utilize existing HW design to lower cost

Key Enablers for High Volume Manufacturing

Deposition

Diffusion / ALD / LPVCD / PECVD
TELINDY PLUS™ / NT333™
ALPHA-8SE™ i / MZETA™

- High quality, defect free films
  - Si photonics waveguides: Si, SiN
  - AR/VR waveguides: TiOx
- Excellent film uniformity
- High throughput
- Extend HVM proven hardware

Etch

Dielectric and Conductor Etching
Tactras™ / UNITY™ Me

- Atomic layer precision etch
  - Si photonics waveguides: Si, SiN
  - AR/VR waveguides: TiOx
  - MicroLED: low damage MQW mesa stack etch, vertical sidewall
- Extend HVM proven hardware

Summary

- Applications for optical devices continue to expand, driving need to solve manufacturing challenges
- Growth and adoption will complement leading edge technologies like AI
- HVM requires robust capability for 200 and 300mm
- TEL is leveraging experience and BKMs from CMOS based devices to enable solutions beyond Silicon
- TEL provides scalability with proven HVM reliability to address MAGIC device requirements
- Collaboration is key to accelerate manufacturing readiness

Thank you!

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