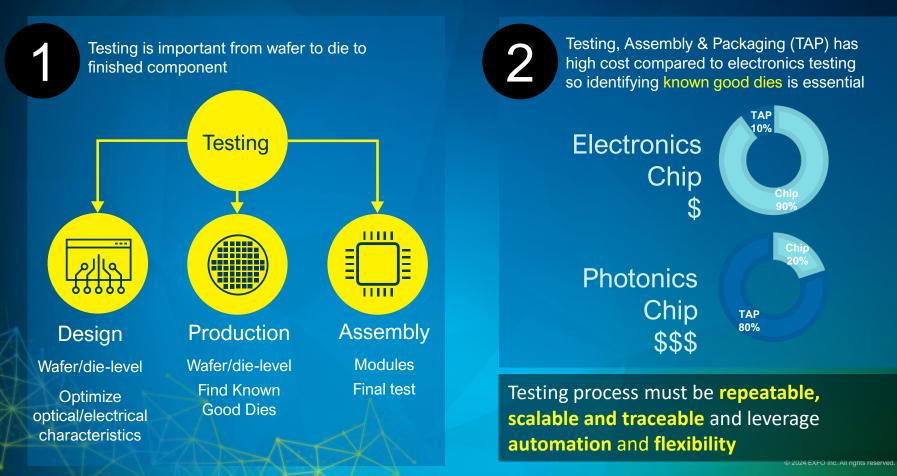
UNLOCKING EFFICIENCY, STRATEGIES FOR ENHACED PIC TESTING PERFORMANCE

Sophie Lange, Business Development Engineer

EPIC Technology Meeting on Photonic Integration and Packaging at Fraunhofer IZM



Why testing is important process in PIC technology?



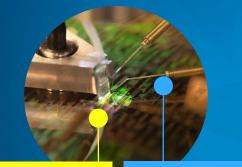
The 3 Steps of Testing

Optical Fiber Coupling & Electrical Probing



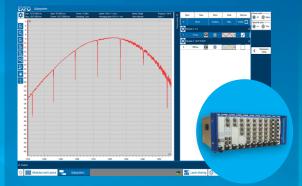


Data Management and Analysis



Optical fiber array

Electrical probe







PIC Testing Bottlenecks

- 1. Time to align fiber Manual processes
- 2. On-chip navigation Moving next component to the probes

3. Pick and place

Loading dies one-by-one onto the probe station

4. Test time

Time to control and run test instruments

5. Disconnected interfaces

Motion control, test instruments, data handling on multiple platforms from different vendors

6. Data handling

traceability throughout process chain, completeness of data including all parameters, experimental conditions etc.

6. No standardization

Variety of components require flexible test setups

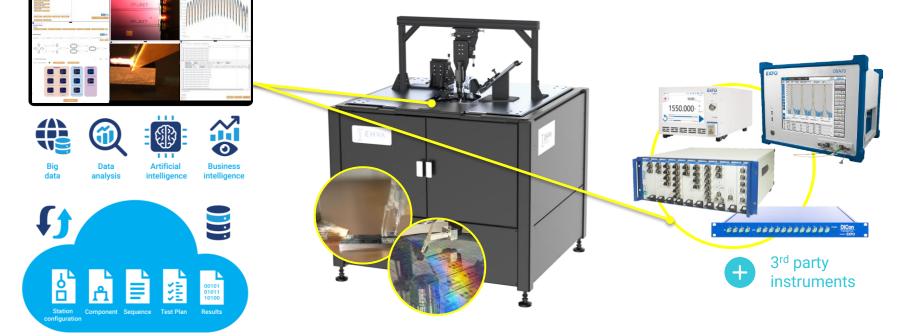
Enhancing Testing Efficiency

Full automation of motion control, instrument drivers and database from single interface

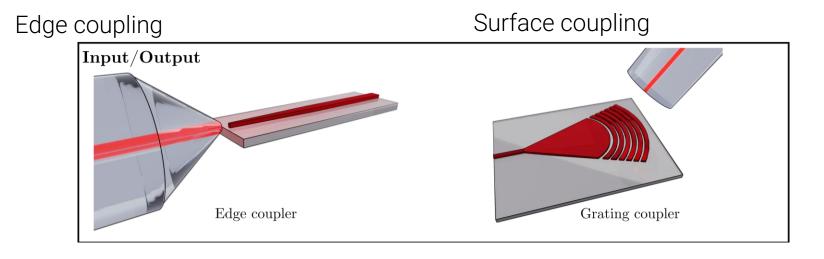
Test orchestrated from single software interface

Flexible single-die, multidie or wafer tester

Instrumentation for full characterization



Optical Fiber Coupling: Surface vs. Edge



Pros: high coupling efficiency, broad bandwidth, polarization independent

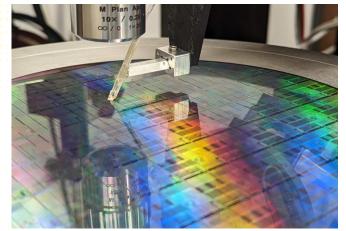
Cons: need cleaved facets, large spot-size converters to match mode size to fiber

Pros: grating couplers can be integrated anywhere on PIC, no cleaving needed

Cons: limited wavelength range, polarization dependent, higher coupling loss

Wafer-Level Edge Coupling

Wafer-level edge coupling using OPAL-EC



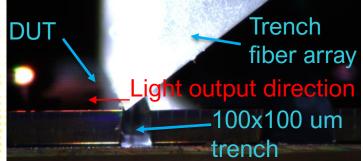
No need to separate wafer into dies for testing

Safe time, cost and effort to manually pick, place and test dies individually

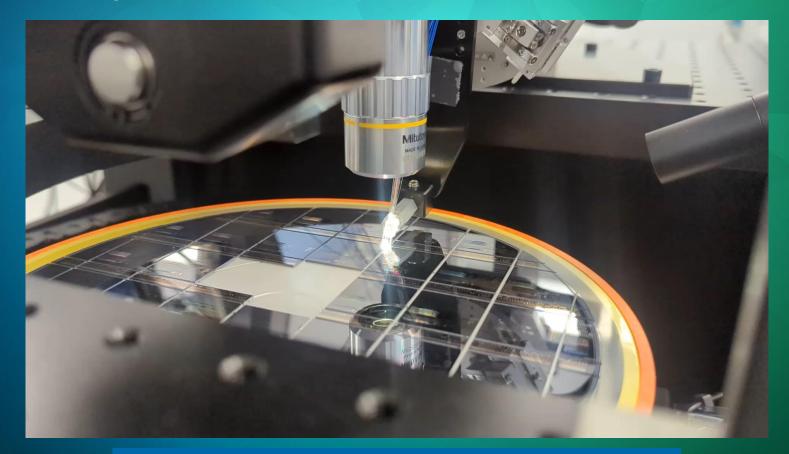
Leverage best coupling performance of edge coupling

High accuracy and repeatability key to assure no collisions during wafer test

Multi-port edge coupling for parallel testing



Running Automated Test Plans

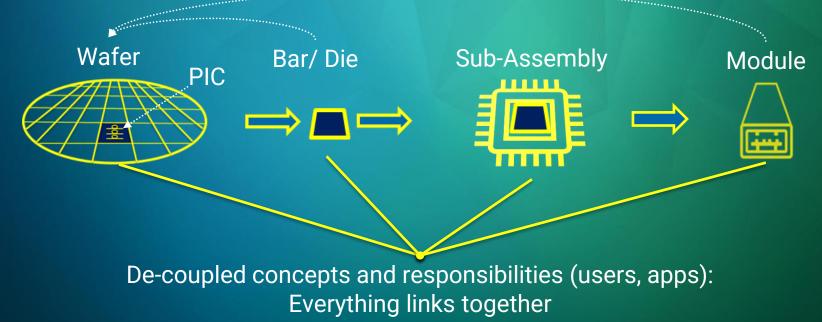


Link: https://cdn.jwplayer.com/previews/n0j3TUSV-xpehj8NL

Life of PIC - from wafer to module

Reusable and connected test environment from wafer to module

Flexible definition of test/analysis scripts, wafer/reticle/die parameters, locations and structure



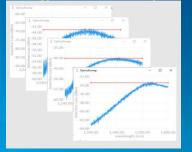
Machine learning to Cut Test Time and Costs

Data-driven live decision-making flow

Skip predicted bad circuits

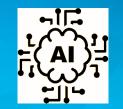


2. Extract figures of merit using batched analysis



3. Build custom datasets from database





4. Train predictive models with machine learning training sequences

🧎 Training Complete	-		×
Best Trainer: SdcaRegression . Train Score: 7.31438747164	3784 S	ave Mod	el ?
Yes No			

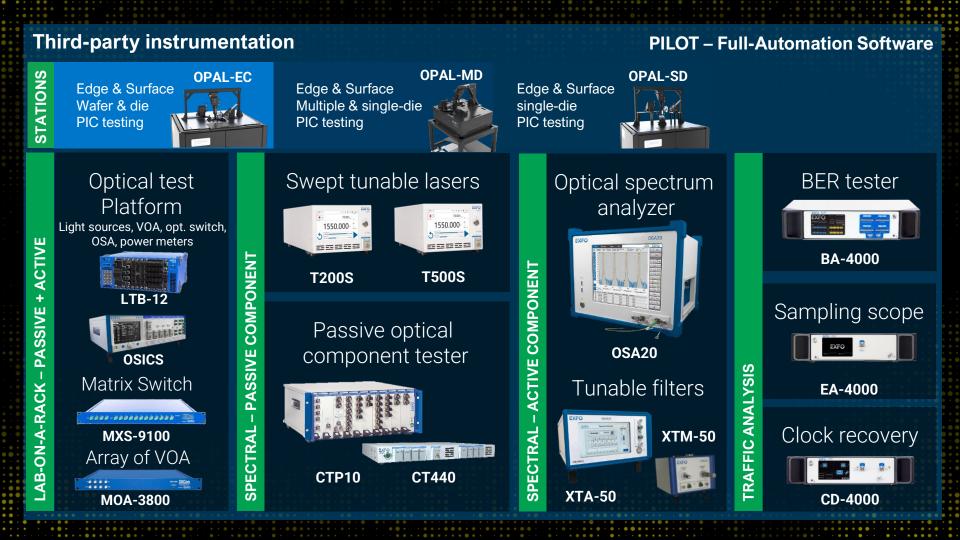
5. Consume predictive models inside test logic



- 0

X

The model predicts that this component is not good enough for our standards. Moving on to the next component, in order to save time. Thank you!



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