



5th June 2023

EPIC Technology Meeting: Photonic Integration and Packaging at Fraunhofer IZM

# Scaling up the photonic testing back-end





# About us

- VLC Photonics offers Photonic Integrated Circuit (PIC) engineering services, focused on design and testing.
- **C** Company founded in 2011.
- **C** Offices and clean-room labs in Valencia Technological Campus (Spain).
- **E** 28 members of extensive academic and industrial experience, and keep hiring.
- Part of Hitachi High-Tech group since 2020.

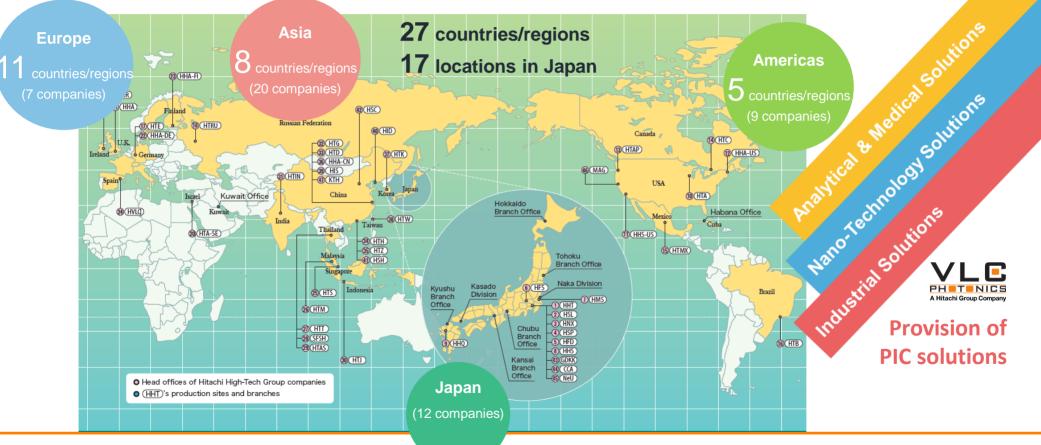




# About us (II)

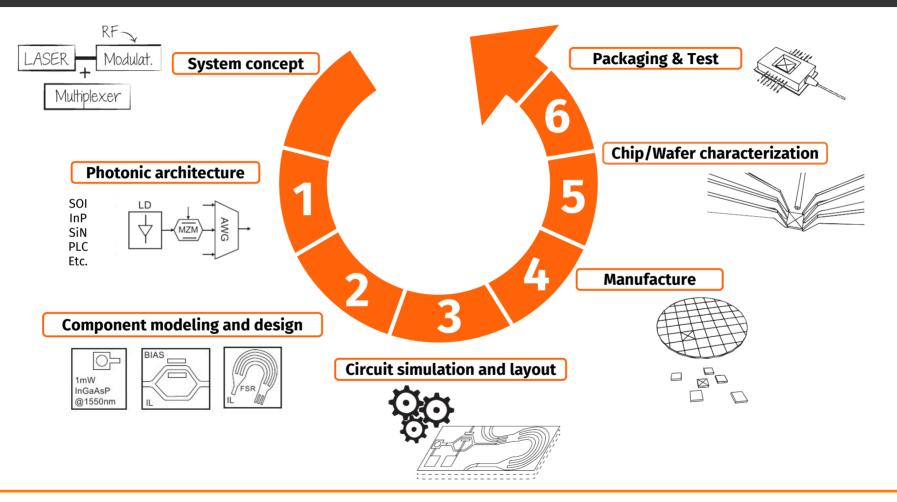


# **OHITACHI High-Tech Corporation**



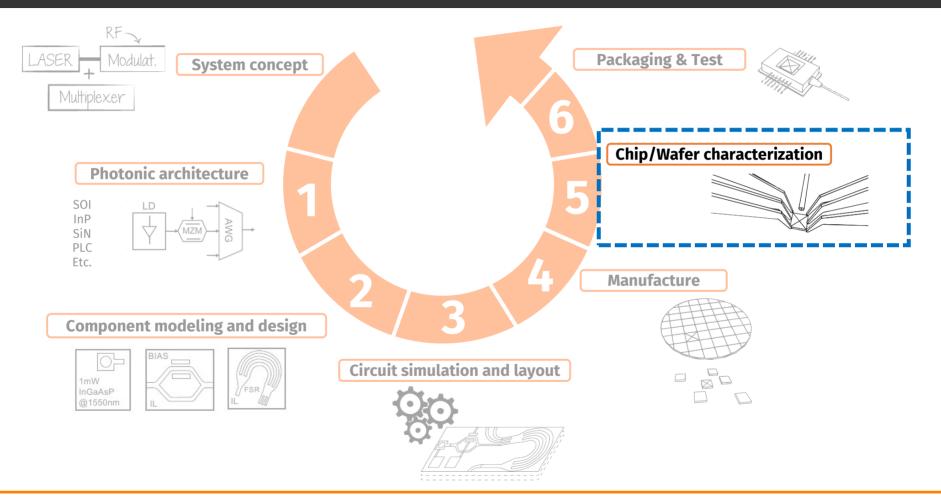
# **PIC development cycle**





# **PIC development cycle**



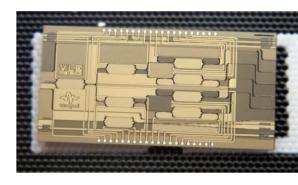


# Characterization and test needs



- It is still critical to do extensive component / circuit characterization when validating PIC designs in engineering.
  - To validate fabrication process and its tolerances through sensitivity analysis (specially needed in photonics).
  - To confirm the intended layout functionality, and feedback the designs for statistical modelling.
  - To sort out known good dies (KGD) and provide feedback on foundry yield, for accelerating ramp up.
- When moving to PIC volume production, scalability becomes an issue:
  - Functional circuit testing is still required beyond fab metrology and PCM.
  - Need fast and low cost Wafer/KGD sorting/binning before packaging.
  - Significant CAPEX for parallelization, engineering and setup time required.







# **Characterization & Testing facilities**



VLE 1172

#### Two clean room labs (ISO class 6 and 8) with:

- C Optical microscopes & SEM for detailed visual inspection
- **C** Optical (vertical and edge light coupling) and electrical probing:
  - **E** 5 semi-automated bare die characterization setups
  - **E** 1 manual electrical wafer tester
  - **E** 2 fully automated opto-electronic wafer testers
- E Electrical measurement instrumentation for DC and RF signal testing up to 110 GHz and optical equipment to work from visible (400 nm) to mid-IR (up to 5 μm).
- **E** Test assembly:
  - **I** manual & 1 automated wire-bonder
  - **E** 1 flip-chip tool



# **Automatic Testing at VLC Photonics I**



#### **DEVICES**

Our Wafer Level Testers are adapted to work with:

- Wafers, up to 12 inches.
- Bars, up to 12 inches.
- Diced chips (from 1mm x 1mm above).

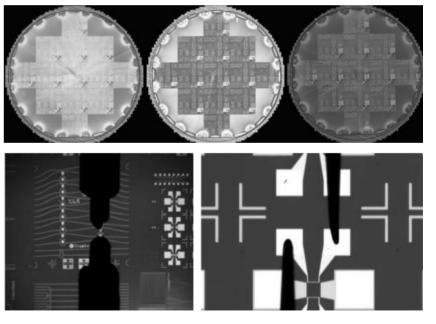
## **E** ELECTRICAL PROBING

We have capabilities to do electrical testing from all 4 sides of the chip.

- DC Probing
  - Single needle.
  - MCM (Multi Contact Needles). Std. pitch: 100um, 150um and 250um.
- RF Probing
  - GSG. Std. pitch: 60um.
  - Up to 110GHz measurements.



SOUTH



# **Automatic Testing at VLC Photonics II**

#### OPTICAL PROBING

We have capabilities to do optical testing from **West** and **East** sides of the chip. North and South stages just can be used for electrical probing.

#### **E** Vertical coupling (All types of devices)

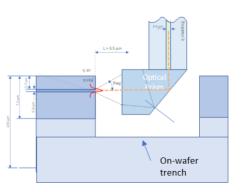
- Cleaved fibers
- Fiber Arrays (FA)
- Leadless Fiber (Leadless FA)
- With or without Anti Reflection Coating (ARC)
- With automatic polarization control.

#### **E** Edge coupling (Bars and Diced chips)

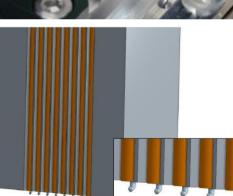
- Cleaved fibers & Lensed Fibers
- Fiber Arrays (FA)
- Fiber Arrays with lensed fibers (Lensed FA)
- With or without Anti Reflection Coating (ARC)
- With automatic polarization control.

#### **E** Extra: Edge coupling with periscopes

• For non-diced wafers with trenches.









# **Automatic Testing at VLC Photonics II**

## • OPTICAL PROBING

We have capabilities to do optical testing from **West** and **East** sides of the chip.

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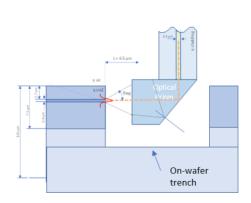
#### E Edge coupling

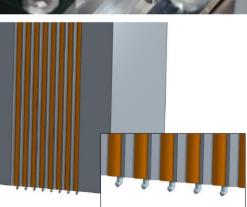
- Cleaved fibers & Lensed Fibers
- Fiber Arrays (FA)
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- With automatic polarization control.

#### **E** Extra: Edge coupling with periscopes

• For non-diced wafers with trenches.

- We are open to evaluate all kinds of projects.
- We did even adapted our WLTs to use **integrated lasers** as optical probes.









U

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Parameter

T: Optical ports pitch

U: Optical ports clearance area

W: Vertical safety distance

V: Optical ports vertical coupling angle

• Assembly Design Kits (ADKs)

W

7° to 13°

30 um

Minimum requirement

1250 µm (for standard FA)

127µm / 250 µm

**Testing layout guidelines.** 

Available for some foundries and EDA software frameworks. Compatible with test and packaging requirements.

Recommended

127um / 250 um

We gathered all the specs to be required by the chip design

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	Testing Layout Guidelin	es
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Recommended

127μm / 250 μm

250 µm

10°

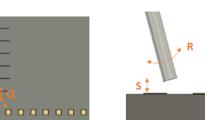
Minimum requirement

50 um

127µm7250µm	F. Optical ports pitci	11	50 µm	1
1500 μm	Q: Optical ports clea	irance area	50 μm	
10°	<b>R: Optical ports vert</b>	ical coupling angle	7° to 13°	
	S: Vertical safety dis	tance	30 um	

Parameter

**D: Optical ports pitch** 





#### **Examples of previous projects:**

DUT	Structures	Measurements
Six 6" wafers, >300 dies	>5k	~50k
Two 8" wafers, >1800 dies	>14.5k	~58k
>50 dies	>140	>31k

#### **Example times**

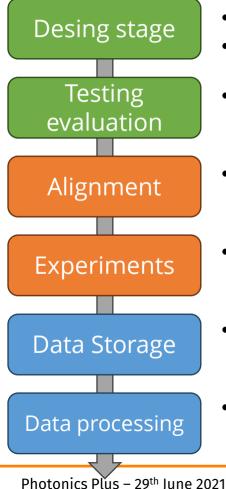
Probing time:	4 s
Measurement time:	1 s
# measurements:	50k

TOTAL TIME = ~3 days

- Fast probing and trace acquisition times are essential when scaling up.
- Smart characterization plan and execution is a must for insightful but time-practical test campaign.
- We developed a tool to estimate the testing times considering the different types of probing we offer and the different experiments we have in our portfolio.

# **VLC Testing environment**

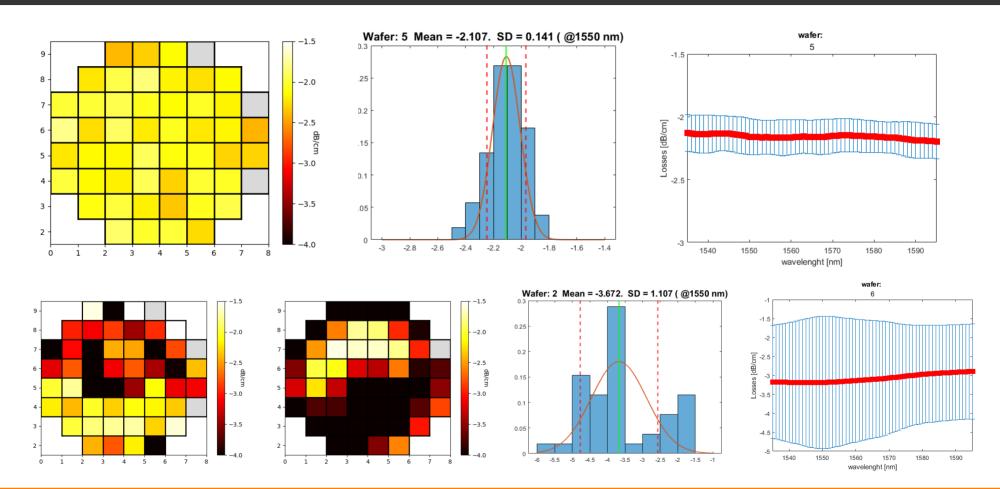




- Different software's are used.
- We automatically extract ports names and their coordinates.
- We create **tables** with the structures to test, their ports and the experiments to run in each probing position.
- Coordinates are imported into **Ficontec PCM** software and probes moved to position.
- Once in position we run the selected experiments using our python libraries to control the instruments.
- Data gathered is both saved in the VLC's database and as CSV files.
- Finally, we used python to gather the data back from the database and **auto-process** the results.

# **Process control and yield analysis**

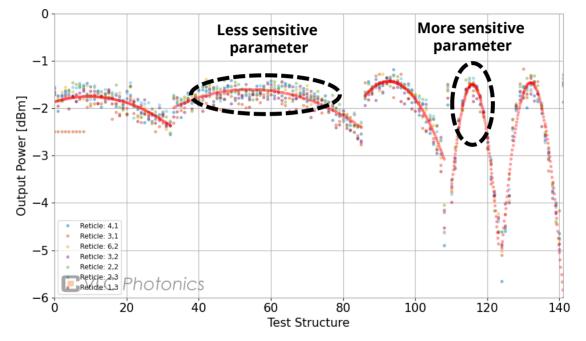




# **Component sensitivity analysis**



#### **Example of design parameters sweep over 140 test structures in 7 reticles**



- Repeatability of bare die measurements with manual alignment is poor (>0.5 dB).
- WLT ensures that alignment and trace acquisition are done automatically with minimal variations (mechanical, thermal etc.)

# **RF testing key for next-gen datacom PICs**





- Lightwave Component Analysers (LCA's) for parametric testing of devices like high speed modulators in transceivers.
  - Up to 110 GHz turn-key test system for optical RX and TX
  - Suitable for die and wafer level testing
  - Return to zero and nonreturn-to-zero (RZ / NRZ) and pulse amplitude modulation (PAM) formats
  - S-parameter testing over the full 1260 nm to 1620 nm range

# Thank you for your attention!



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