

# High accuracy placement - passive versus active alignment, benefits and challenges

D.Lieske, 04.06.2024



## Overview

- ✓ Motivation
- ✓ AEMtec at A Glance company and technology overview
- ✓ Active and Passive alignment
- ✓ High accuracy placement
- ✓ Optical and Photonics packaging examples
- ✓ Summary

### **Motivation**

- Photonics is advanced packaging
- High accuracy placement is the key for Photonics in the next decade and beyond
- There can be seen a very good development in photonics since more than a decade, e.g. Intel and IBM (now Globalfoundries by offering PIC wafers with IBM's technology), IHP, XFAB, Ligentec and others
- At AEMtec a rising demand for high accuracy placement in Photonic applications can be seen
- High accuracy placement not only needs high accuracy placement equipment
- The understanding of materials, available interconnect technologies, wafer processing and chip handling is the key
- Smart assembly techniques will be needed, new interconnect technologies need to be developed and standardized to improve manufacturability and product reliability



### **Motivation**

- Photonics IC's (PIC) are on the way, but add packaging costs
- Data center drive the development of PIC's
- with PIC's the demand for Flip Chip applications for photonics packaging with higher placement accuracy than traditional Flip Chip is rising
- FC-PIC have advantages over wire bond due to high pin count and short signal length, as well as capability of integrating optical elements in photonic IC's
- But as integrated laser are still expensive VCSEL, Photodiodes and TIAs are widely used for optical applications
- For both solutions the fiber attach is adding packaging cost and complexity
- If high precision placement can be done and active alignment of fibers can be avoided it reduces cost

The challenge of Photonics IC packaging and fiber connection

High accuracy die placement + V-groove passive fiber placement

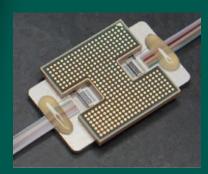
Optical fiber

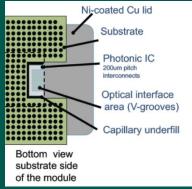
PIC

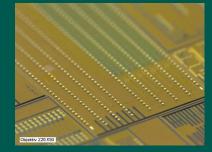
ASIC

Interposer (Glass, Silicon or Organic)









1 + 2 Source: IBM 3 source: AEMtec

### **AEMtec at A Glance**

### We are:

- 220+ employees
- 70 Mio<sup>+</sup> € Revenue
- Headquarter and Production: Berlin Adlershof
- 2000 founded as Spin of from Infineon Fiber Optics
- 9000 m<sup>2</sup> facility including sufficient space for our employees, offices, production and test equipment (3000m<sup>2</sup> clean room, ISO 5, 6 and 7)
- Today the team of AEMtec is proud to count more than 60 customers worldwide and over 500 realized projects



Introduction

# What is unique about AEMtec?



### We are:

- A unique Semiconductor packaging service provider in Europe
- A full service address for Wafer backend, Advanced packaging and Test
- A strong partner with leadership in high accuracy placement under ISO5 cleanroom condition
- Very flexible and innovative in finding solutions for customized products
- Well equipped for mid volume manufacturing products in ISO 5, 6 and 7



### **AEMtec - Process line up**



Wafer back-end

High-precision packaging & testing

Positioning, soldering, testing

System Integration

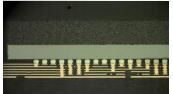
UBM, balling, dicing

Flip chip

Surface-mount technology

Complex product assembly







Chip on board





- Under bump metallization (UBM)
- Solder balling
- RDL or FOWLP
- Au-stud bumping
- Wafer Dicing

- Soldering
- Gluing (ACA, ICA, NCA)<sup>1)</sup>
- Copper pillar
- Thermocompression
- Underfill

- Die bonding
- Wire Bonding
   Al and Au wedge and ball bonding
- Encapsulation
- Solder Cap
- Heat spreader

- Pick & Place
- Selective soldering
- BGA Rework
- Milling or Laser-cutting
- AOI
- X-Ray

- Product codevelopment
- Prototyping + industrialization
- Serial production including repair service
- Worldwide supply

# We provide Wafer Services, SMT, Chip on Board, Flip Chip and high end system integration to our customers worldwide

### **Examples:**

- ✓ X-ray detectors
- ✓ Light sources (VCSEL or LED)
- Multi-channel optical transceivers
- ✓ Optical Systems
- ✓ RF-chip packages on SiGe
- UBM and Solder bumping of PIC Wafers
- ✓ Photonic SiP
- ✓ MCM, 2.5D / 3D SiP

## Active and passive alignment - a comparison



### Active alignment

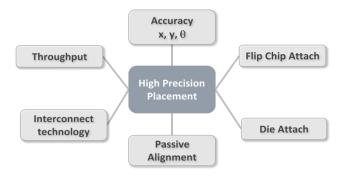
- only where needed
- more complicated setup
- accessibility required, DFM (Design for manufacturability) is needed in early development of the product
- Slower than passive alignment

### Passive alignment

- down to 0,5μm is the easier process
- higher throughput, up to 500 UPH → price benefit
- lower invest
- use PIC's, Lenses or TIR<sup>1)</sup> with V-grooves
- use ferule and alignment pin approach
- alignment mark quality is mandatory (DFM)

# High accuracy die bonding (Passive)

### Throughput under high accuracy is key for competitiveness and price



high precision placement- What matters?

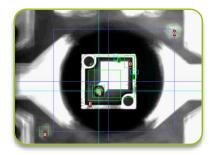
### Placement accuracy depends on interconnect technology

| Interconnect technology | Temperature | Force       | Method                      |             | Accuracy               | Throughput (die bond and cure) |
|-------------------------|-------------|-------------|-----------------------------|-------------|------------------------|--------------------------------|
| Adhesive                | low         | low         | stamp, place, batch cure    | high        | <1,5μm                 | medium                         |
| Thermocompression       | high        | high        | bond, heat                  | high        | <3μm                   | medium                         |
| Pressure sintering      | high        | high        | bond, heat, pressure anneal | medium      | <10μm                  | medium                         |
| Soldering               | high        | low         | place, mass reflow          | low         | <20µm (<5µm advanced*) | high                           |
| TLPS                    | high        | medium high | bond, heat, anneal          | medium high | <3μm                   | medium                         |
| Hybrid bonding (D2W)    | low         | medium high | clean, bond, anneal         | high        | <1µm                   | medium                         |

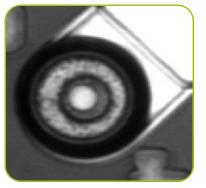
<sup>\*</sup> more information on request



# On chip structures to be used with good contrast







# **Examples**



### Telecommunication:

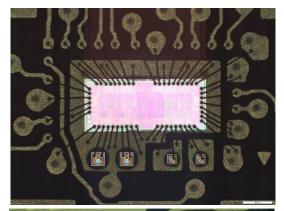
- 100Gbit Rosa (Receiver Optical Sub Assembly) x,y < 2,5μm
- Network pluggable, long distance, 100Gbit, (SMF-ready, ferule)
- Transceiver fiber to chip coupling for Gbit/s link in data centers, MMF
- Optical cable (MMF)
- High accuracy TIR bonding
- High accuracy Lens bonding

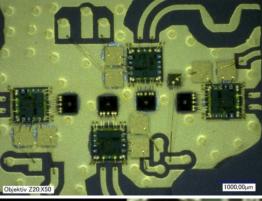
### Industrial:

- Laser distance measurement Z-height <1µm (passive + active alignment)</li>
- Motion control sensors, VCSEL
- Optical sensors
- VCSEL arrays for illumination and heating

### Medical

- Photodiode/LED integration for implantable devices
- CT-scanners



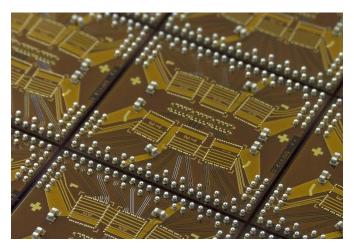


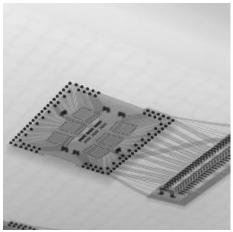


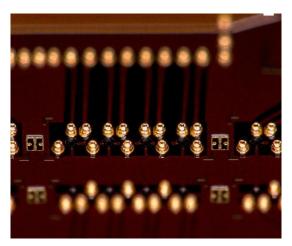
# Telecommunication - Flip chip package for Data centers



• As an example **optical Flip Chips** with an accuracy of +/-3µm are specified to be placed onto a substrate. Doing that - equipment and material, as well as temperature control does have a major influence on the final placement accuracy





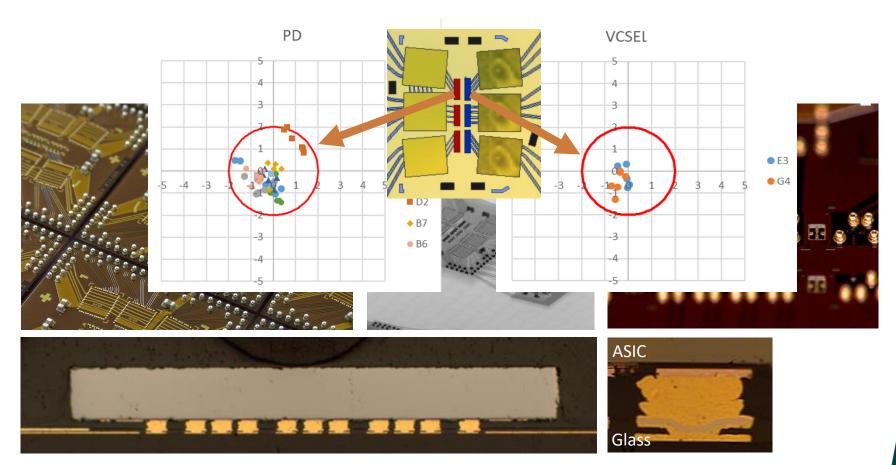


- ✓ Au- studbumping
- ✓ Flip Chip
  Thermocompress
  ion +/-2,5 μm

# **Telecommunication - Flip chip package for Data centers**



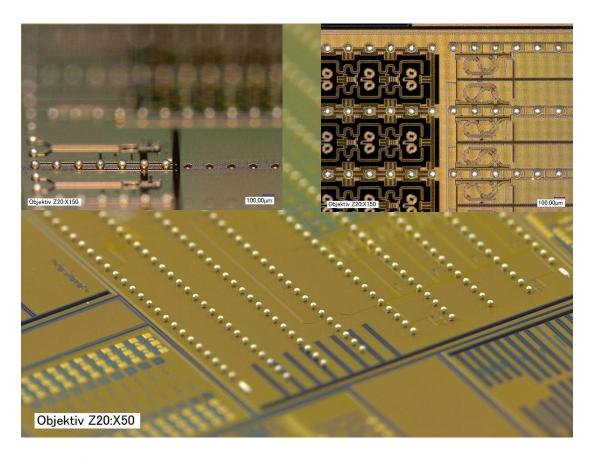
• Results: Thermocompression bonding with +/-2,5μm accuracy

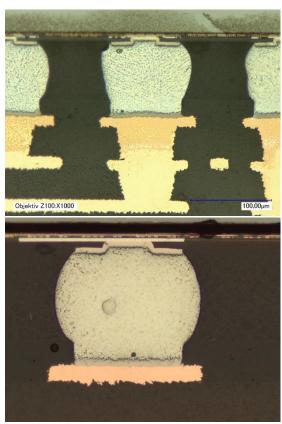


- Au- studbumping
- ✓ Flip ChipThermocompression +/-2,5 μm

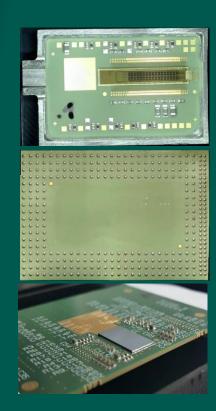
# Flip Chip - Photonics Wafer

- Flip Chip photonics wafer (UBM, solder balling and packaging)
- Electroless plating ENIG, Solder balling SAC305 or low melting alloys





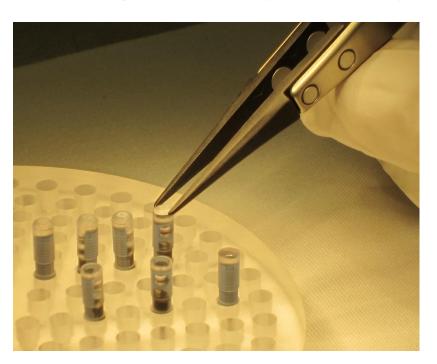


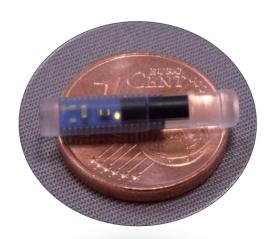


Silicon Photonics
Enabling Exascale Data
Networks — SPEED

# Medical - optical blood sugar sensor

- There is optics in!
- Wafer → UBM → Chip to wafer soldering of Photodiodes → system assembly
- Cleaning and biocompatible encapsulation (implantable device)

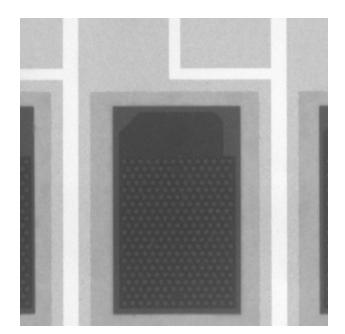




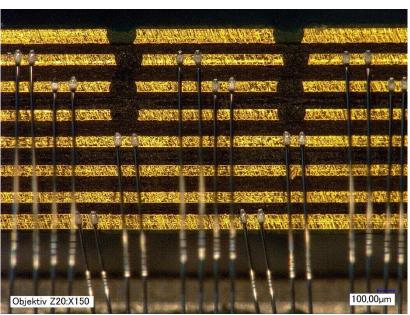


# Industrial - VCSEL based high power laser module

- Void free AuSn soldering of VCSEL
- Speciality: Wire Bonding onto PCB edge (vertical)



Void free AuSn soldering



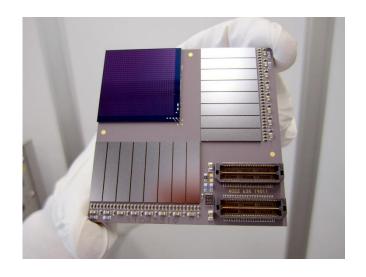
Wire Bonding onto PCB edge



✓ VCSEL Arrays

# Semiconductor









- ✓ MEMS Mirror
- ✓ VCSEL light source

### **Summary**

- Optical packaging with high accuracy placement and photonics packaging is available in Europe
- We want to convince customers, that not only development but volume manufacturing of photonics and RF packaging can be in Europe → investments are ongoing
- Next Photonics packaging will be a driver for development of new interconnect technologies
- There needs to be a strong network in Europe that combines it's capabilities
- EPIC association is doing a great job, (AEMtec is part of it)

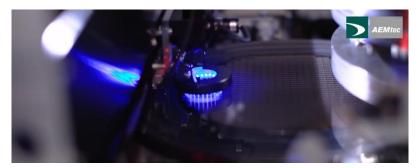
  "EPIC drives the competitiveness of the European photonics industry"



PhotonicsPackaging is a chance for Europe

# **AEMtec Career**







**AEM**tec









Success is build by people.

Come and join us!

www.aemtec.com/karriere

# **AEMtec Network in Europe & worldwide**





- Central Position in Europe
- ✓ Worldwide Customer Network
- Strong Institutes Network
- Strong Foundry Network



# **Your Strategic Technology Partner**

**THANK YOU!** 



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