Welcome and Introduction of Fraunhofer IZM

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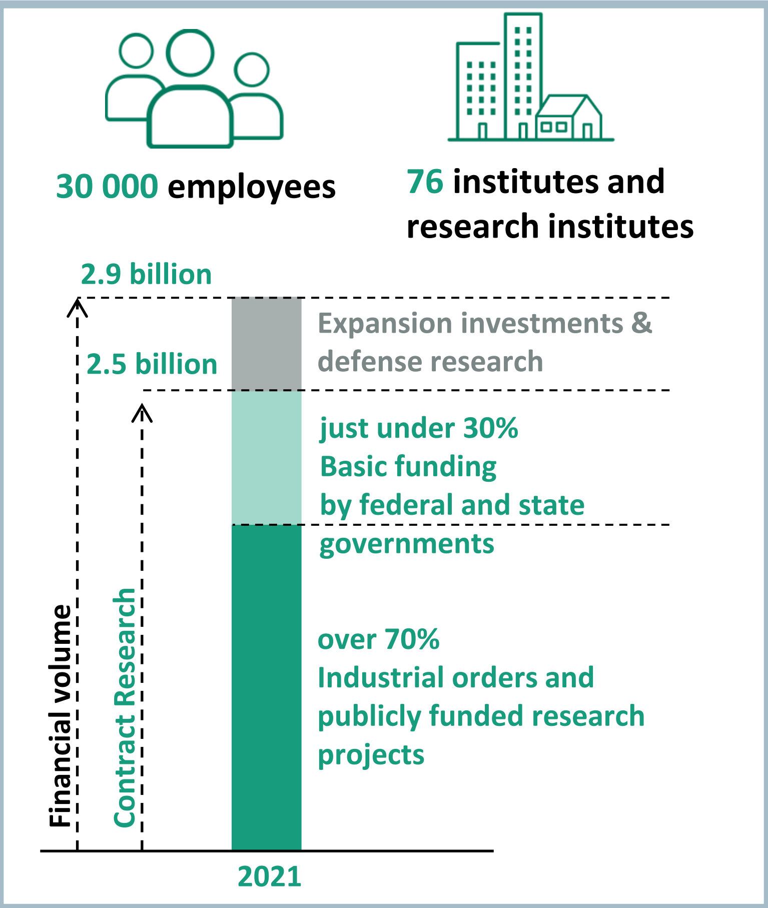
Fraunhofer
IZM
Fraunhofer Institute for Reliability and Microintegration IZM

The Fraunhofer-Gesellschaft

Application-oriented research with a focus on future-relevant key technologies as well as on the utilization of the results in business and industry.



Forschungsfabrik Mikroelektronik (FMD)

- Facts and Figures

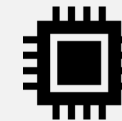
560 m EUR Budget

200 m EUR projects/industry

235 m EUR projects/public funding

125 m EUR basic funding

2.2 bn EUR assets / investment



Design (down to 10/12 nm)
Wafer Processing:
GaAs/InP (4”), SiC (6”)
Si, SiGe, GaN (8”), Si (12”)
Advanced Packaging up to 12”; 600 mm panel
System Integration
Test & Characterization

11 institutes from **Fraunhofer**

2 institutes from **Leibniz**

Approx. **4,500** employees with **2,635** scientists

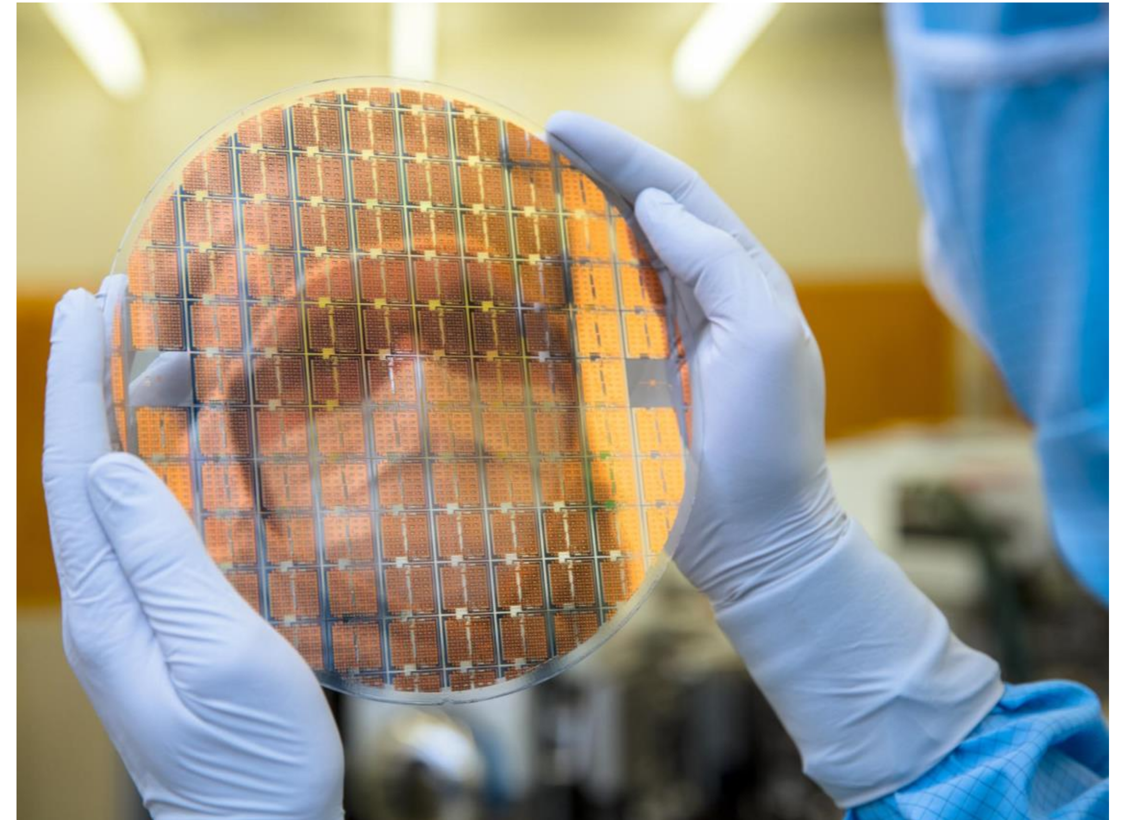
Fraunhofer IZM

Three facts about our institute

1 — is one of the world’s leading institutes for applied research and the development and system integration of robust and reliable electronics.

2 — means 29 years of novel technological solutions developed in cooperation with partners from industry and academia.

3 — is the only fully integrated packaging institute covering everything from design, technology, reliability, and eco-assessments.



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Fraunhofer IZM at a glance

30 years of experience

438 employees (incl. students and trainees)

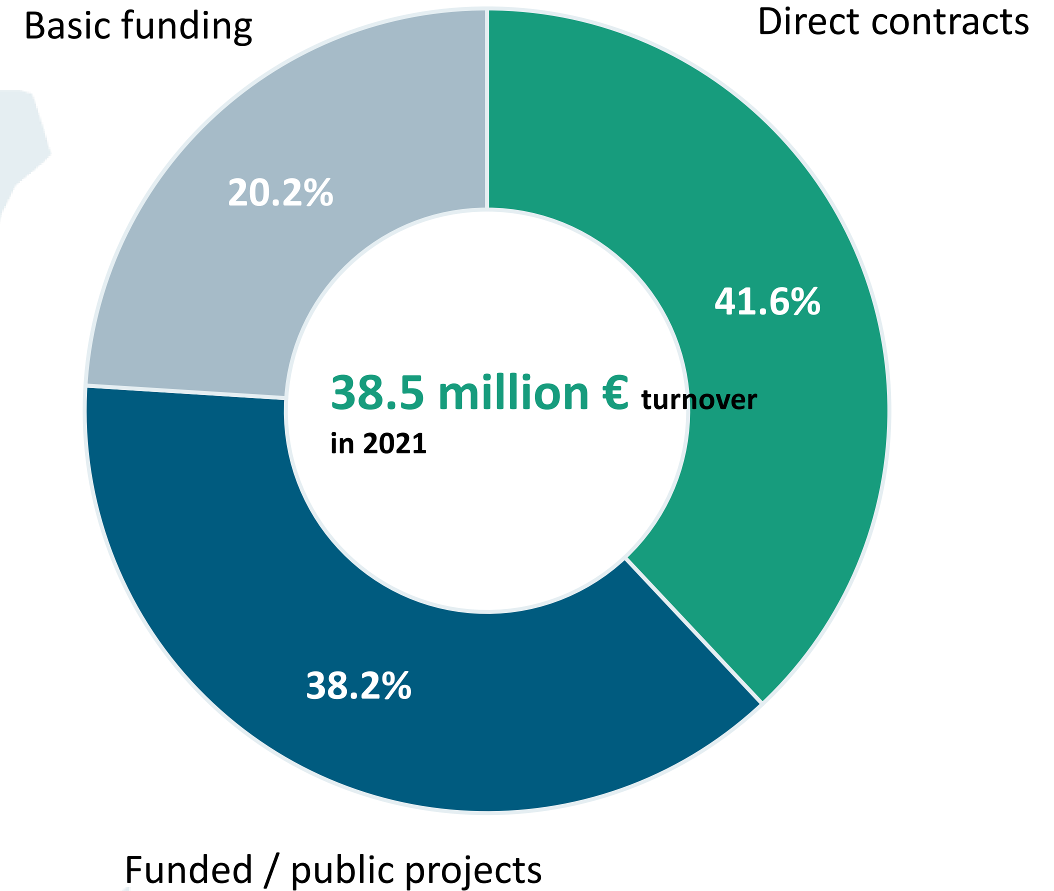
- 132 interns, bachelor students, master students and student assistants have been supervised at Fraunhofer IZM
- 8 trainees have successfully completed their training

5,374 m² laboratory space

69 labs and measurement spaces

Long-term contracts with

- Technical University of Berlin
- Technical University of Dresden
- Brandenburg University of Technology



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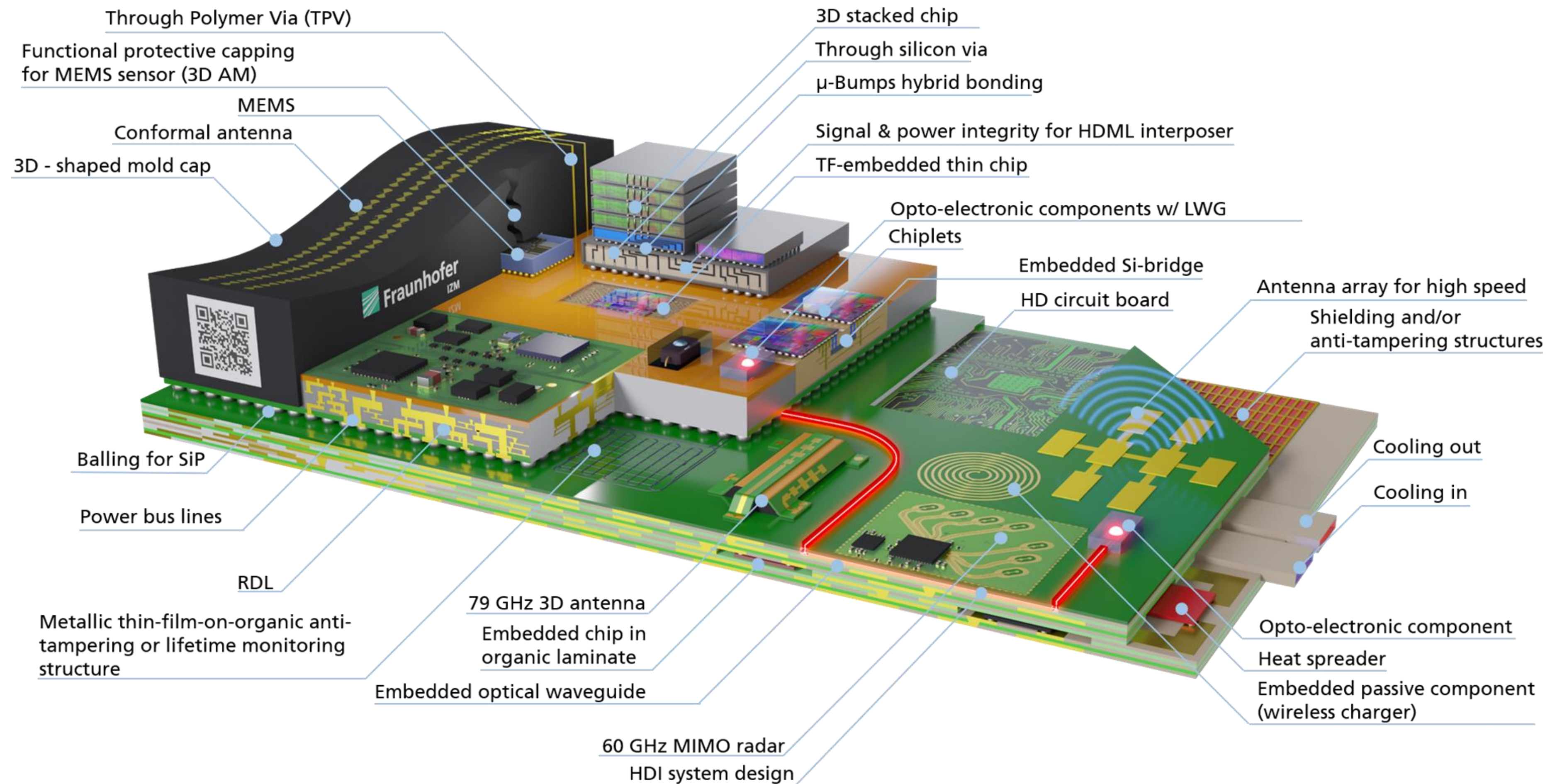
Our Mission at Fraunhofer IZM

Bringing Microelectronics into Application



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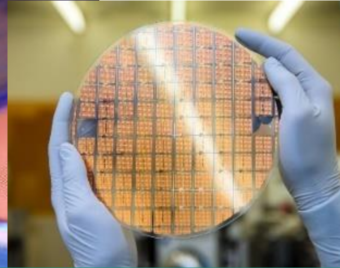
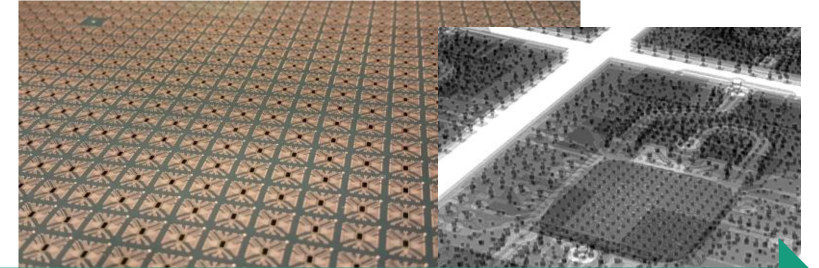
Fraunhofer IZM – Wafer- and Panel-Level Technologies

From Wafer Level System Integration to Panel Level System Integration



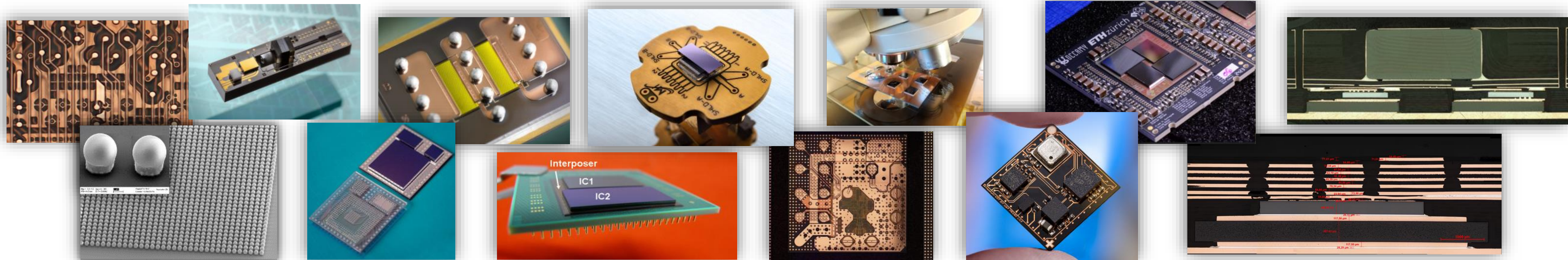


CMOS Feature Sizes 5 nm … >100 nm

WLP Feature Sizes 0.75 µm … >10 µm

PLP Feature Sizes < 5 µm … 100 µm

Wafer Level Packaging (WLP)		Panel Level Packaging (PLP)
Based on thin film materials & equipment	**Technology**	Based on PCB materials & equipment
100mm … up to 300 mm	**Format**	up to 610 x 456 mm²
CMOS – III / V - WBG wafers	**Input**	CMOS - III / V - WBG dies (w/ bumping)
2.5D / 3D integrated systems or system components	**Output**	Packaged / embedded modules



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EU Chips Act: Contribution of the three major RTOs

Pillar 1

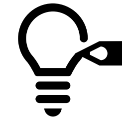
»Chips for Europe Initiative«
Strengthening research, development and innovation

Pillar 2

»Security of Supply«
Support for new types of production facilities and EU foundries

Pillar 3

»Monitoring and Crisis Response«
Coordination mechanism for monitoring the supply of semiconductors



R&D in microelectronics & semiconductors are the basis for technological sovereignty and the industrial future of Europe.

- Creation of a pan-European Pilot Line Facility by major European RTOs in the field: FMD, CEA-leti, imec with VTT, Tyndal, SAL, TNO and more
- Europe is an attractive and reliable location for investments in the production of semiconductor technologies.
- It is important that we talk to the industry about supply chain developments at an early stage so that we can avert possible crises in advance.

FMD Advanced Heterogeneous System Integration (AHSI) Pilot Line

Chiplet Interface Readiness for Heterogeneous Integration

Heterogeneous Integration Platforms (2.5D / 3D)

FMD Demonstrators

Interposer/Bridge
200 mm

Interposer/Bridge
300 mm

Organic/Glass Core Interposer
up to 600mm

Chiplets from external partners (RTOs, IDMs, Foundries,…)

FMD chiplets

- Compute and Memory Integration
- Photonics Integration
- RF Integration
- QMI System Integration
- MEMS Integration

Characterization Test Reliability (CTR)

STCO Approach

FhG IZM TOPICS!

Design Topics:

- Communication Interface IPs
- System Network Architecture
- Thermal / Power Management

CTR Topics:

- KGD Test Access
- In-Line Reliability Test Concepts
- Defect Analysis and Repairability

Integration Topics:

- 3D Stack (TxV, W2W / D2W, …)
- 2.5D Assembly + Overmold
- Bridge / Chiplet / Passives Embedding
- High Density Routing (l/s <5µm)
- E/O Routing (Polymer, SiN, Ag doped glass, …)
- µ-Bump Scaling (pitch <5µm)
- Interface / Assembly Technology Mix
- High Throughput Assembly
- High Accuracy D2W <1µm
- Holistic Process Flow Approach (Chip-Interposer-Board)

Characterization Test Reliability (CTR)

Demonstrators

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Thank you for your attention!

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