# TINKER : ENABLING 3D INTEGRATION AND ADVANCED PACKAGING FOR NEXT LIDAR GENERATION FOR AUTONOMOUS VEHICLE DRIVING

# WELCOME !


## "3rd Innovative Public Research Organization Worldwide" 2012 -2020

Derwent™
A Clarivate Analytics company

Since **1967**

**2,000** people

**Patents:**
- > 3,000 in portfolio
- 40% under license agreement

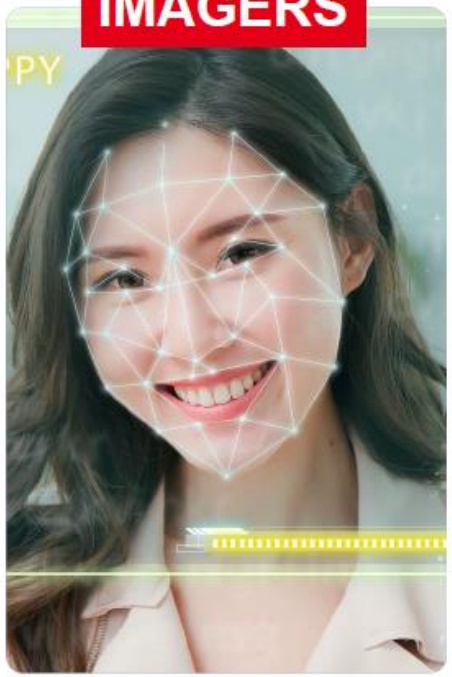
**Startups:**
- 68 created for 20 years (75% in activity)
- 3500 jobs created

**Cleanrooms:**
- 500 state-of-the-art equipment in 200 & 300 m²
- 10 000 square meters cleanroom

**Budget:**
- 315 M€
- 85% from R&D contracts

# PHOTONICS DIVISION

## IMAGERS



## SILICON PHOTONICS

## DISPLAYS

## OPTICAL SENSORS

## PHOTONIC SYSTEMS

**300+ EMPLOYEES**
40 doctoral students and post-docs

**80M€ ANNUAL BUDGET**

**700+ PATENT FAMILIES**
IN PORTFOLIO
*40% licensed*

**DEDICATED TOOLS**
FOR MODELING AND SIMULATION

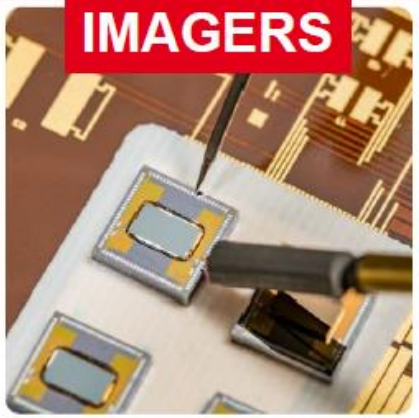
**PHOTONICS CHARACTERIZATION**
FACILITIES

**III-V & II-VI MATERIALS**
ON VERSATILE SUBSTRATE

# PHOTONICS DIVISION High-performance technologies

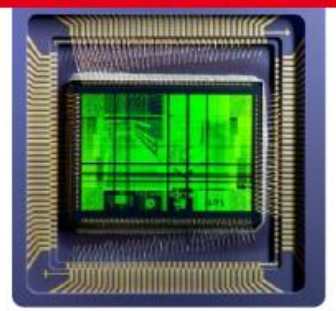
## CMOS IMAGERS

## HYBRID INFRARED IMAGERS



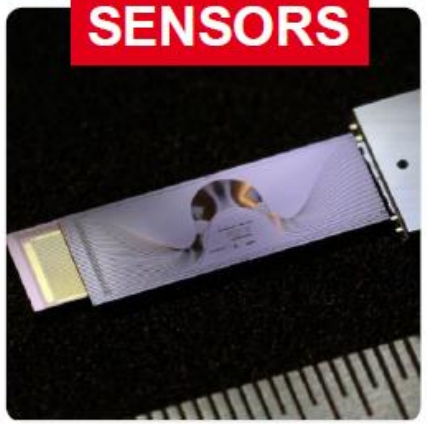
## THERMAL INFRARED IMAGERS

## MICRODISPLAYS

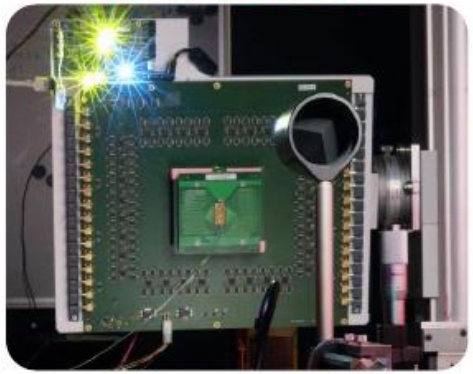


## SILICON PHOTONICS

## ADVANCED OPTICAL SENSORS



## LIDARS



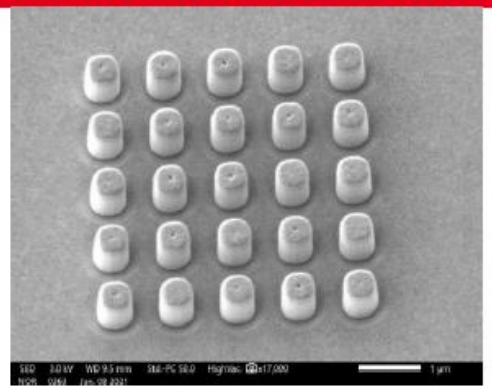
## GAMMA/X IMAGERS

cea

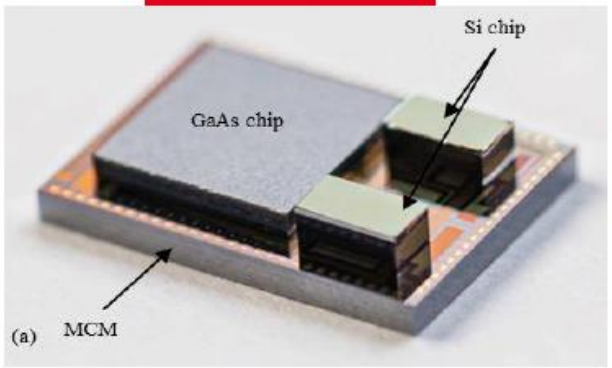
338.7 x 190.5 mm

# PHOTONICS PACKAGING

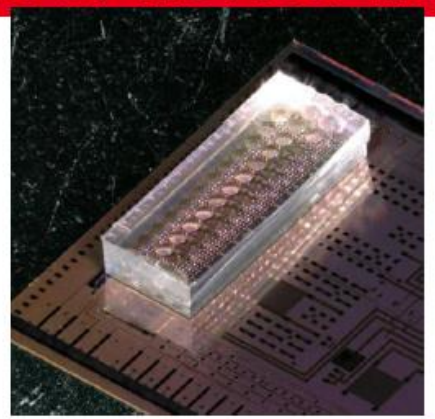
## FINE PITCH INTERCONNECTS



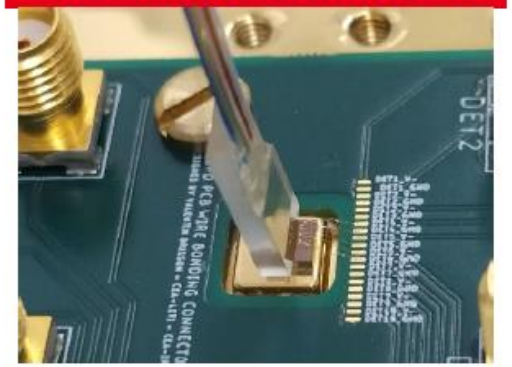
## FLIP CHIP



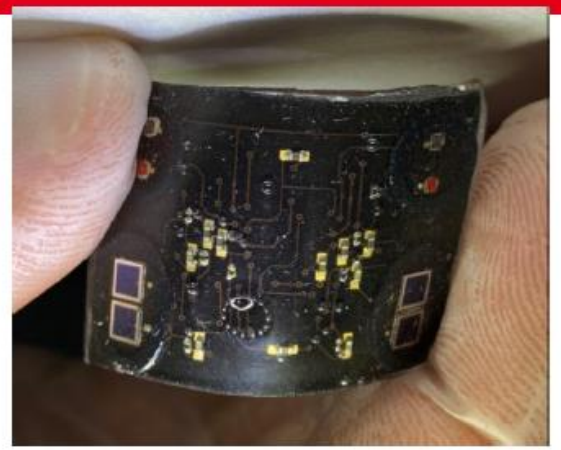

## MICROOPTIC ASSEMBLY



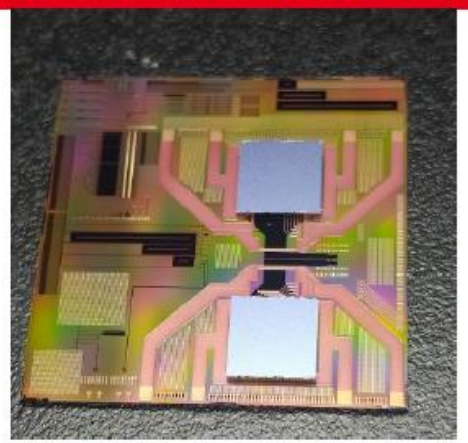
## FIBER ASSEMBLY



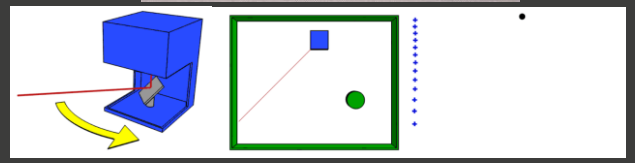
## PHOTONIC SENSORS MINIATURIZATION



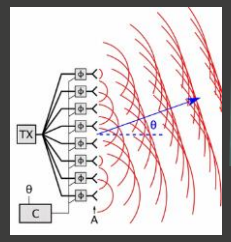
## PHOTONIC INTERPOSERS

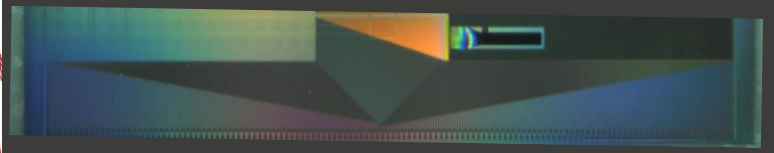


# TINKER LIDAR MOTIVATION

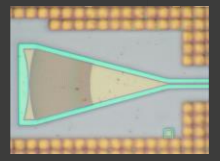
Mechanical steering is huge,
slow and expensive

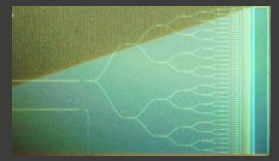


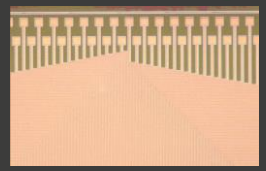



Si wafer level technology based Optical Phase Array (OPA)

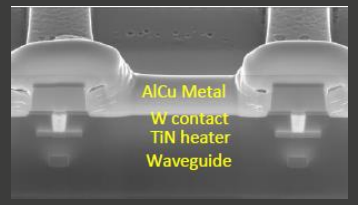

It works ! But …



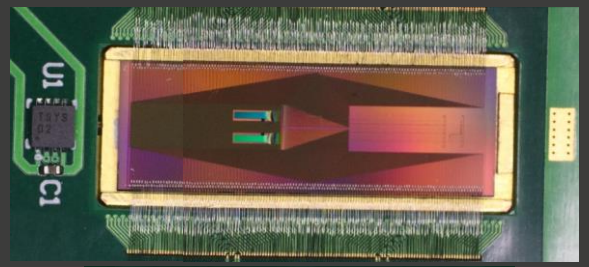




*Si/SiO2 grating couplers and waveguides - Interconnects*




*TiN thermal wavelength shifters*

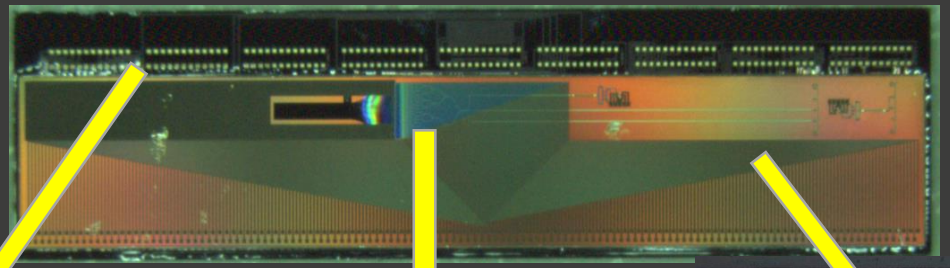


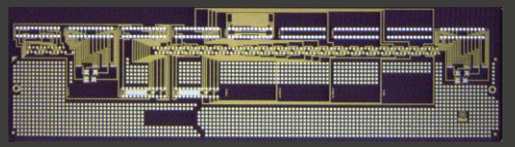

Too many wires for a 256 channels OPA
>1000 channels required for ADAS

TINKER

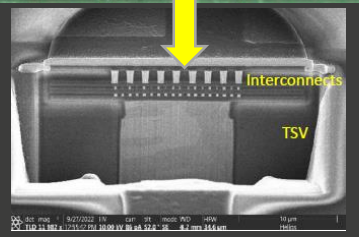
leti
cea tech

3D packaging integration of
Photonic IC on Interposer

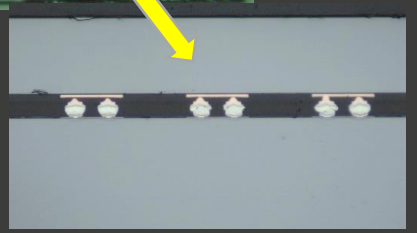




Interposer can contain OPA
+ CMOS drivers & Laser




OPA back side surface for higher
connections density
10x100µm TSVs



High density
Collective Flip chip
20µ Φ Copper pillars

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# Photonic on silicon processing

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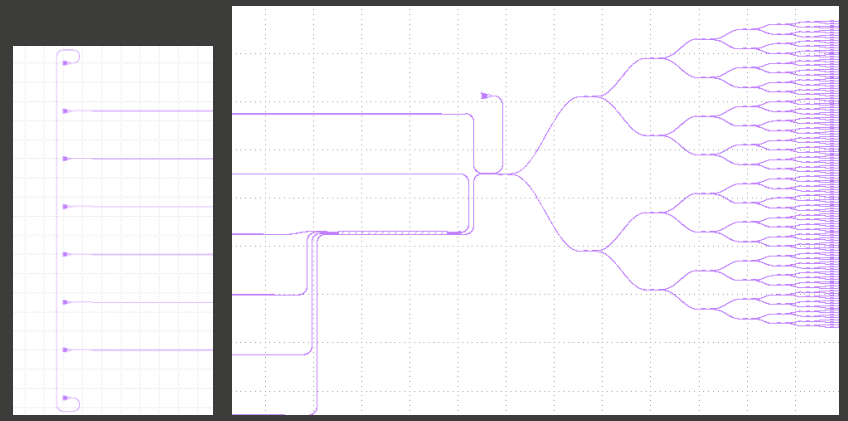
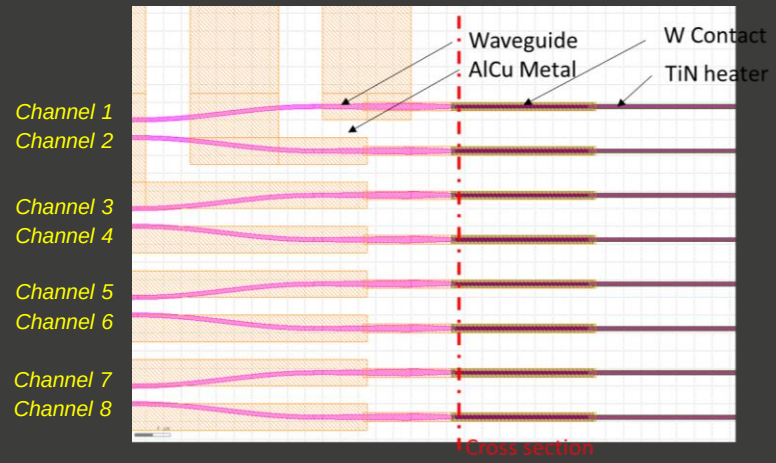
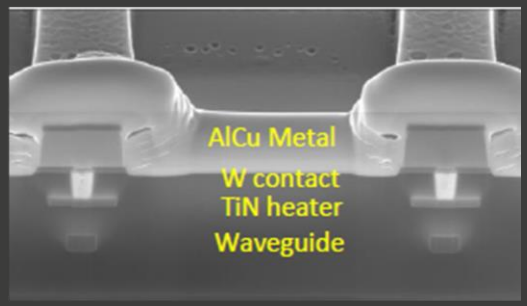
- Photonic processing



Grating couplers

Waveguides & splitters




- *TiN thermal heaters for light pahse shift*
- *W contacts to metallization*
- *Conventionnal AlCu metallization*

Si/$SiO_2$ photonic structure with standard Si technology

Standard Si interconnects features

**Photonic phase processing is compatible with a standard silicon technology platform**

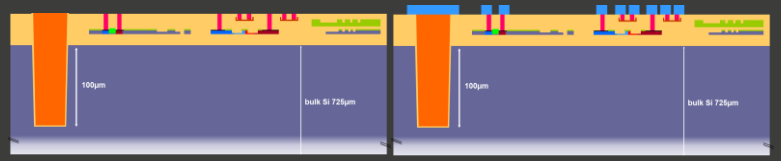
cea leti

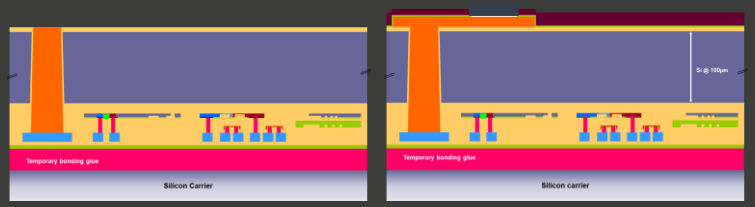
# TSV Technology

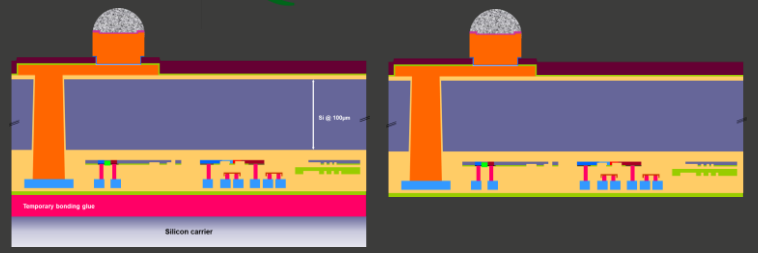
- 2 types of TSV available and developped
  - ✓ Option 1 : Mid process TSV
    - Performed between the contacts and front side metallization
    - ☺ Higher density
    - ☺ Higher performances
    - ☺ Smaller footprint
    - ☹ Die warpage for flip chip
    - Available in IDMs and Foundries
  - ✓ Option 2 : TSV Last
    - Performed after full standard processing
    - ☺ Thicker silicon to reduce die warpage
    - ☺ « easier » processing steps
    - ☹ Larger footprint and lower density
    - Available in OSATs and Foundries
  - ✓ **Both are developped in TINKER**

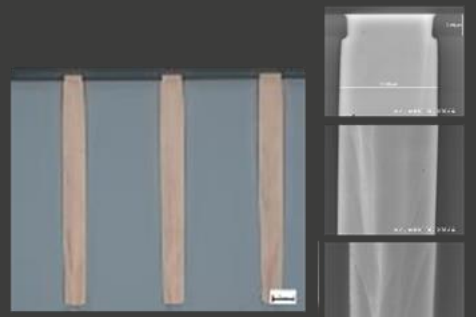
# TSV Technology

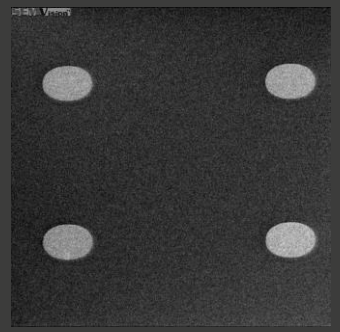
- Mid process TSV

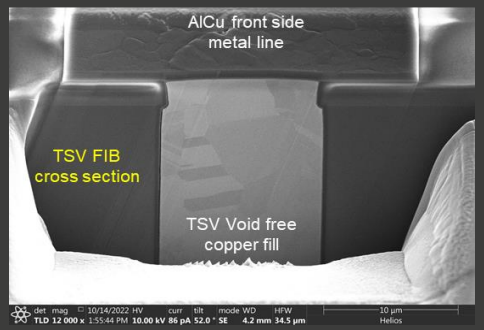


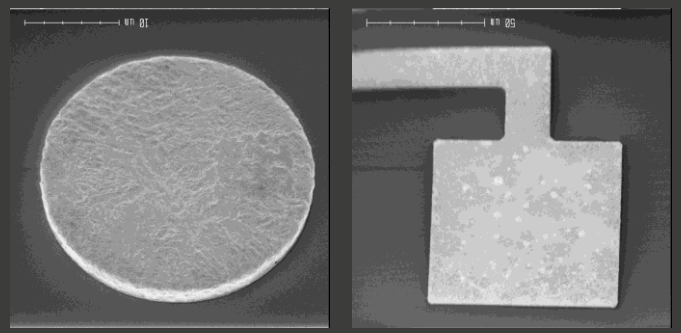



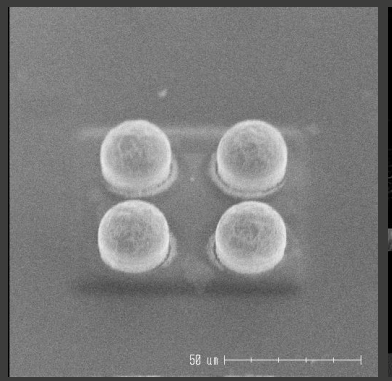



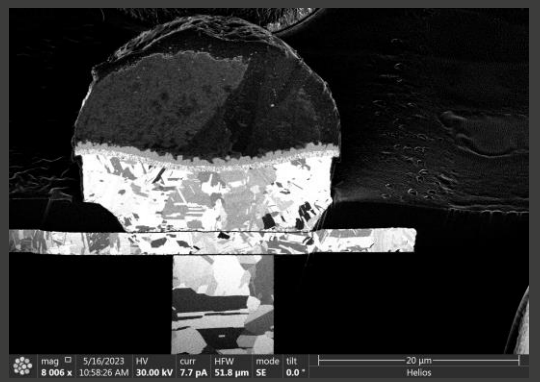











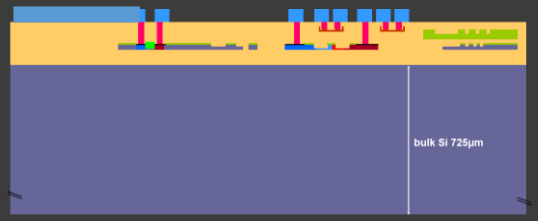
*Φ10 µm mid process TSV processing*
*And further standard metallization*

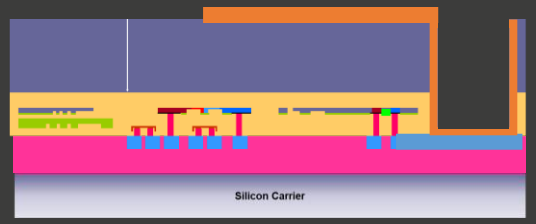
*Back side contact on TSV bottom*
*And RDL back side metal routing*

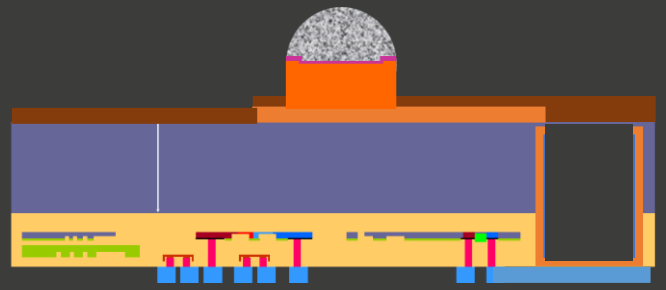
*Φ20 µm SnAg bumps processing*
*And debonding from carrier*

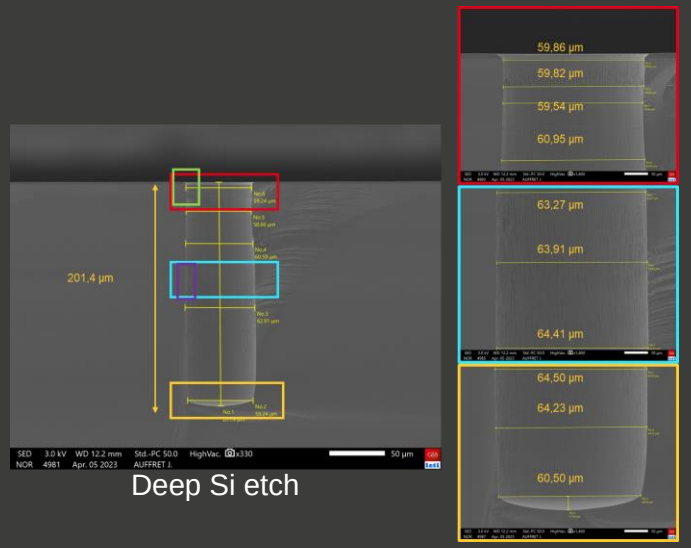
# TSV Technology

- TSV Last (development in progress)

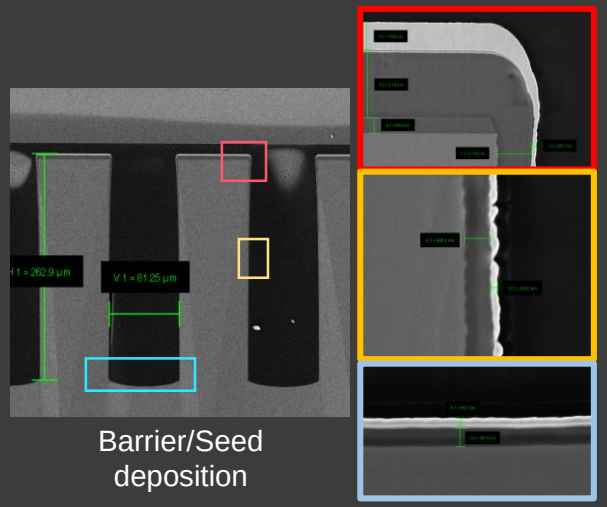


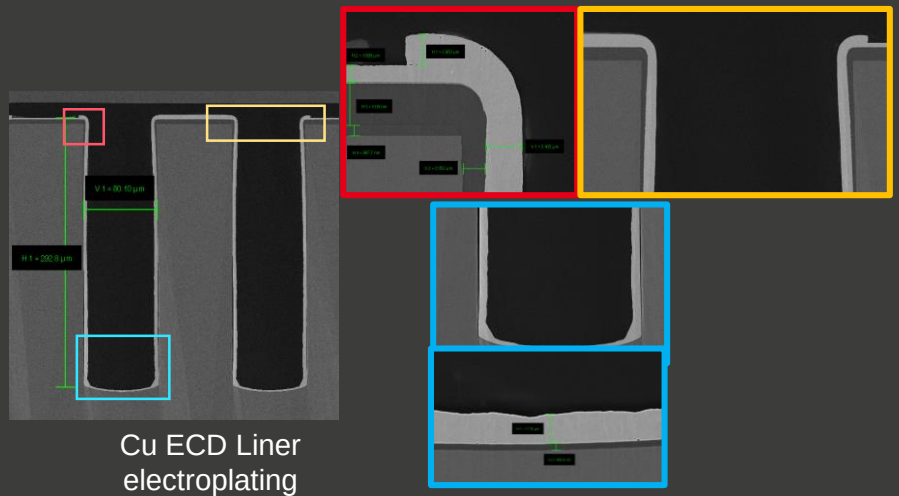






Deep Si etch



Barrier/Seed deposition



Cu ECD Liner electroplating

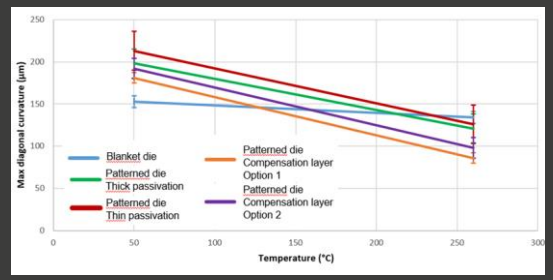
*Φ50 µm TSV Last processing*
*Deep Si etch and isolation*

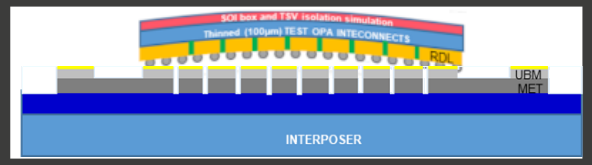
*Φ50 µm TSV Last processing*
*Coper liner metallisation*

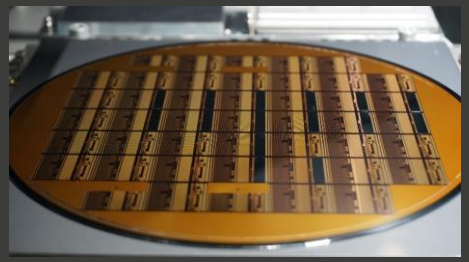
*Φ40 µm SnAg µBumps processing*
*And wafer debonding from carrier*

# TSV Technology

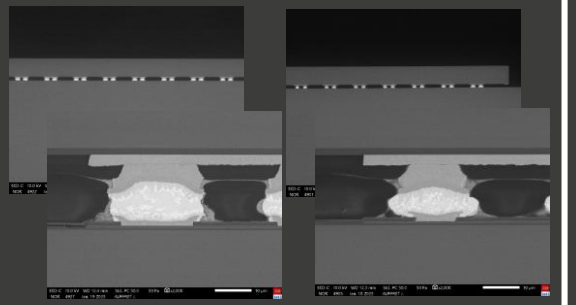
- Flip chip technology
  - ✓ Both Thermocompression (robust for R&D) and Mass reflow (Fast for manufacturing) Die to wafer Flip chip technologies developped in Tinker
  - ✓ eg : Mid process TSV



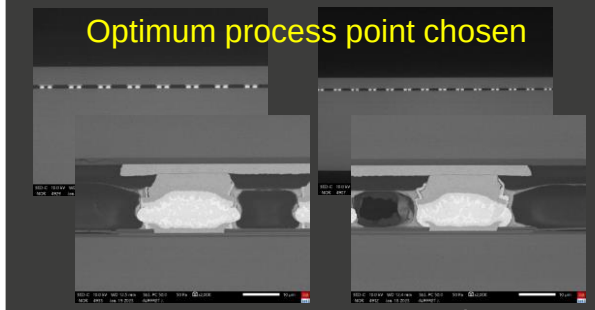
*180 °C*



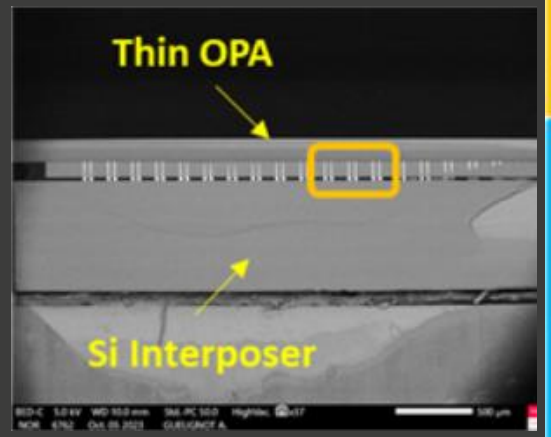
*Center* *Edge*

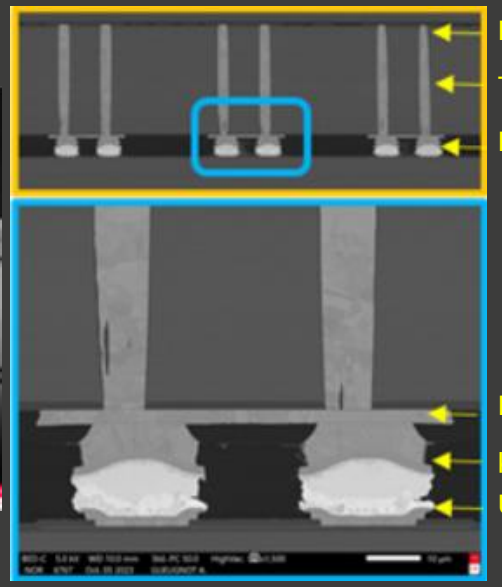
*200 °C*

Optimum process point chosen



*Center* *Edge*




*Mass reflow option*

# Conclusion

- Tinker LiDAR Platform proposes a Photonic 3D Integration and packaging solution to meet the LiDAR requirements for ADAS
- Photonic on Silicon, TSV and Fine pitch flip chip are integrated and final integration is in the testing phase

- This technology is proposed on CEA-LETI Silicon Platform through the Tinker project
- Participation to the EPIC technology meeting allows Tinker consortium as well as CEA-LETI to disseminate the work carried on in this H2020 european project