QUANTIFI PHOTONICS™

FUTURE OF PHOTONIC TEST

PIC MANUFACTURING TESTING

EPIC ECOC 2023

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TESTING NEEDS TO CHANGE

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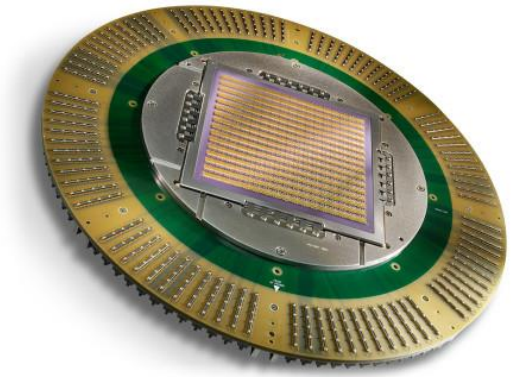
e
electron

Wafer Testing/Sort involving electrons uses load boards with 100-1000's of contacts with instrumentation built into the load boards.

Instruments can be calibrated with standards on-site with little setup or dismantling.



- Throughput is extremely HIGH
- COST OF TEST per known good die is LOW

γ
photon

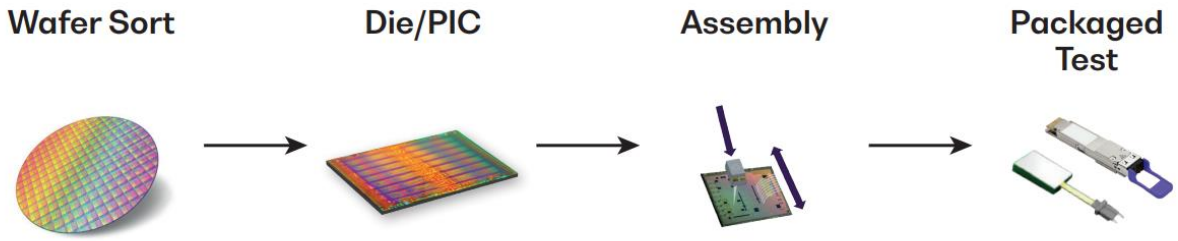
Wafer Testing/Sort involving photons uses precision alignment with at best a fiber ribbon with a dozen channels.

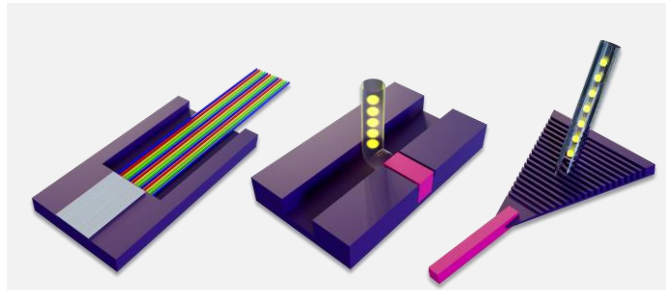
Setup needs to be dismantled to enable instrument calibration.

- Throughput is LOW
- COST OF TEST per known good die is HIGH

CHALLENGES

Optical wafers, dies, subassemblies and devices are evolving very quickly.



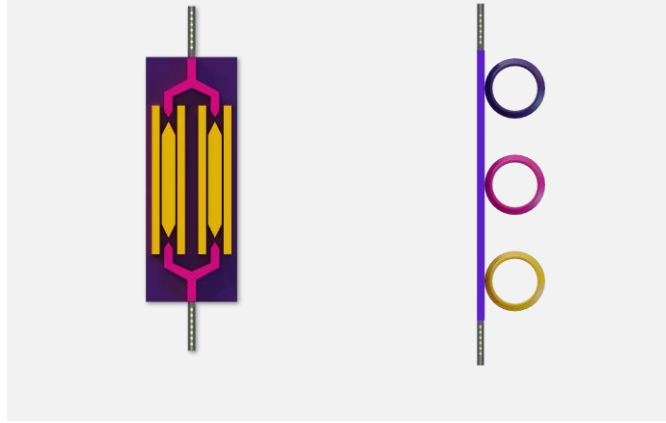


No Standardization from Design, to Foundry, to OSAT to CM:

- Everything is custom and efforts are repeated within all companies
- Difficult and very expensive to scale

Good reasons why T&M isn't keeping up:

- Volumes are still very low, making the business case for purpose fit test solutions very tenuous and risky.
- Current photonic test instruments are being shoehorned in.
- Resulting a wide gap between the desired throughput.



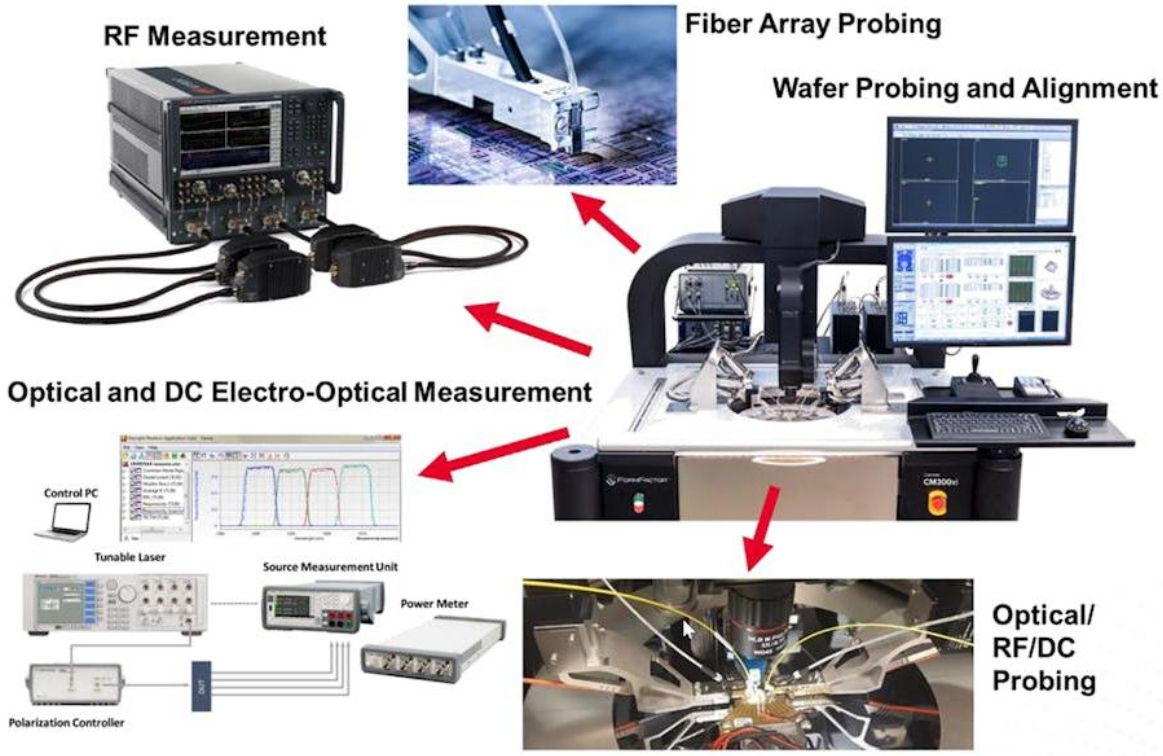
PHOTONIC TESTING TODAY

Mainly **SERIAL** testing, at most parallel wavelengths on single fiber or a fiber ribbon at wafer sort.

Small number of channels with heavy reliance on large switch matrixes to access instruments.

SLOW to sort, even slower for parametric tuning.

At RF test, Network Analyzers and Sampling Oscilloscope are prohibitively **LARGE** and **EXPENSIVE**. These two end up dictating the extent of parallel testing that is possible.



SOURCE: Keysight and FormFactor

TESTING NEEDS TOMORROW

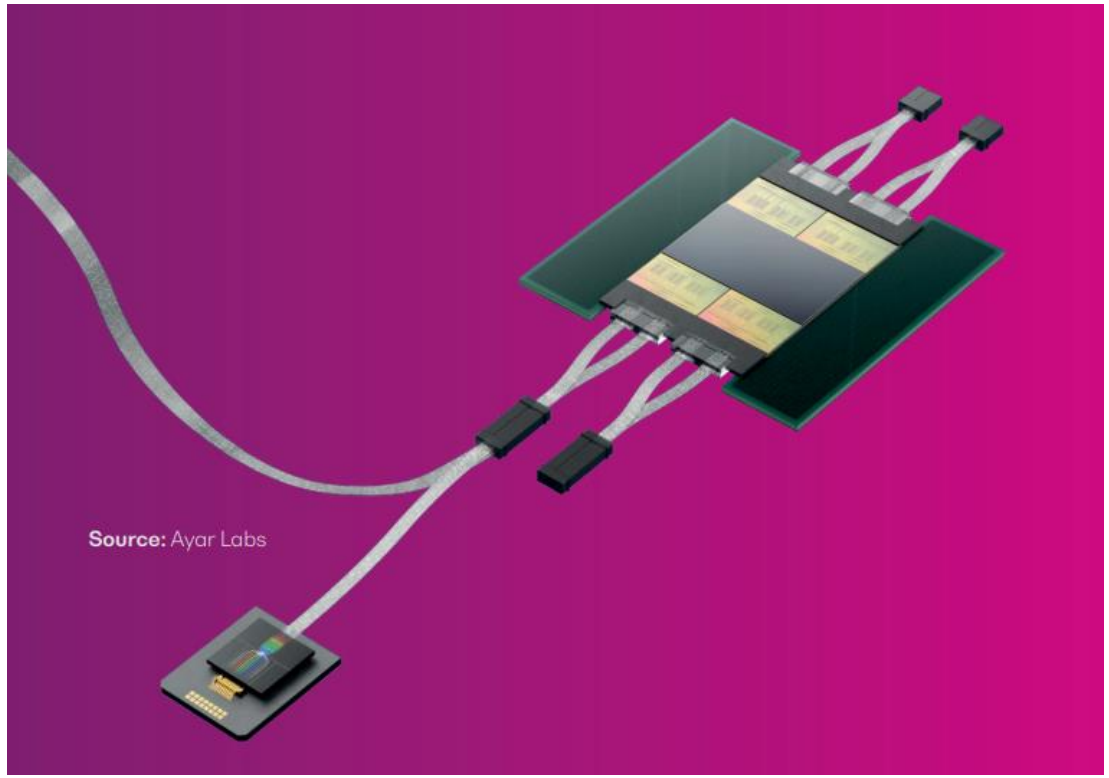
In limited test today:

Chiplets with 8x8=64 channels.

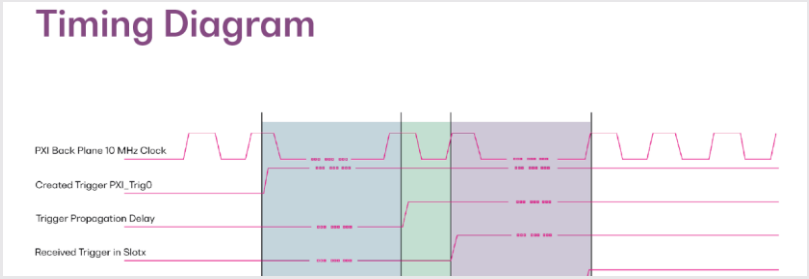
Co-packaged devices with 8x8x8= 512 channels.

Devices with **>1024 CHANNELS** are in planning.

1. Parallel devices needs **PARALLEL TEST** solutions.
2. **DECREASE COST** of scopes or remove need for Eye Diagram testing.
3. **DECREASE SIZE** and cost of Network Analyzer.
4. **OPTIMIZE TEST FLOWS** that decrease reliance on software events preferably in a standards defined ATE.



HOW DO WE GET THERE?

SOLUTIONS	OUTCOME
1. Instrument density   288ch Power Meter	- More instruments closer to DUT - Enabling parallel testing
2. Hardware triggering 	- Less idle time - Better instrument utilization - Lower test time
3. Updated Remote Procedure Call: gRPC	- Less development time - Less idle time with push/pull - Lower test time

HOW DO WE GET THERE? (CONTINUED)

SOLUTIONS	OUTCOME
4. Decrease cost of ownership and footprint of Sampling Scopes and Network Analyzer/LCA	- More channel in smaller footprint - Enable parallel testing - Lower cost of test
5. Introduce service ports into instruments Service ports for in-situ calibration 	- In-situ calibration - Less down time - Less mistakes - Decrease spare instruments

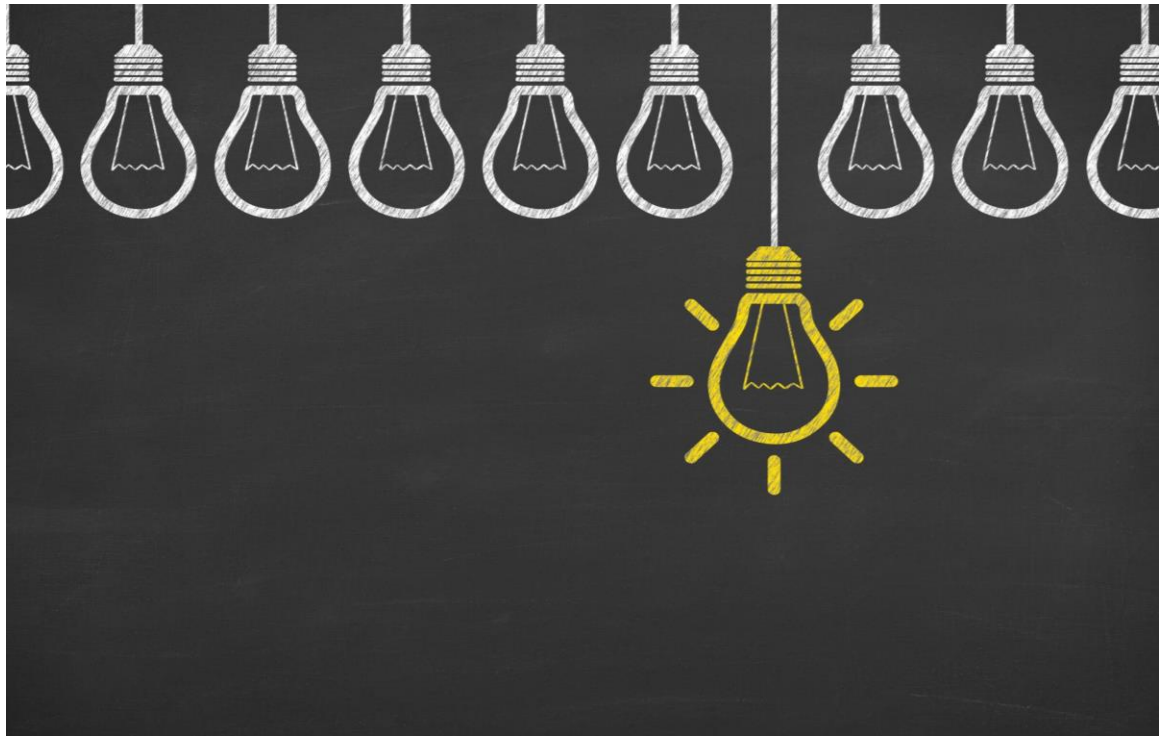
INDUSTRY LED SOLUTIONS

1. Photonics equivalent to load boards?

   Solve optical alignment that can scale

2. Ecosystem adoption of standards for T&M platforms and remote interface.

   E.G. PXIE / gRPC.



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