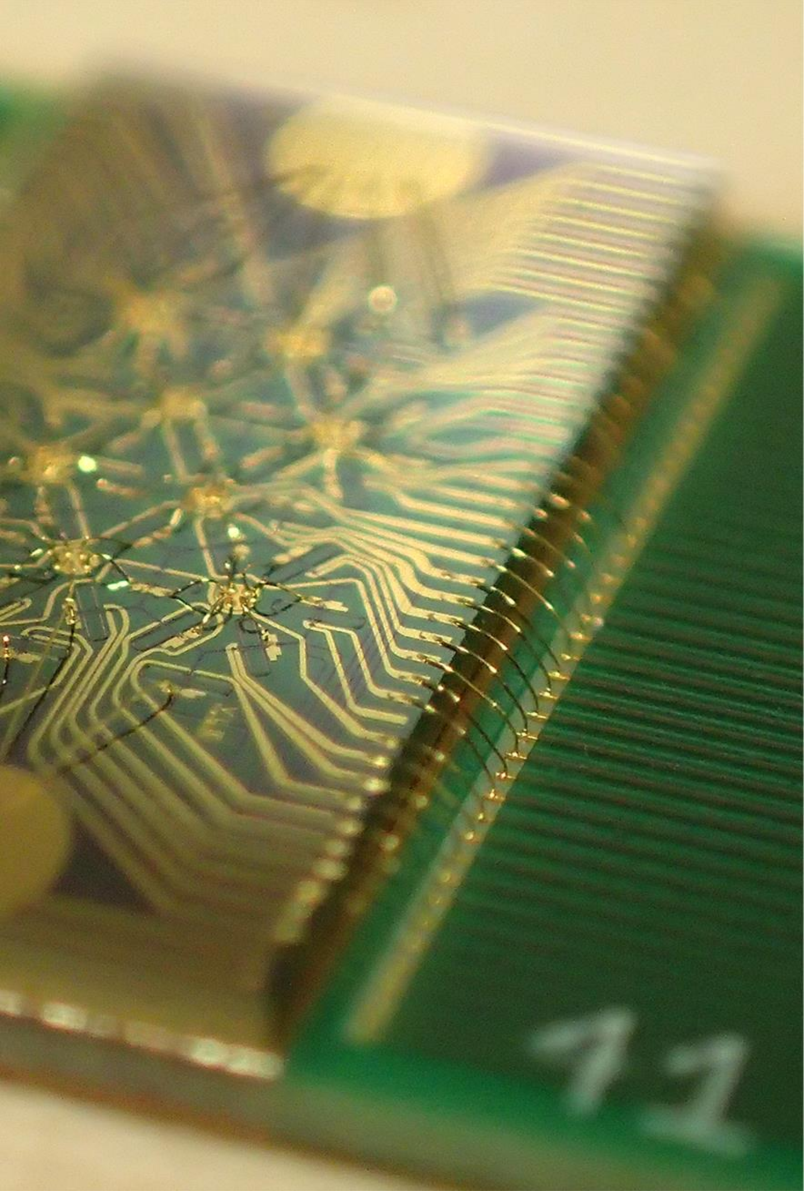


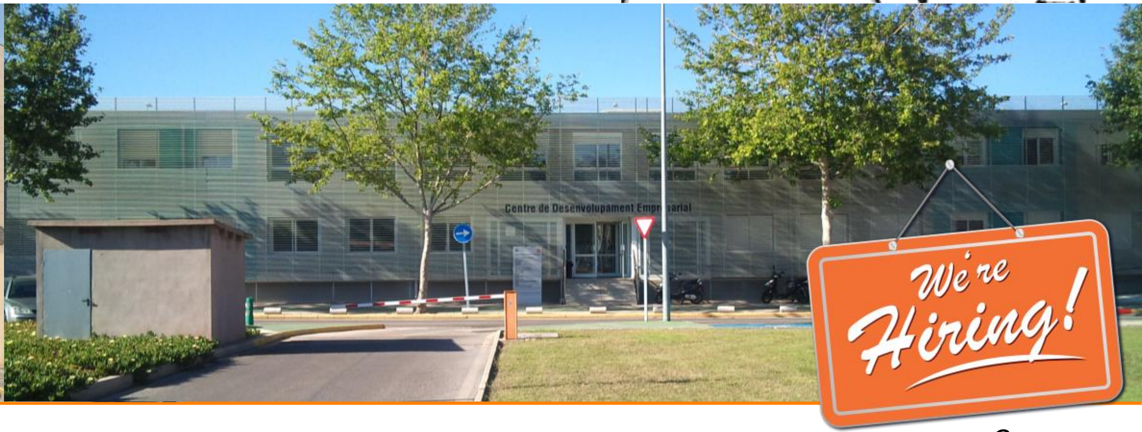
4th October 2023

EPIC TechWatch:

Scaling up the photonic testing back-end

About us

- VLC Photonics offers Photonic Integrated Circuit (PIC) engineering services, focused on design and testing.
- Company founded in 2011.
- Offices and clean-room labs in Valencia Technological Campus (Spain).
- 25 members of extensive academic and industrial experience, and keep hiring.
- Part of Hitachi High-Tech group since 2020.



About us (II)

Hitachi High-Tech Corporation

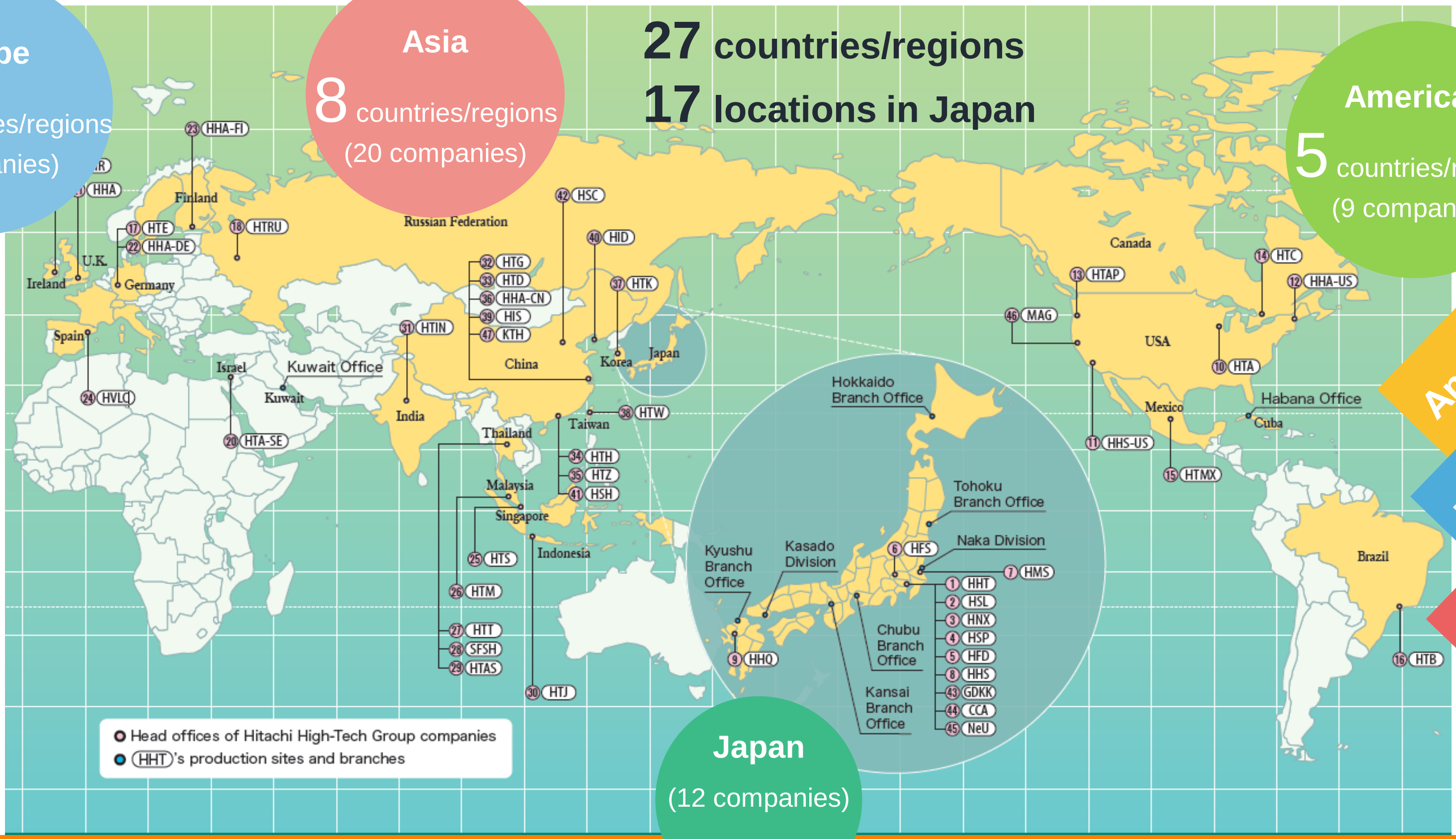
27 countries/regions
17 locations in Japan

Europe
11 countries/regions
(7 companies)

Asia
8 countries/regions
(20 companies)

Americas
5 countries/regions
(9 companies)

Japan
(12 companies)



Analytical & Medical Solutions

Nano-Technology Solutions

Industrial Solutions

Provision of PIC solutions

HHT optical components supply

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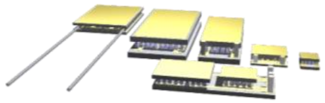
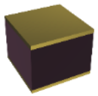
Optical Lens

Thermo Electric Cooler



Thermistor



Ceramic Package

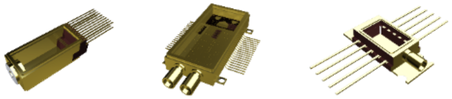
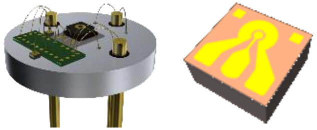
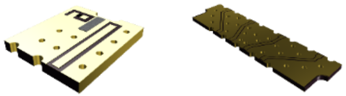


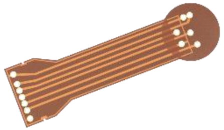
Photo Diode



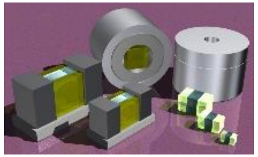
Ceramic Submount

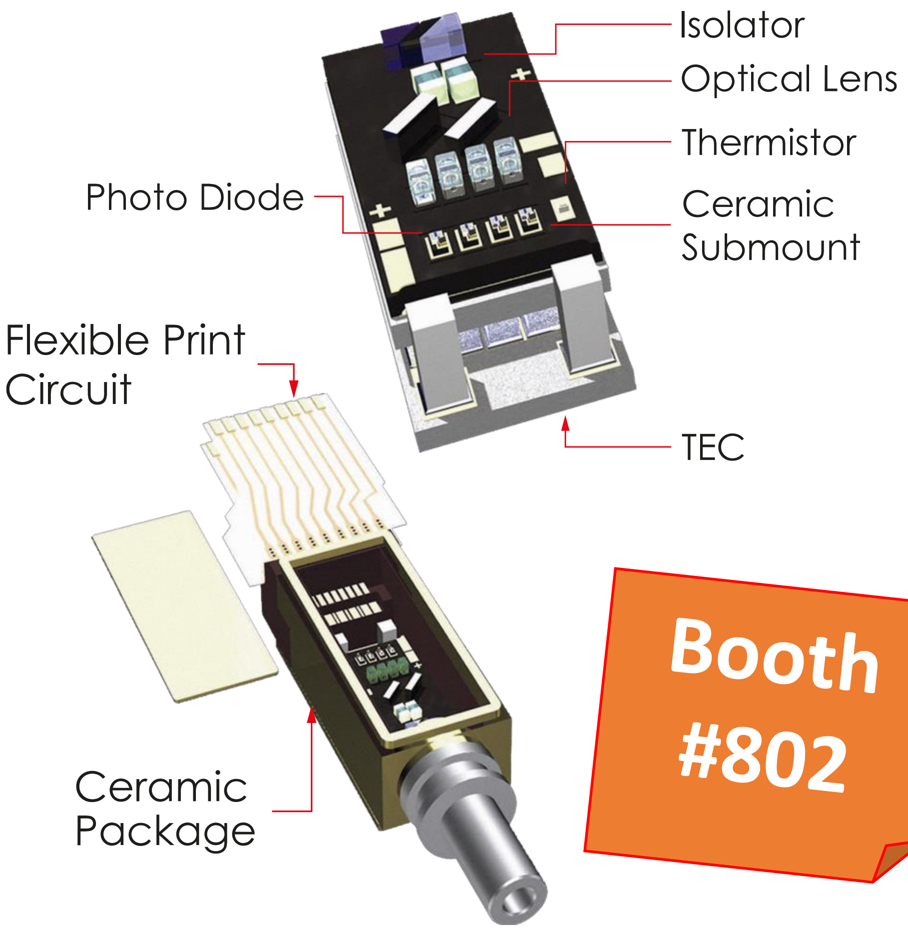


Flexible Print Circuit



Isolator

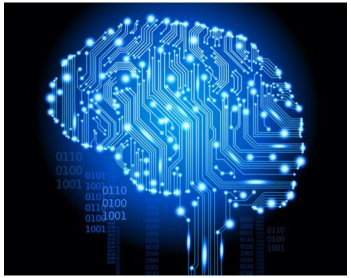


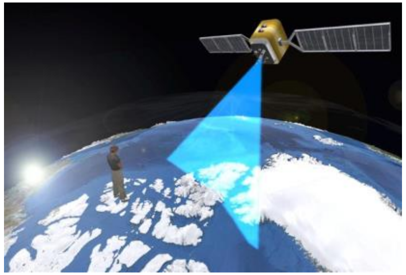


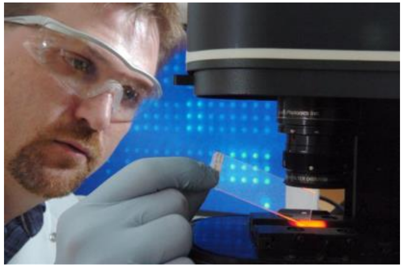
Booth #802

PIC application markets






Communications

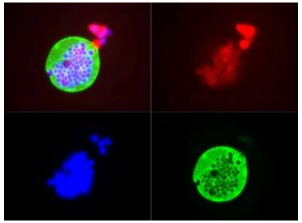
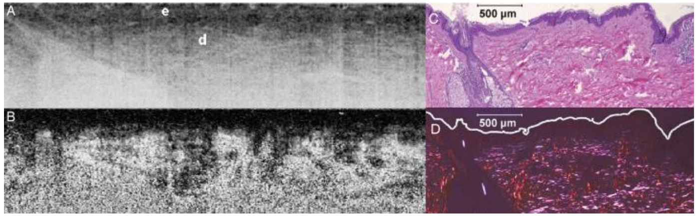
Computing & AI

Quantum

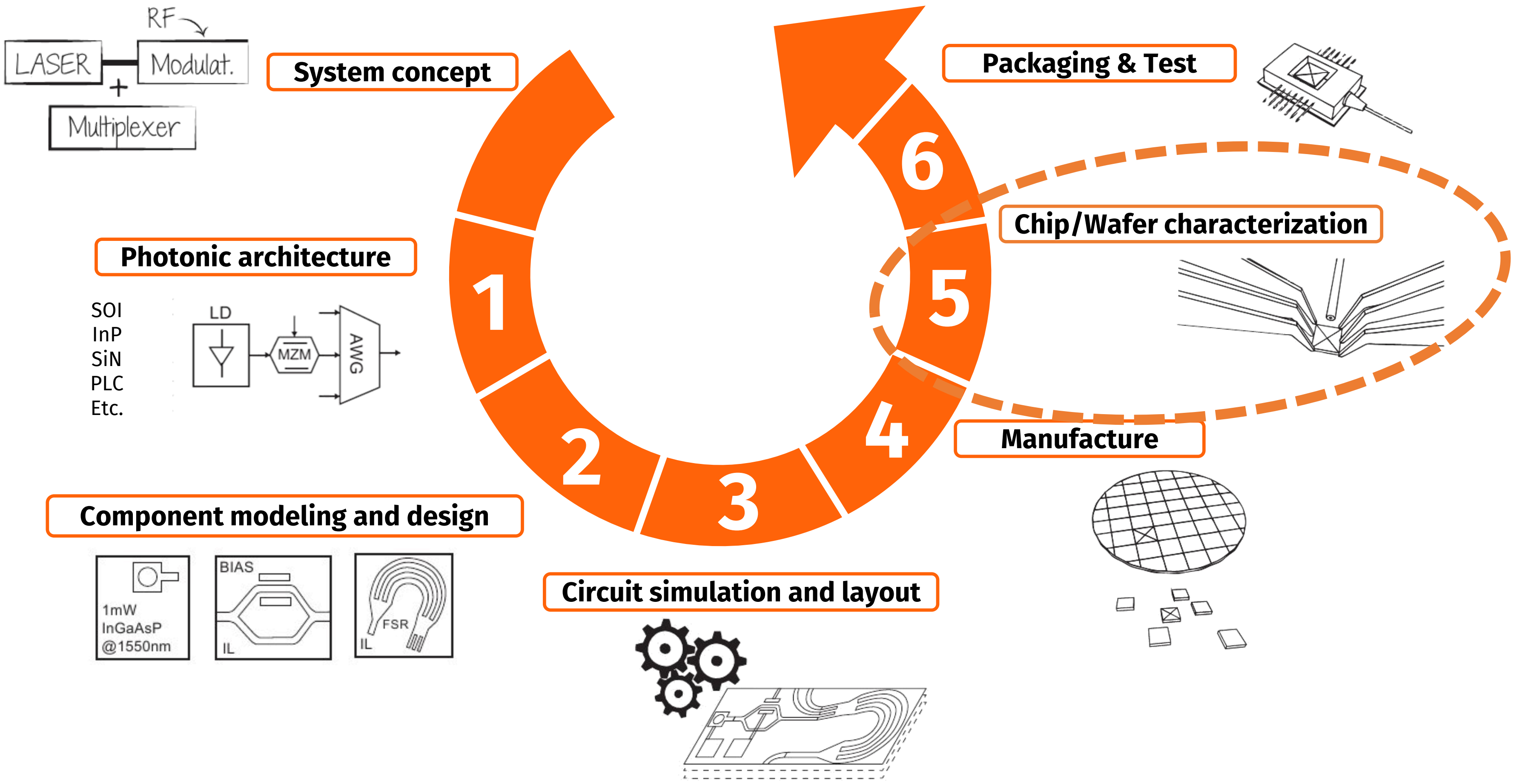
Lidar

Biosensing



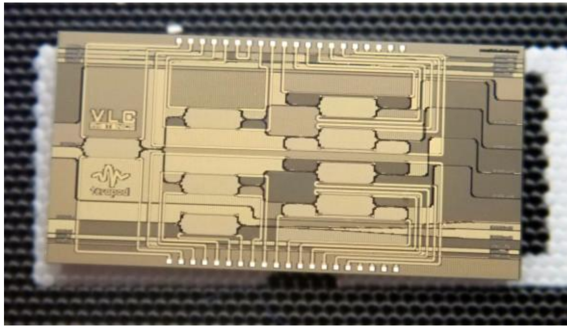




PIC development cycle



Characterization and test needs

- **It is still critical to do extensive component / circuit characterization when validating PIC designs in engineering.**
  - To validate fabrication process and its tolerances through sensitivity analysis (specially needed in photonics).
  - To confirm the intended layout functionality, and feedback the designs for statistical modelling.
  - To sort out known good dies (KGD) and provide feedback on foundry yield, for accelerating ramp up.

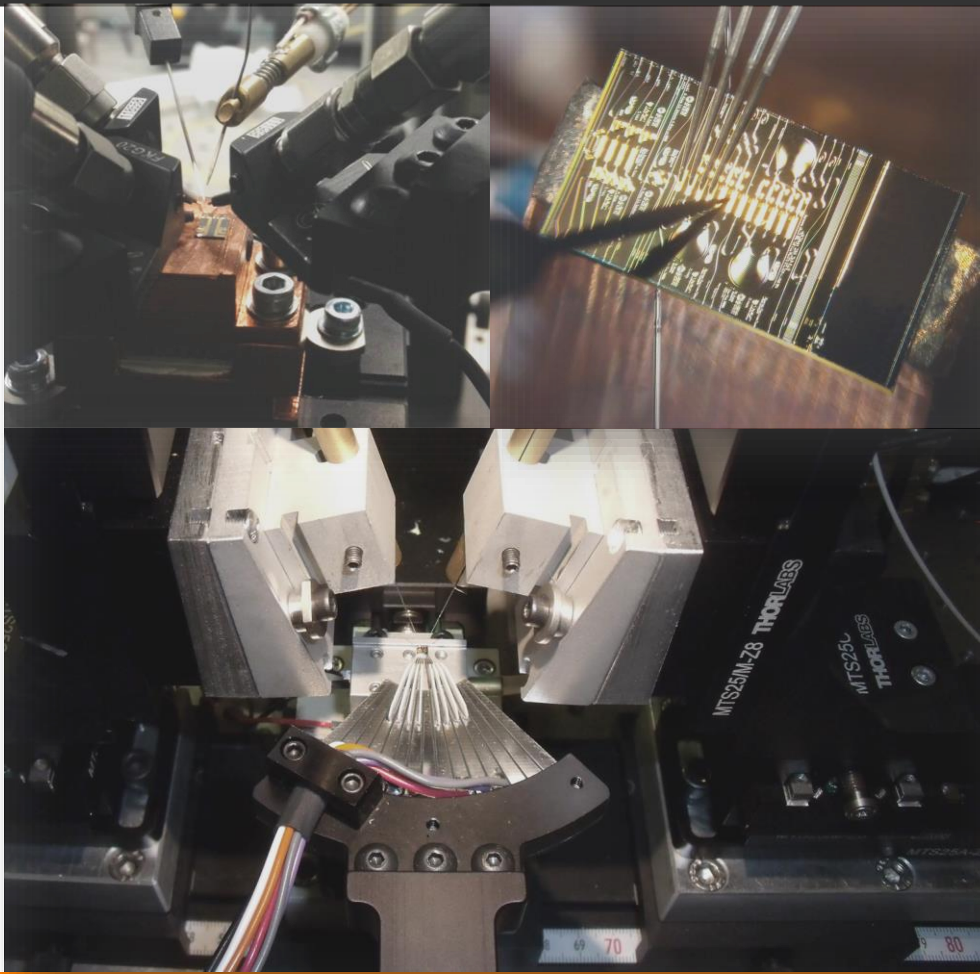


- **When moving to PIC volume production, scalability becomes an issue:**
  - Functional circuit testing is still required beyond fab metrology and PCM.
  - Need fast and low cost Wafer/KGD sorting/binning before packaging.
  - Significant CAPEX for parallelization, engineering and setup time required.

HORIZON 2020 InPULSE

Advantages of outsourcing the photonic back-end

- **Infrastructure investment:**
  - Clean-room lab
  - Opto-electronic probing stations
  - High-end instrumentation
  - Redundancy and consumable stocking
  - Maintenance for 24/7 operations
  - Quality certifications & calibrations
- **Engineering expertise:**
  - Photonics
  - Automation
  - Big data processing and analysis
- **Timing:**
  - Procurement
  - Installation and configuration
  - Hiring and training



Characterization & Testing facilities

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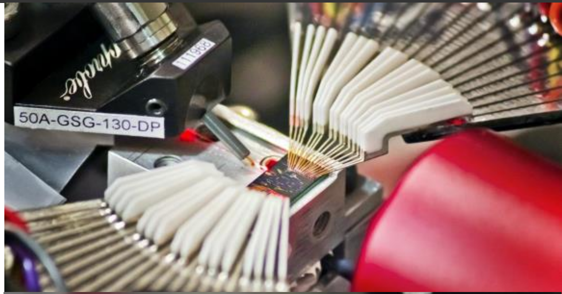
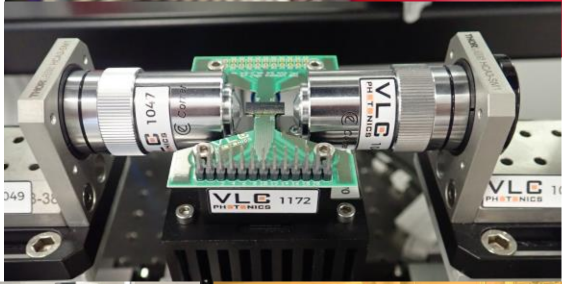
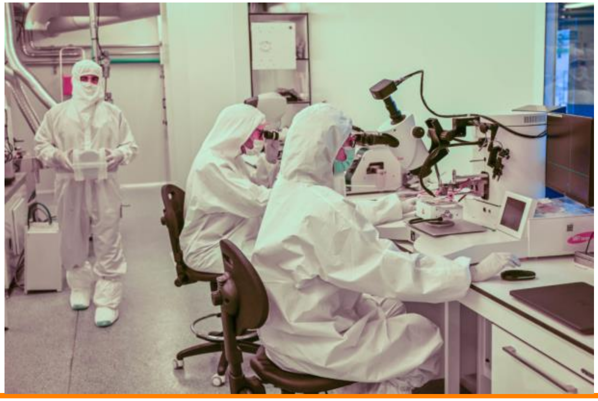
Two clean room labs (ISO class 6 and 8) with:

- Optical microscopes & SEM for detailed visual inspection
- Optical (vertical and edge light coupling) and electrical probing:
    - 5 semi-automated bare die characterization setups
    - 1 manual electrical wafer tester
    - 2 fully automated opto-electronic wafer testers
- Electrical measurement instrumentation for DC and RF signal testing up to 110 GHz and optical equipment to work from visible (400 nm) to mid-IR (up to 5 µm).
- Test assembly:
    - 1 manual & 1 automated wire-bonder
    - 1 flip-chip tool





Design for testing

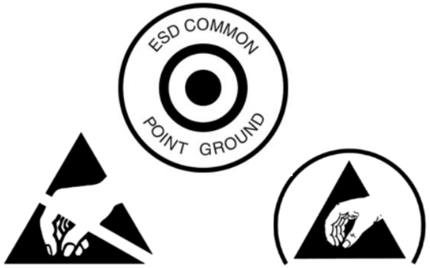
- **Testing starts at the layout phase, prior to fabrication:**
  - **<u>Test structures:</u>**
    - Component DoE's
    - Built-in test circuits
  - **<u>Placement:</u>**
    - Electrical and optical port positions
    - Port pitch
- **Assembly Design Kits (ADKs)**
  - Available for some foundries and EDA software frameworks.
  - Compatible with test and packaging requirements

Measurement planning and execution

- **Detailed test plan:**
  - Measurement campaign specification
  - Failure mode & Effects (FMEA) / root cause analysis (RCA)
  - Agile methodology

- **Quality system in place:**
  - ISO 9001 certified and audited annually
  - Well documented processes and work instructions
  - Calibrated instruments and measurements
  - Redundant parts in stock

- **ESD safe operations:**
  - Controlled environment humidity and ionization
  - Compliant tools, furniture and instruments
  - Custom jigs, chucks and holders
  - Verified grounding, constant monitoring system
  - Extensive ESD training for personnel



Visual inspection

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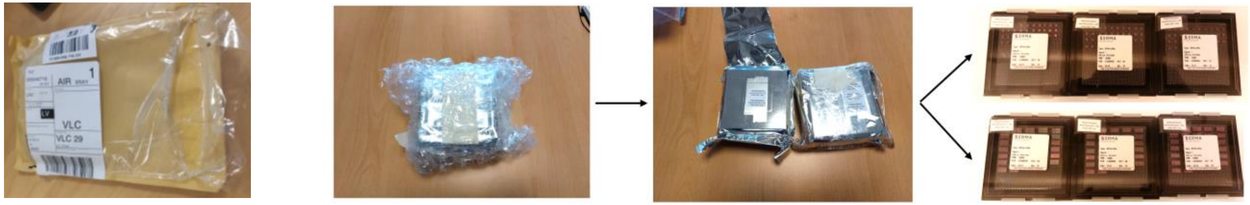
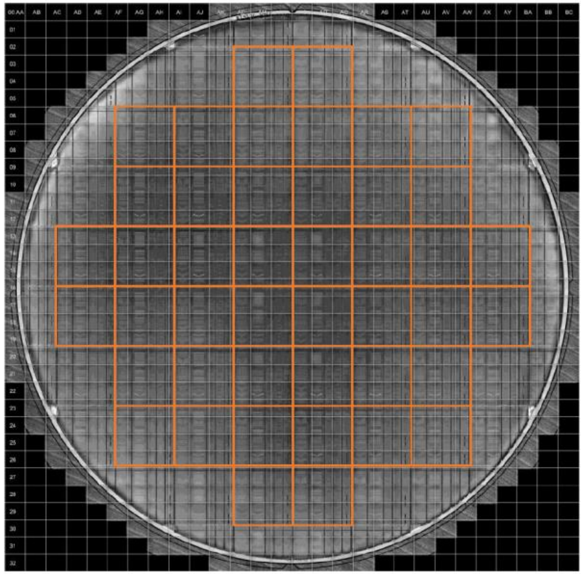
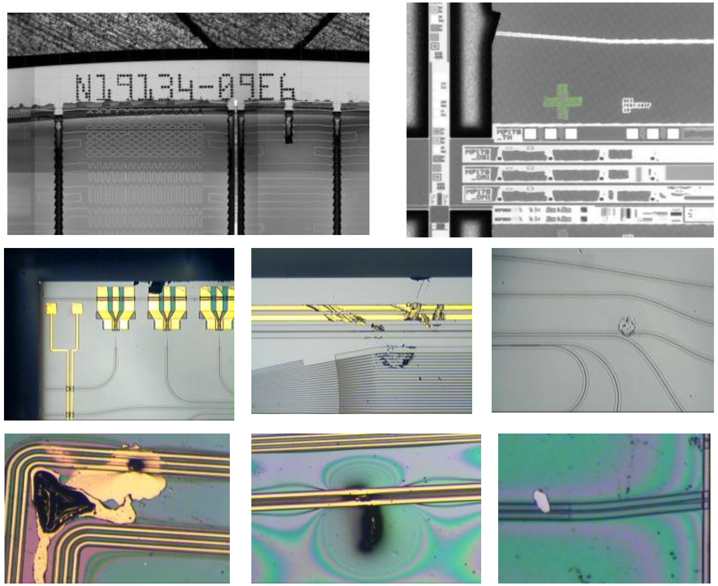


Parts inspection:

- Full tracking
- Inventorying, reception reporting
- Safe storage
- Confidentiality preserved



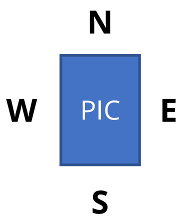


Chip/wafer automated inspection:

- ID and fiducial recognition
- Epitaxy issues
- Litho & etching tolerances
- Defective metallization
- Damaged structures
- Dirt and resin leftovers
- Surface & side scratches

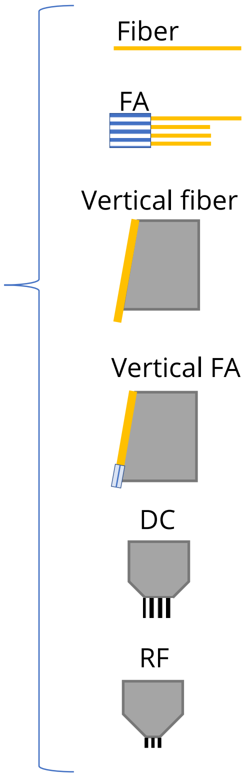
Probing

- Optical probing usually happens in E/W sides of the PIC.
  - Alignment tolerances 1-2 orders of magnitude stricter than in electrical probing!
- The electrical probes should ideally be placed in N/S sides of the PIC.
  - Number of electrical ports constantly increasing!



Setup side	Yes/No	Probing element
N	✓	DC / RF
S	✓	DC / RF
E	✓	Vertical fiber, Vertical FA, Fiber, FA
W	✓	Vertical fiber, Vertical FA, Fiber, FA

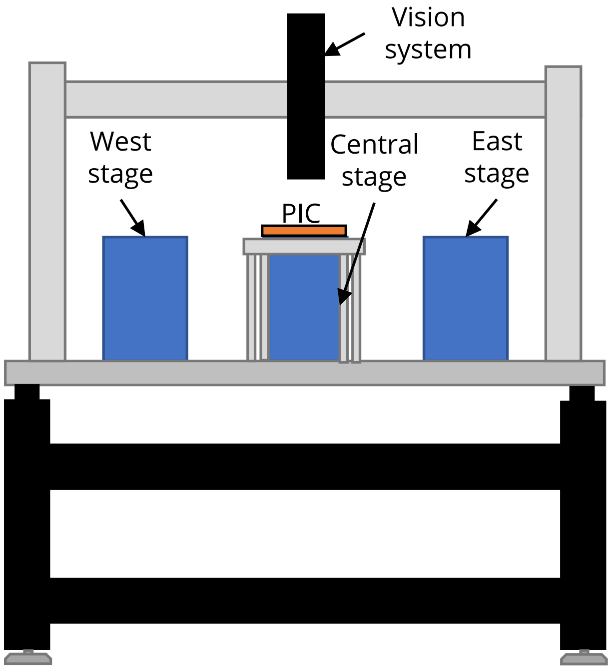
Probing elements



Optical probing	
Number of fibers	1 - many
Fiber pitch	127 µm / 250 µm
Type of fiber	SMF / PMF / Specialty

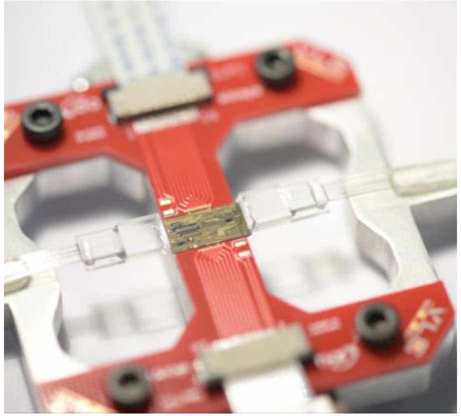
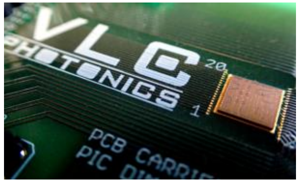
Electrical probing	
Type of probe	DC / RF
Number of needles	2 - many
Needle distribution	GSG, GSGSG, DC+GSGSG+DC
Needle pitch (µm)	100 µm / 150 µm
Bandwidth (GHz)	Up to 110 GHz

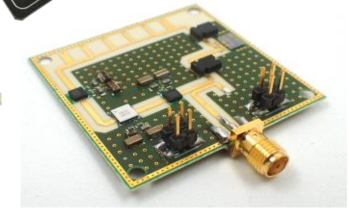
Die-level photonic probing



Available for purchase

- Typical configuration in an optical table with manual or piezoelectric positioners for the electrical and optical probes.
- Vision system can be used for edge coupling (top image) and for vertical coupling (tilted view).
- Not scalable and poor repeatability, but usually good enough for R&D and prototyping.
- Class 100k (ISO 8) clean room or even room air ok.
- PIC test assemblies can help on speeding up the measurement.

Automated probing and testing

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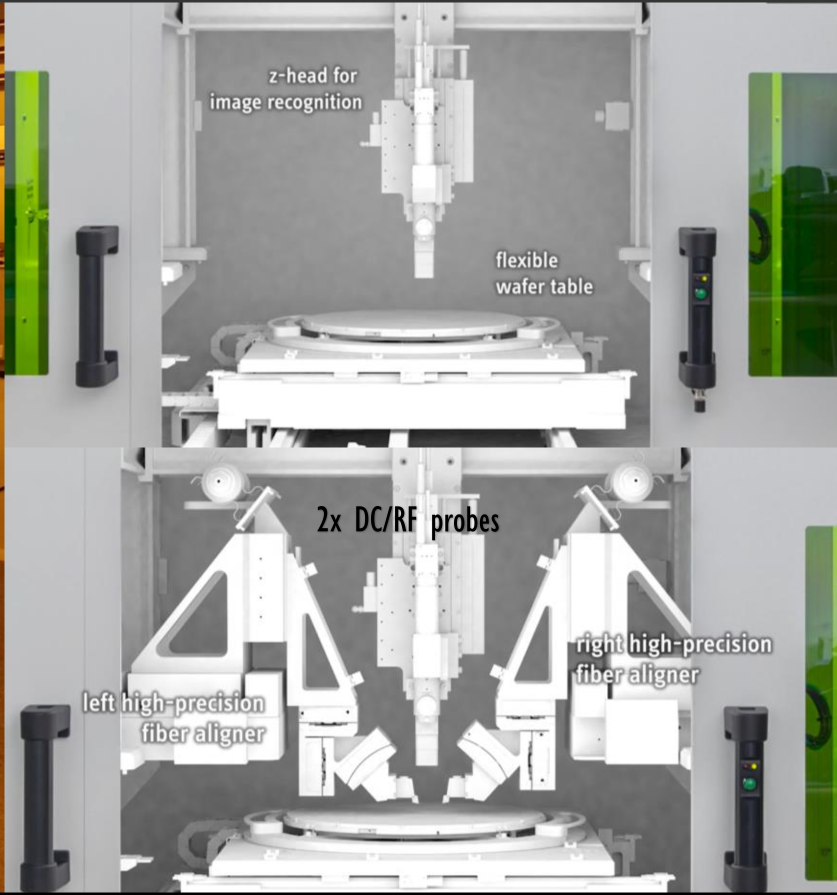

Full production enclosure wafer-level testers (up to 12’’) in class 6 clean room

Automated probing and testing (II)

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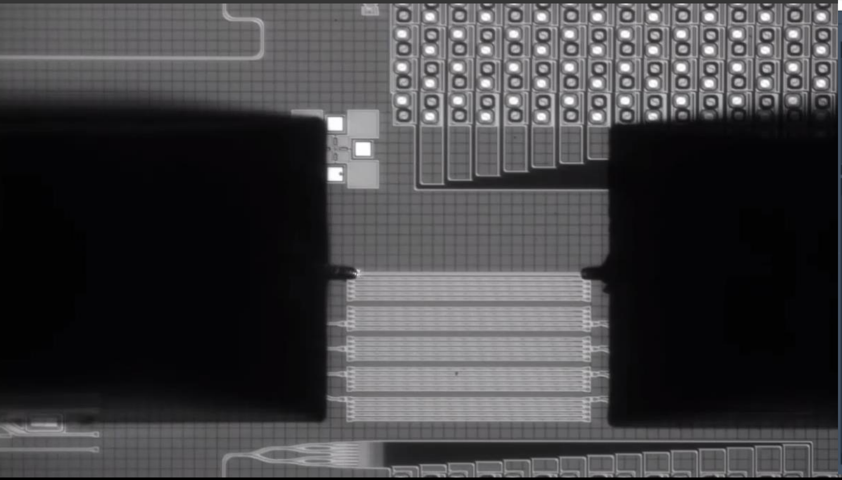
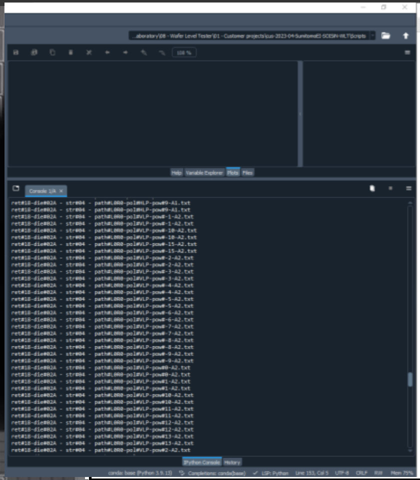
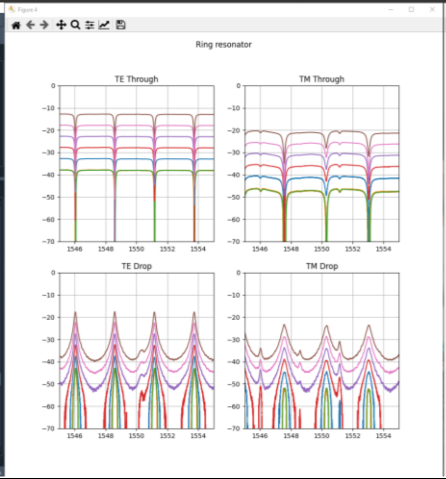
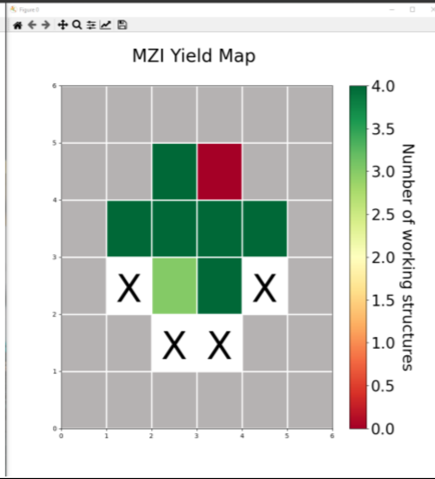


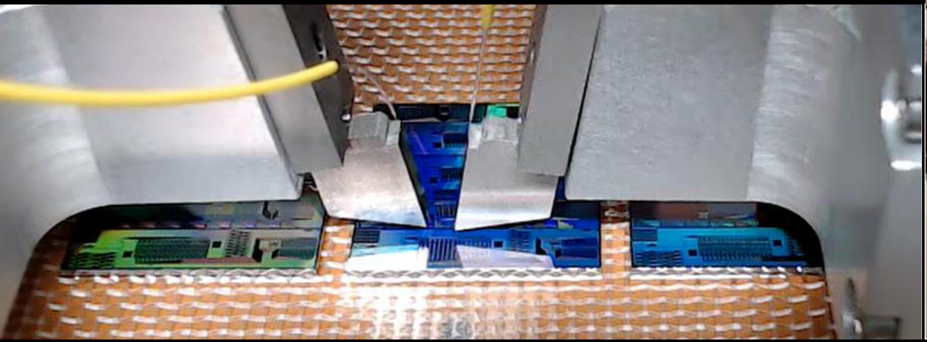






< 4s optical alignment, < 0.1 dB repeatability

Fully automated data collection and processing

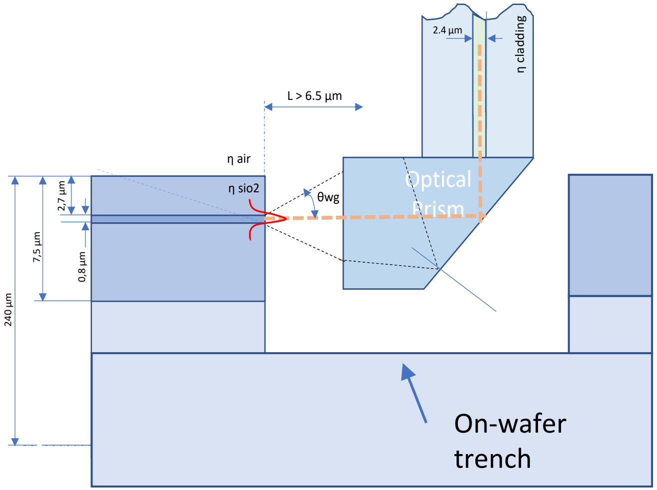


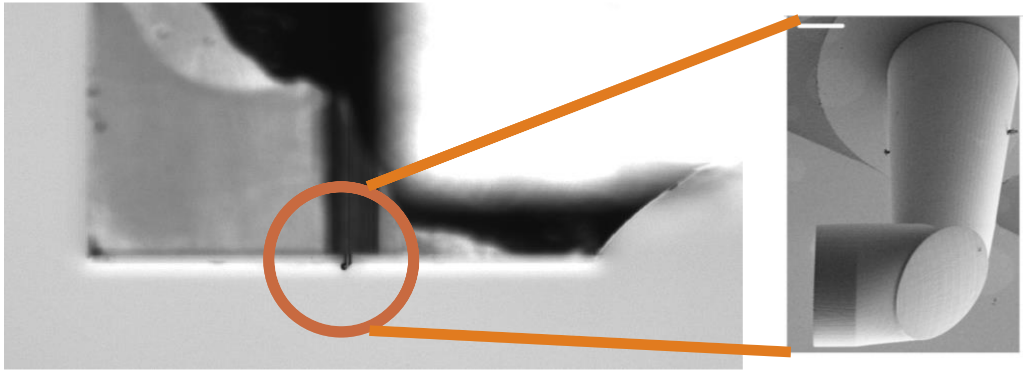
Die and bar level testing possible

Test setup ready for OSAT scale-up

Optical edge coupling at wafer-level

- Edge-coupling wafer access through deep-etch trenches or v-grooves.
- Several types of custom optical probes (single channel and multi-channel)
- Adaptable Mode Field Diameter (2.3 – 10.4 um)



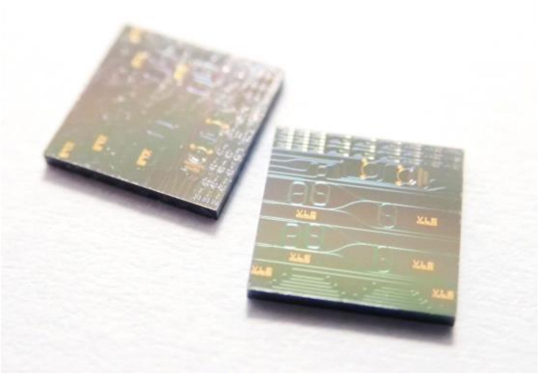


Measurement

Passive components

- Examples: splitters, combiners, filters, reflectors, etc.
- Parameters to measure: insertion loss, coupling loss, excess loss, spectrum, polarization dependency, cross-talk, extinction ratio, etc.

Active components



- Examples:
  - P-i-n, APDs, SPADs
  - DFB, DBR, VCSELs, PCSELs, hybrid, tunable lasers, SOAs
  - Mach-Zehnder, ring, & electro-absorption modulators, switches
- Parameters to measure: Optical power spectrum, integrated power, voltage-current curve, extinction ratio, scattering matrix (S-parameters), temperature dependence, etc.

Other non-photonic components

- Examples: electronics, RF devices, MEMS, micro-lenses etc.

High-speed is key

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Examples of previous projects:

DUT	Structures	Measurements
Six 6” wafers, >300 dies	>5k	~50k
Two 8” wafers, >1800 dies	>14.5k	~58k
>50 dies	>140	>31k

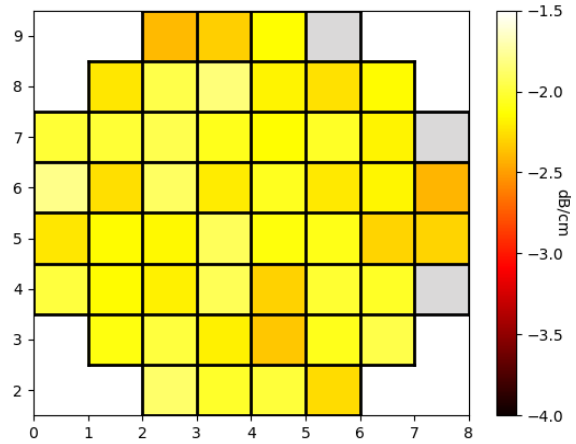
Example times

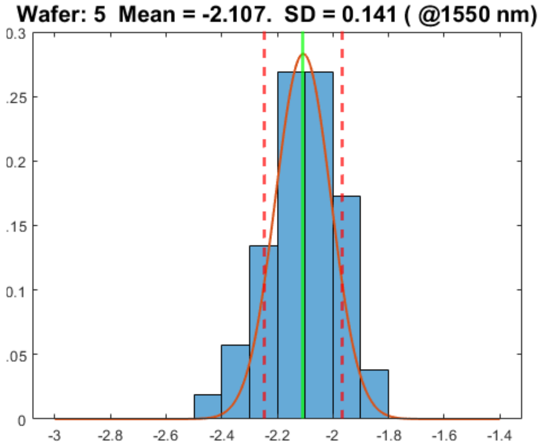
Probing time: 4 s
Measurement time: 1 s
measurements: 50k

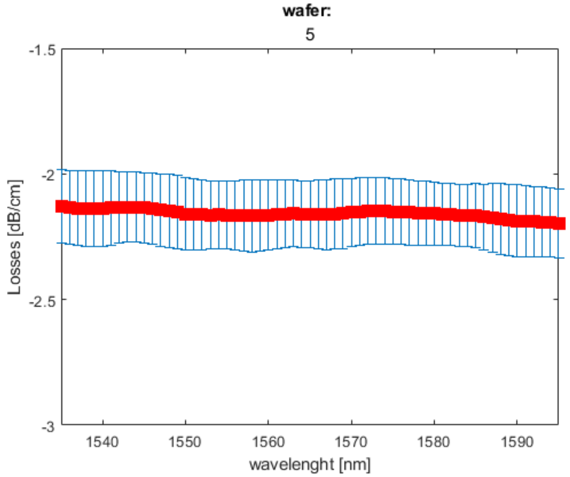
TOTAL TIME = ~3 days

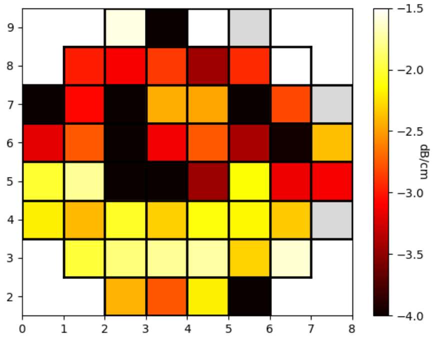
- Fast probing and trace acquisition times are essential when scaling up.
- Smart characterization plan and execution is a must for insightful but time-practical test campaign.

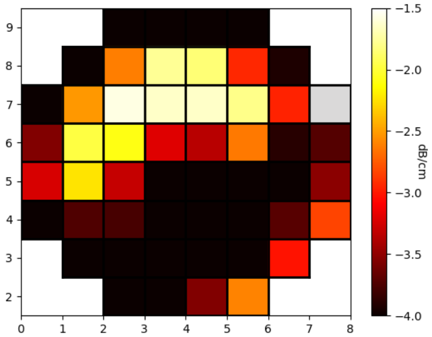
Process control and yield analysis

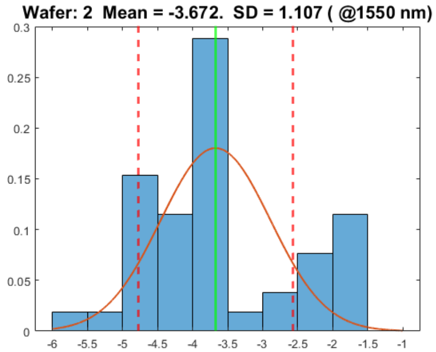


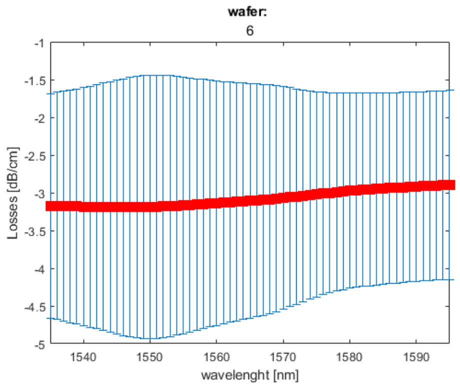






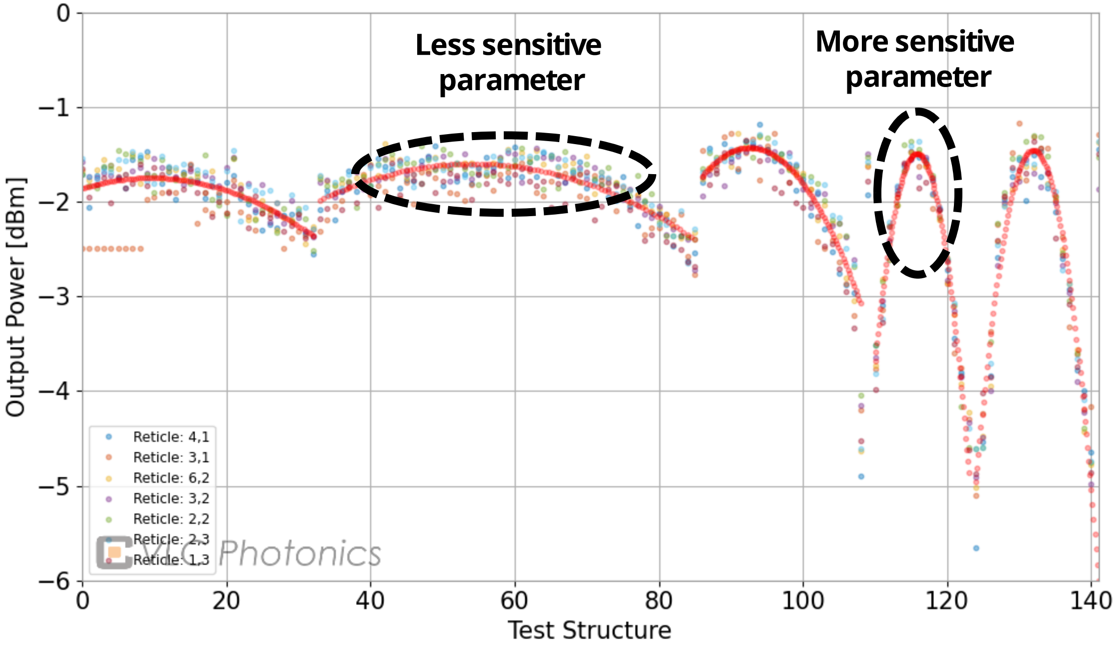






Component sensitivity analysis

Example of design parameters sweep over 140 test structures in 7 reticles



- Repeatability of bare die measurements with manual alignment is poor (>0.5 dB).
- WLT ensures that alignment and trace acquisition are done automatically with minimal variations (mechanical, thermal etc.)

RF testing key for next-gen datacom PICs

- **Lightwave Component Analysers (LCA’s) for parametric testing of devices like high speed modulators in transceivers.**
    - Up to 110 GHz turn-key test system for optical RX and TX
    - Suitable for die and wafer level testing
    - Return to zero and nonreturn-to-zero (RZ / NRZ) and pulse amplitude modulation (PAM) formats
    - S-parameter testing over the full 1260 nm to 1620 nm range

PIC testing trainings

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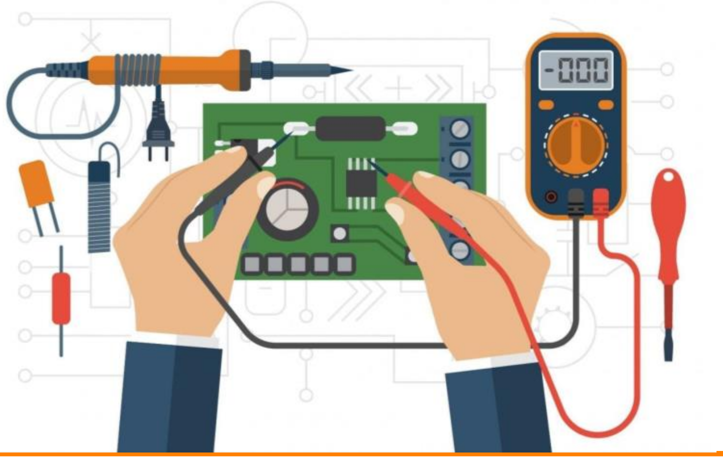
- 2-5 days training at our facilities in Valencia
- Basics of photonic test lab
- Wafer, chip and probe handling
- Electrical and optical probing
- Instrumentation control and measurement
- Data processing and analysis



Thank you for your attention!

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