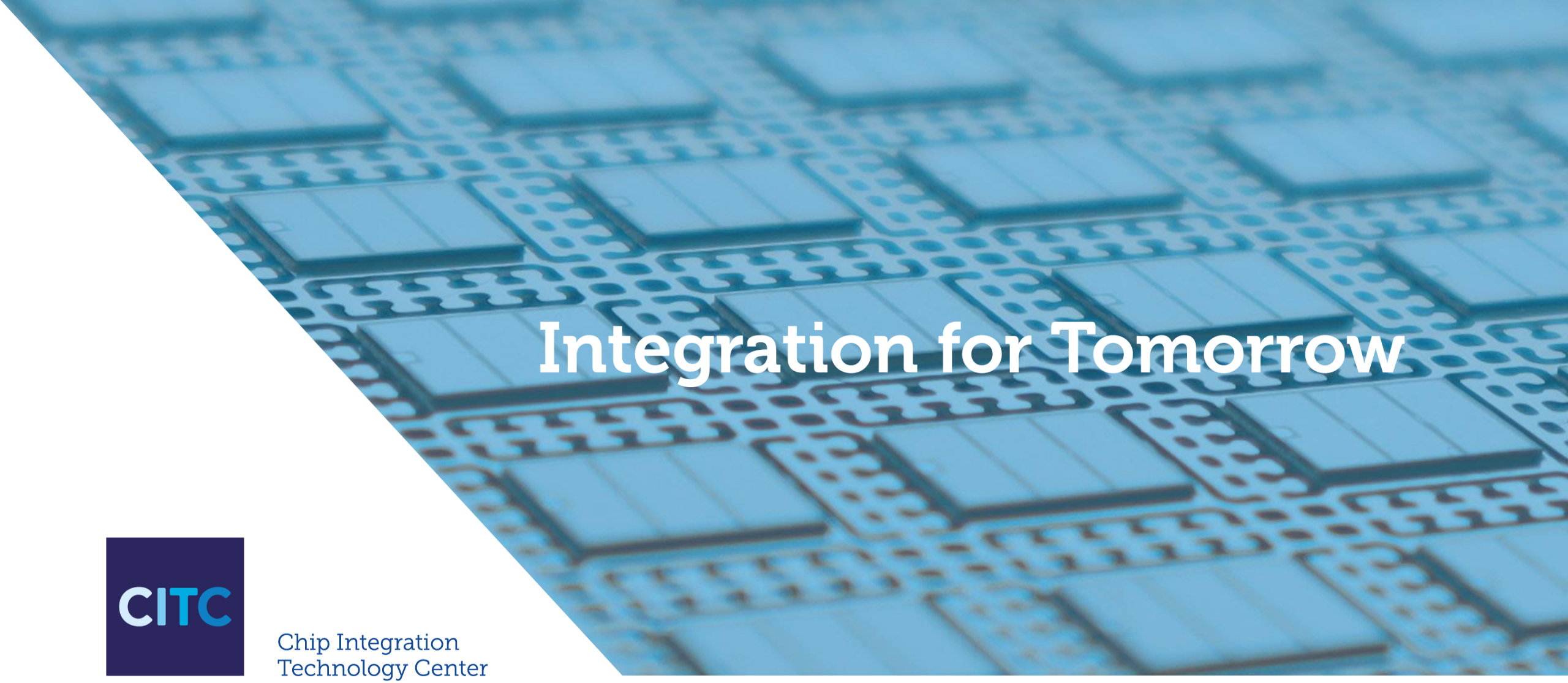


Integration for Tomorrow

CITC

Chip Integration
Technology Center

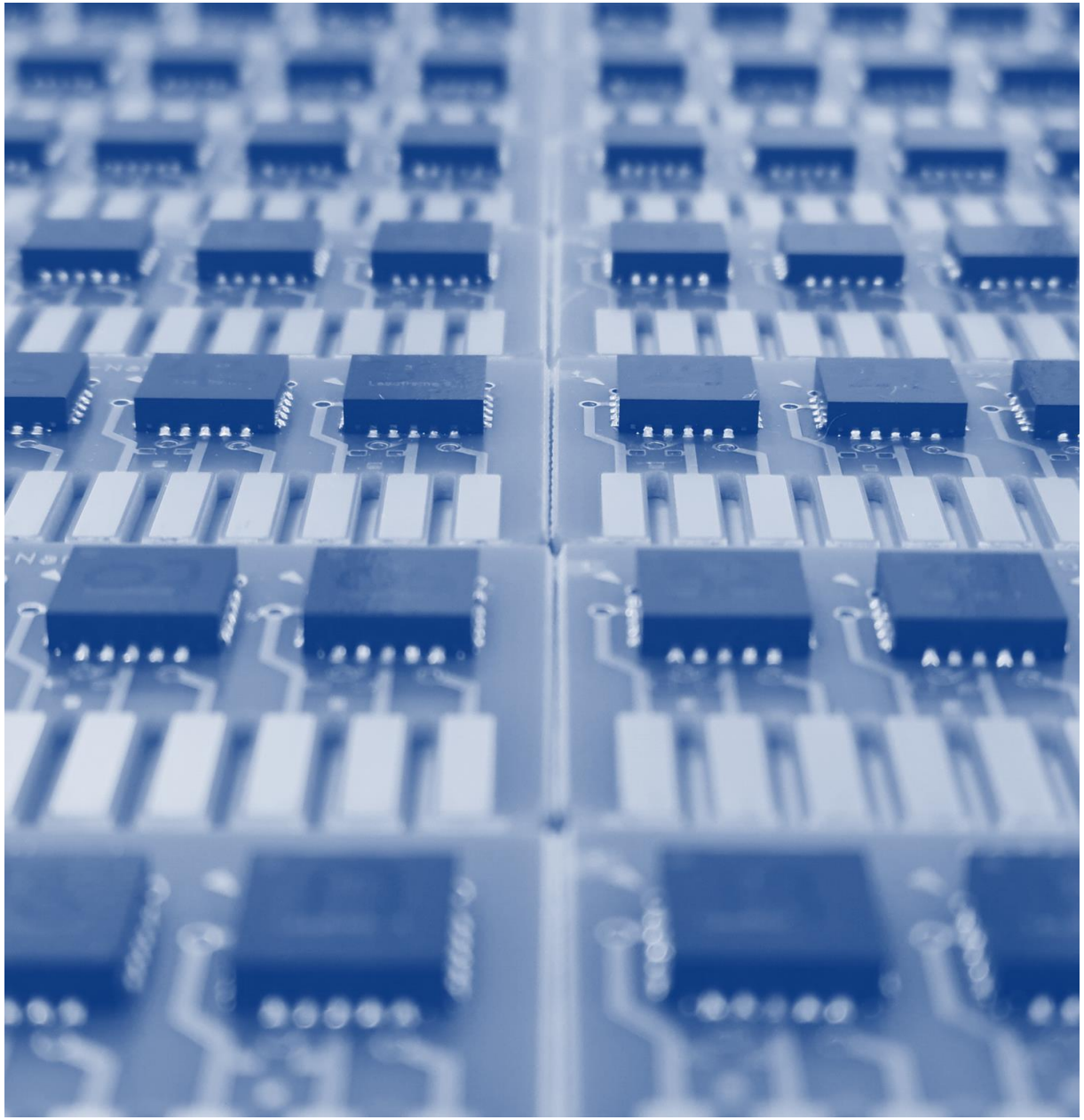
EPIC - Two sides of one Coin

Sander Dorrestein – CITC
Senior Electro-Optical packaging engineer

CITC
Chip Integration
Technology Center

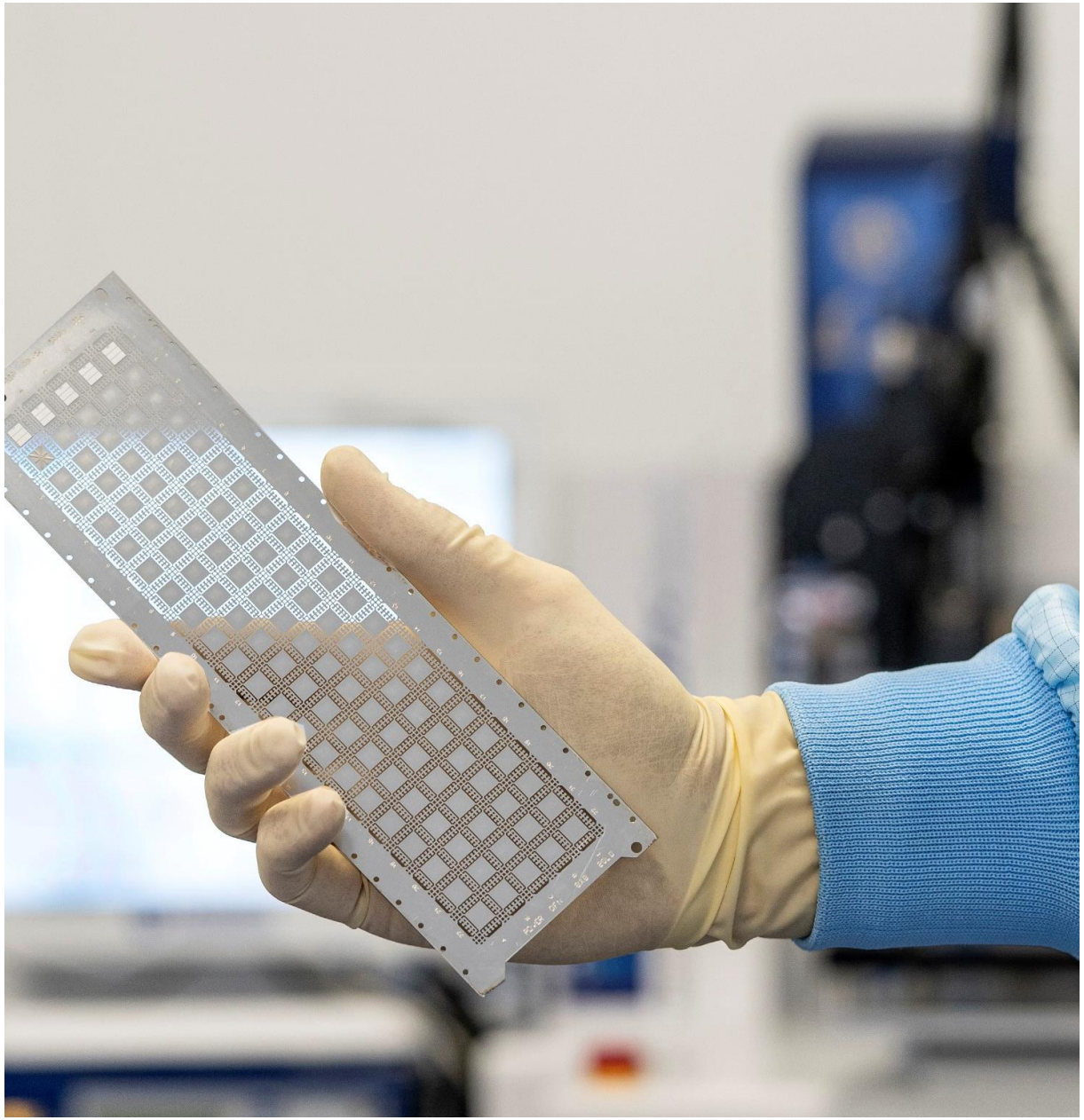
About CITC - who we are

- Joint innovation center founded in 2019
- Initiative of NXP, Nexperia and Ampleon
- Powered by TNO and TU Delft
- Located at Noviotech Campus, Nijmegen

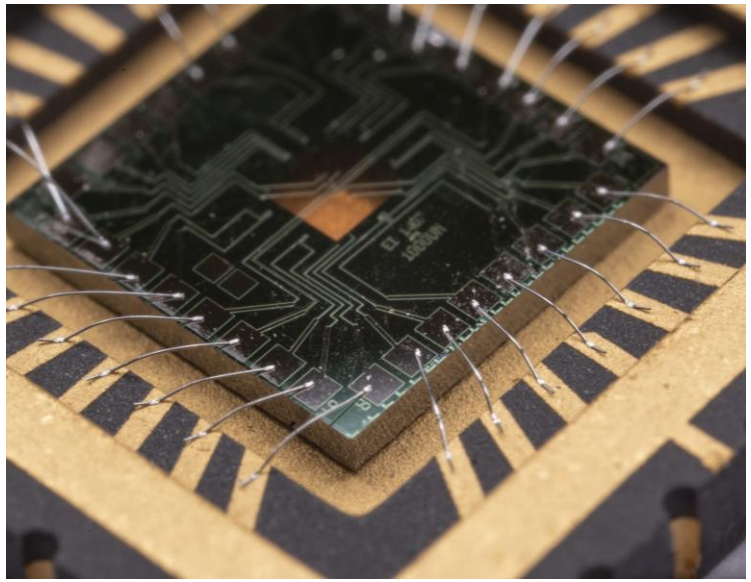


About CITC - what we do

- Development of enabling technologies for semiconductor and photonics packaging
- Create ecosystem to accelerate innovation in key application areas:
  - Power electronics
  - RF and mmWave
  - Advanced & Additive Manufacturing Packaging
  - Photonics Packaging
- Education and training
  - Semiconductor Packaging University Program
  - Internships and graduation/PhD assignments
  - Enthuse the young

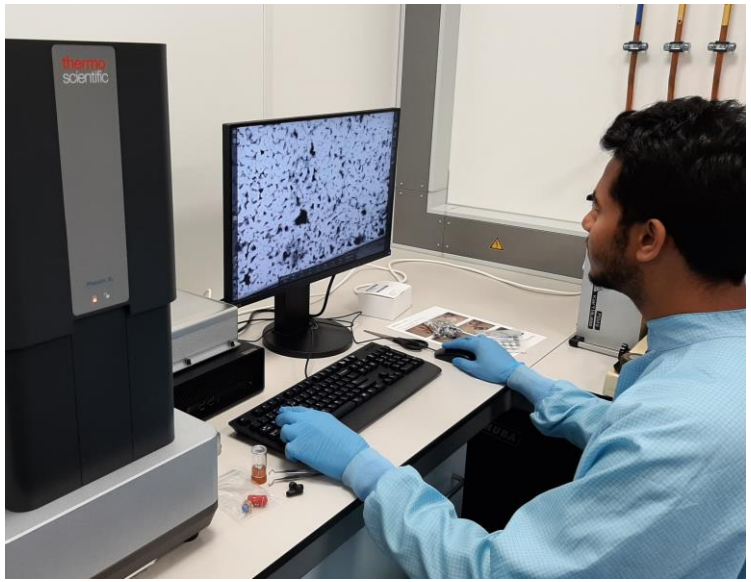


About CITC: what we offer



Access to innovation

- 2- up to 5- year research programs
- Together with partners



Access to infrastructure

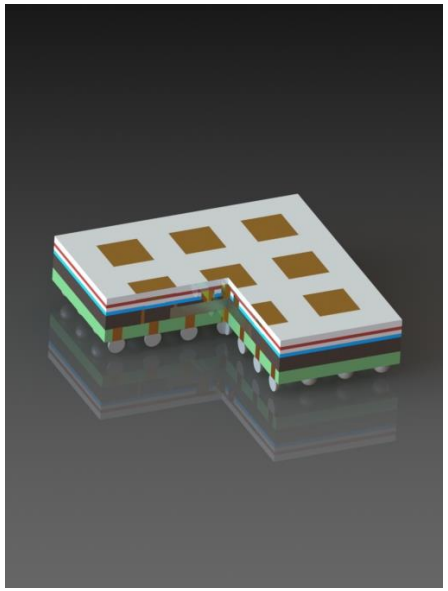
- Facilities support innovation and education programs
- Demo and application lab
- Available to third parties

Access to education

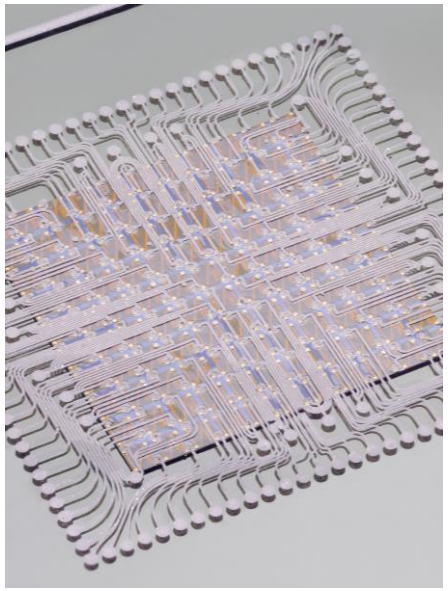
- Targeted education and training for young talent
- Together with companies and educational institutes

Access to innovation – Innovation programs

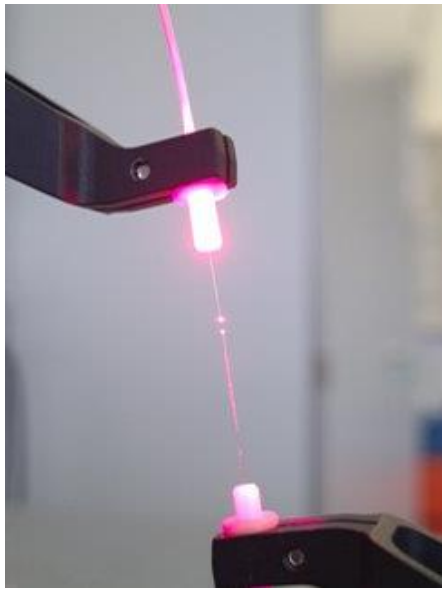
Thermal high-performance Packaging



RF packaging mmWave and AiPs



Advanced Packaging & Additive manufacturing



Integrated photonics

Two sides of one coin – MicroElectronics meets Integrated Photonics

Technologies in MicroElectronics

- Materials and technologies for 100 GHz and beyond
- Die attach materials thermal conductivity >150 W/mK
- Additive manufacturing technologies based on printing
- Strip/wafer and panel level concepts

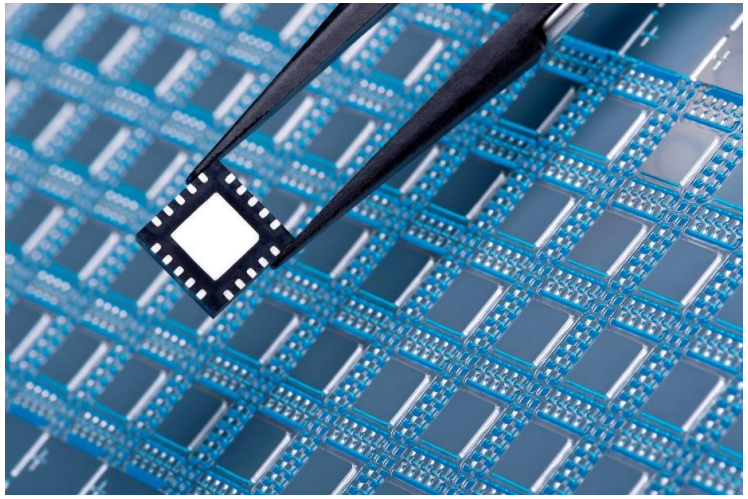
Shared Building Blocks

Challenges in Integrated Photonics

- Increased bandwidth
- Better thermal performance
- WLFOP Increased electrical and optical IO density
- Solutions for scalable volume manufacturing

Two sides of the coin – MicroElectronics meets Integrated Photonics

Typical MicroElectronics assembly



Batch / Strip / Panel processing

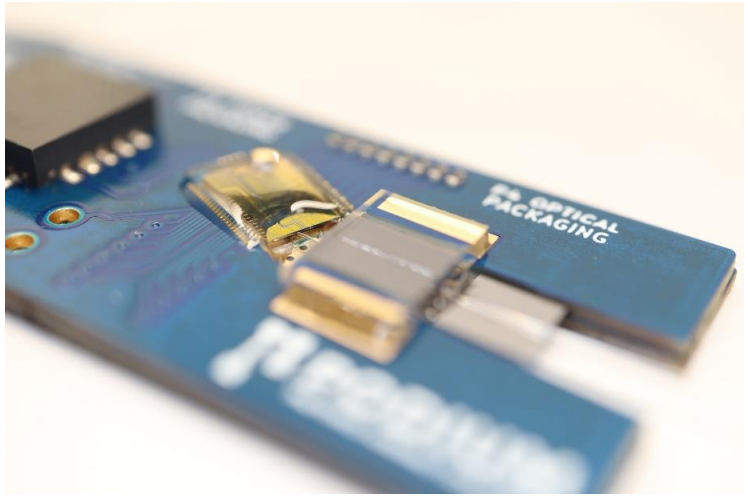
Multiple assemblies per lead frame

Reduced time for product handling

Automated loading and unloading

Standardized interface assembly equipment

Typical Photonics assembly



One piece flow

Single assembly per carrier

Long product handling time

Complex systems

Application specific tooling required

Available to packaging engineers

Packages

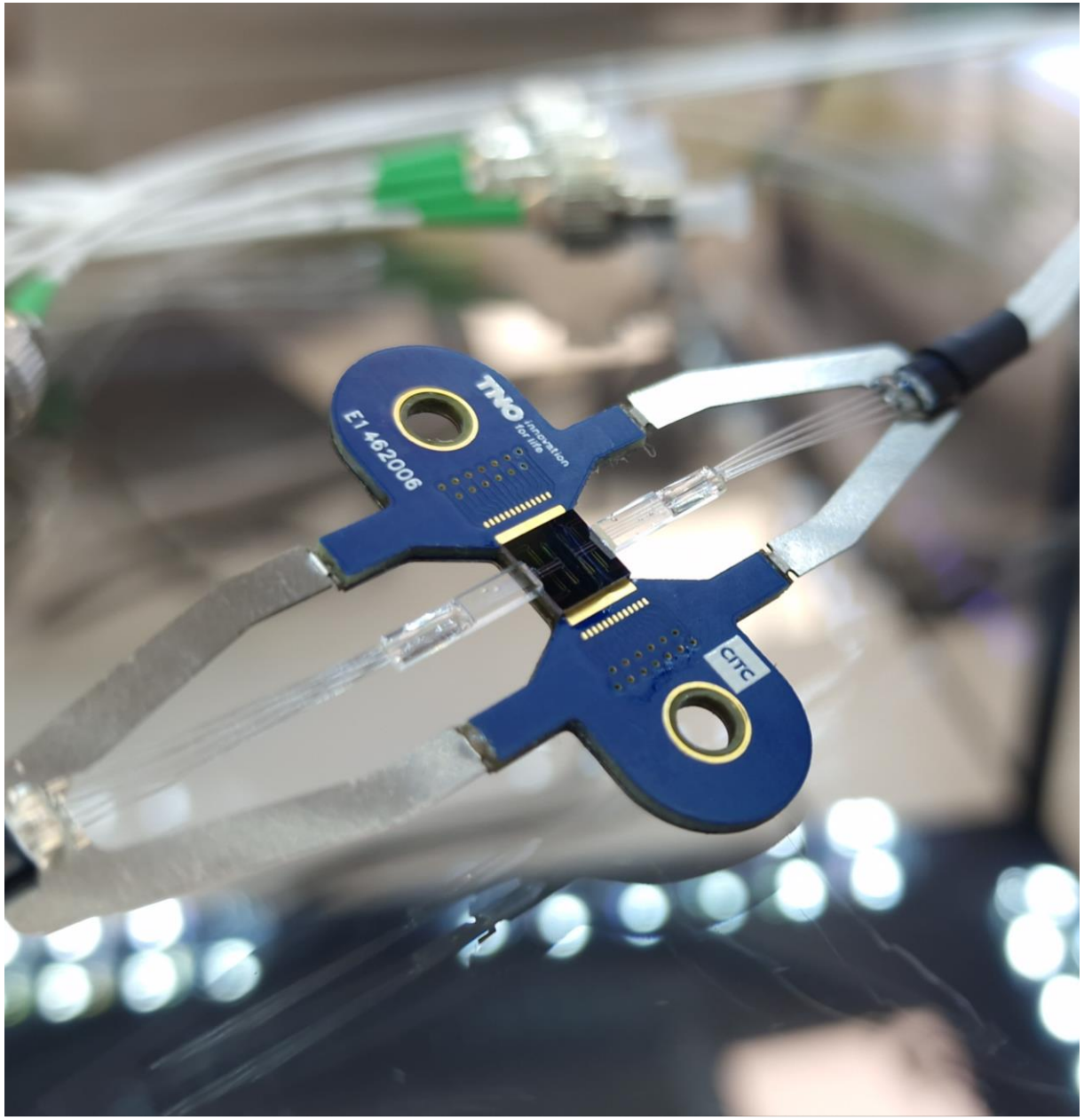
- Metal packages, Ceramic packages, LTCC packages, Plastic packages, On board assembly

Advantages of these packaging platforms

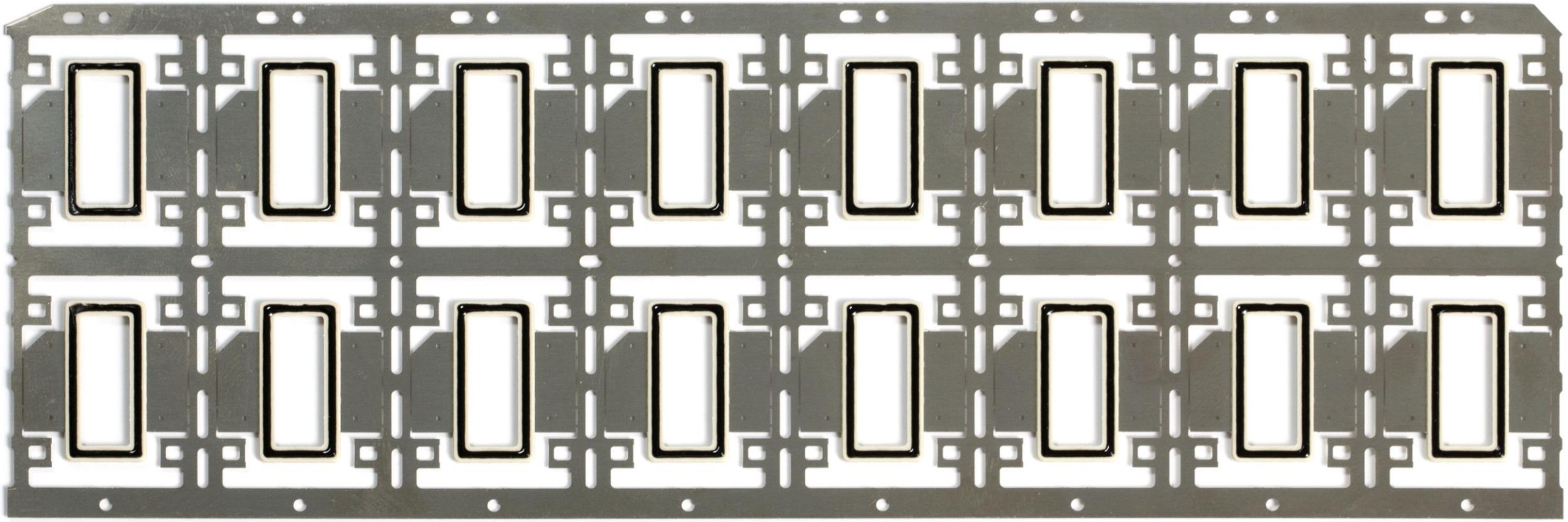
- Hermetic packaging
- Thermal
- High-performance and reliability

Disadvantages

- High cost per piece
- Difficult to scale for manufacturing
- Design flexibility

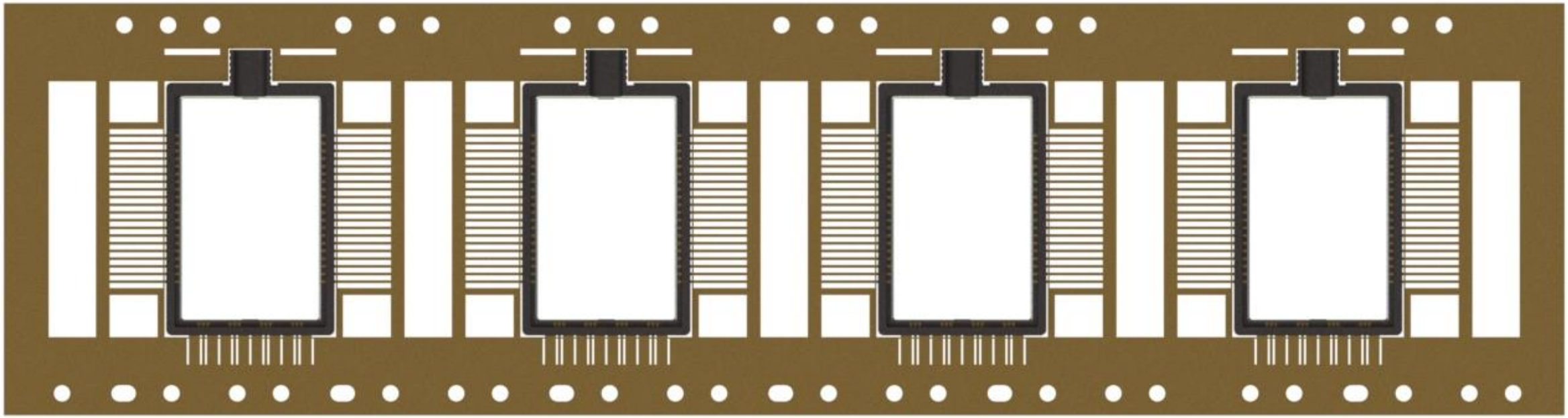


Scalable manufacturing – A step into Semiconductorization photonics



Strip of ACP transistors

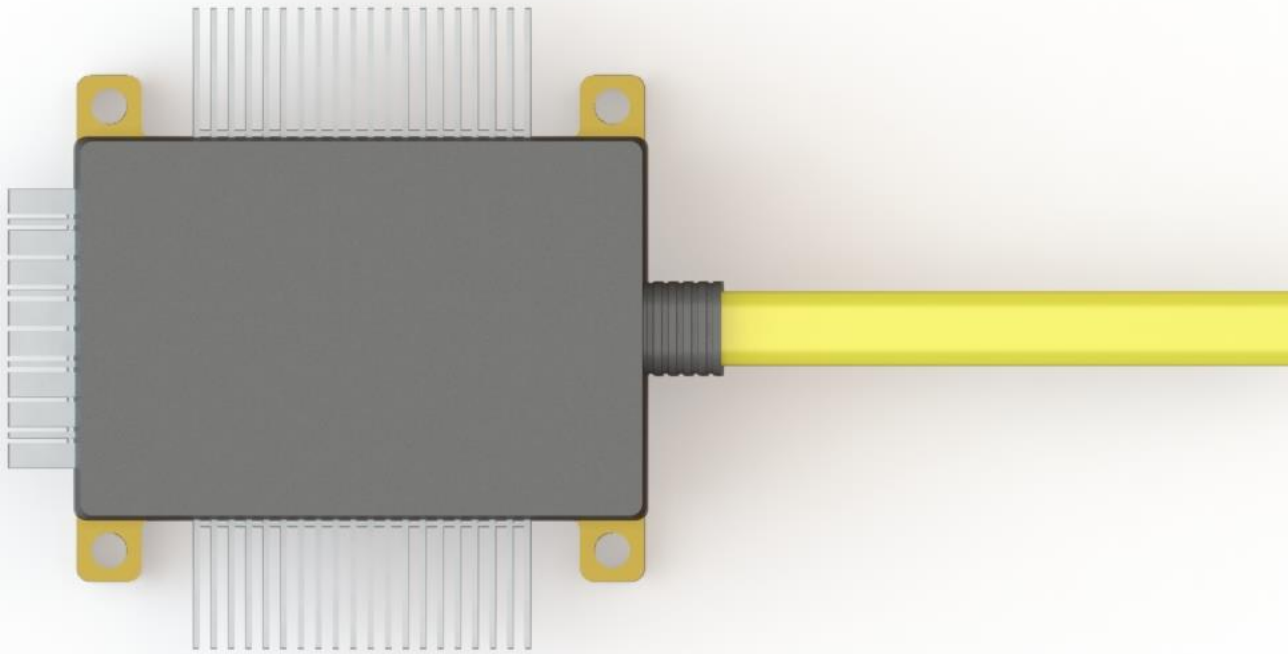
Semiconductorize photonics industry – Scalable manufacturing



Strip of “butterfly” packages

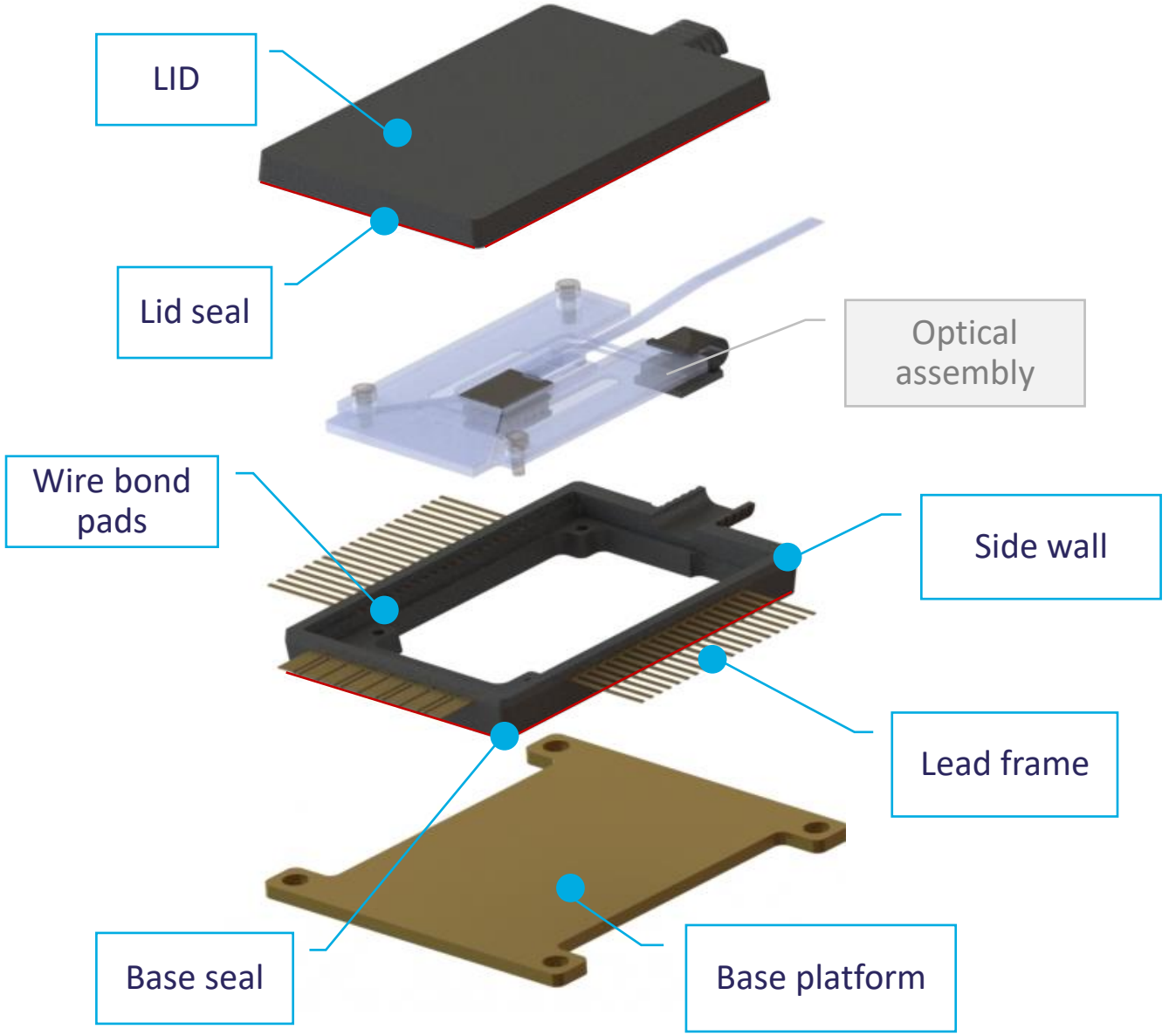
Air cavity package for Photonics Assembly

- Air-cavity package using low-moisture absorption and high temp liquid crystal polymer (LCP)
- Robust design provides near-hermetic performance
- Excellent mechanical reliability
- Good electrical and thermal performance
- Thermal expansion matched to minimize differential thermal stresses
- mold 2, 4, 8, 16 or 32 in a single strip (extended strip)
- Base of the package is a mechanically stable and robust platform

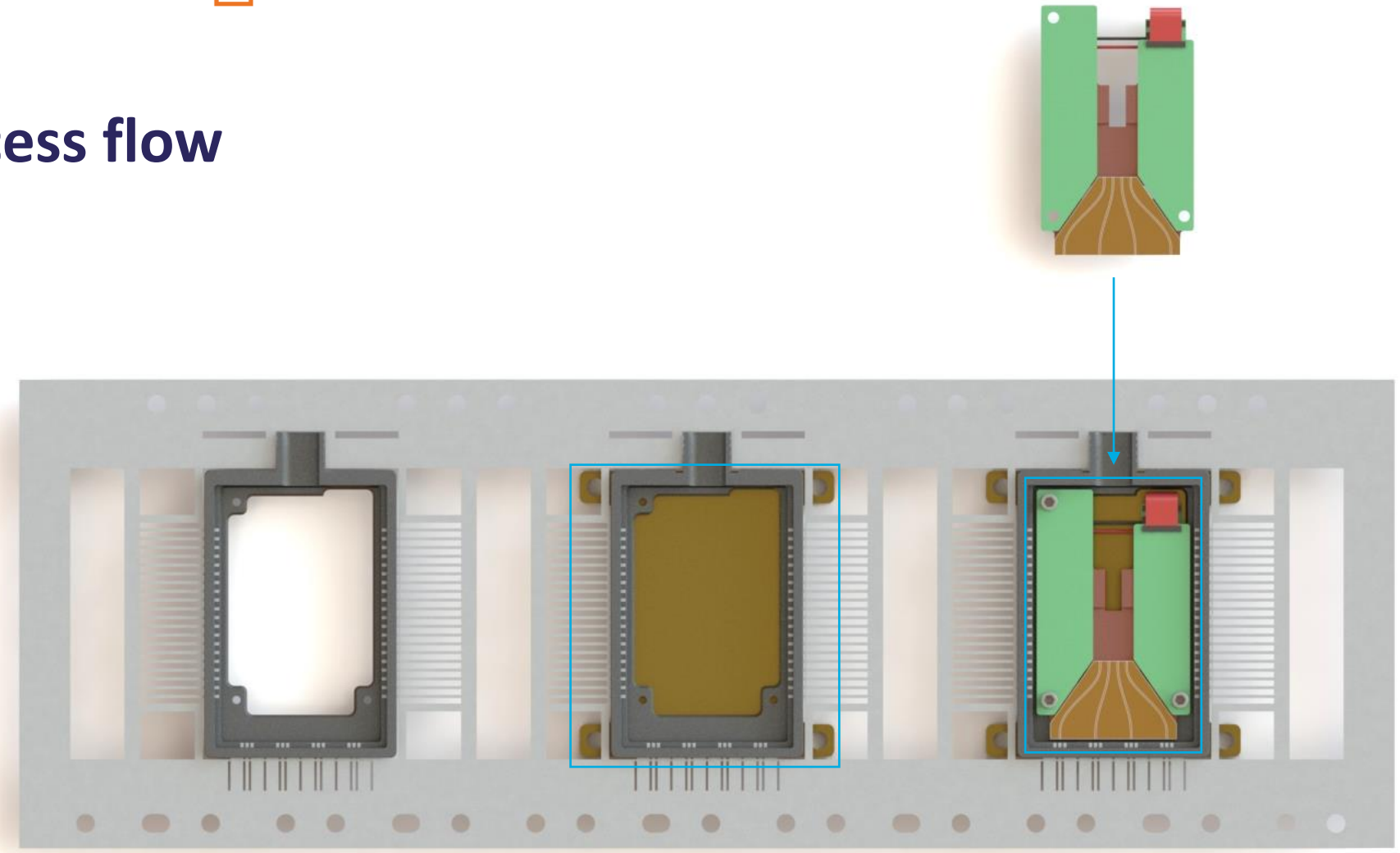


Plastic package elements

- Packages are molded around lead frames in a multi-strip format (2K moulding)
- Formulated Plastic to match the CTE of copper for low stress and reliability
- Leads are coated with moisture resistant polymer before injection molding
- Thermal-Mechanical rigid base platform ensures the stability of the optical and electrical assembly inside the package
- Lead frame configuration allows for automation of the assembly process steps (indexing)

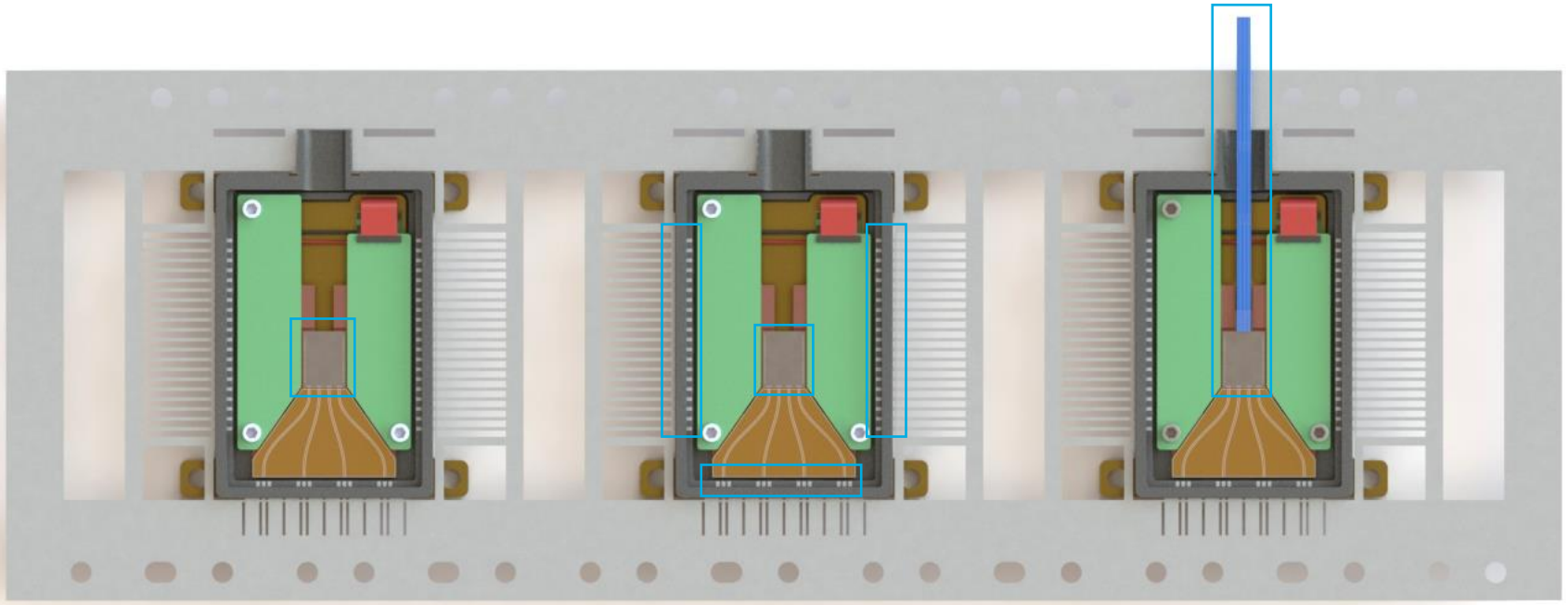


Build Process flow



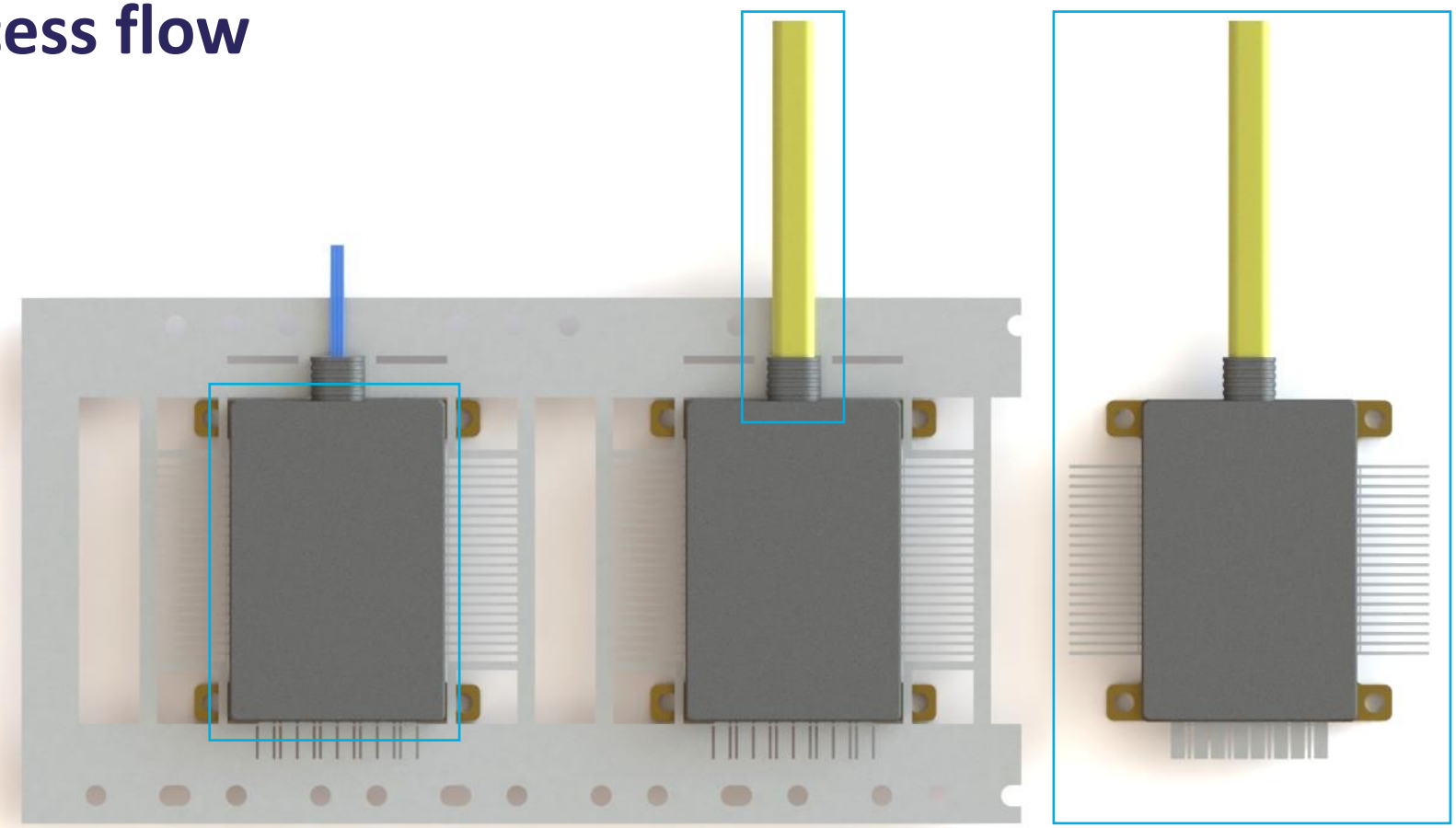
1. Start
2. Base attach
3. Mechanical assembly

Build Process flow



4. PIC attach 5. Wire bonding 6. FAU termination

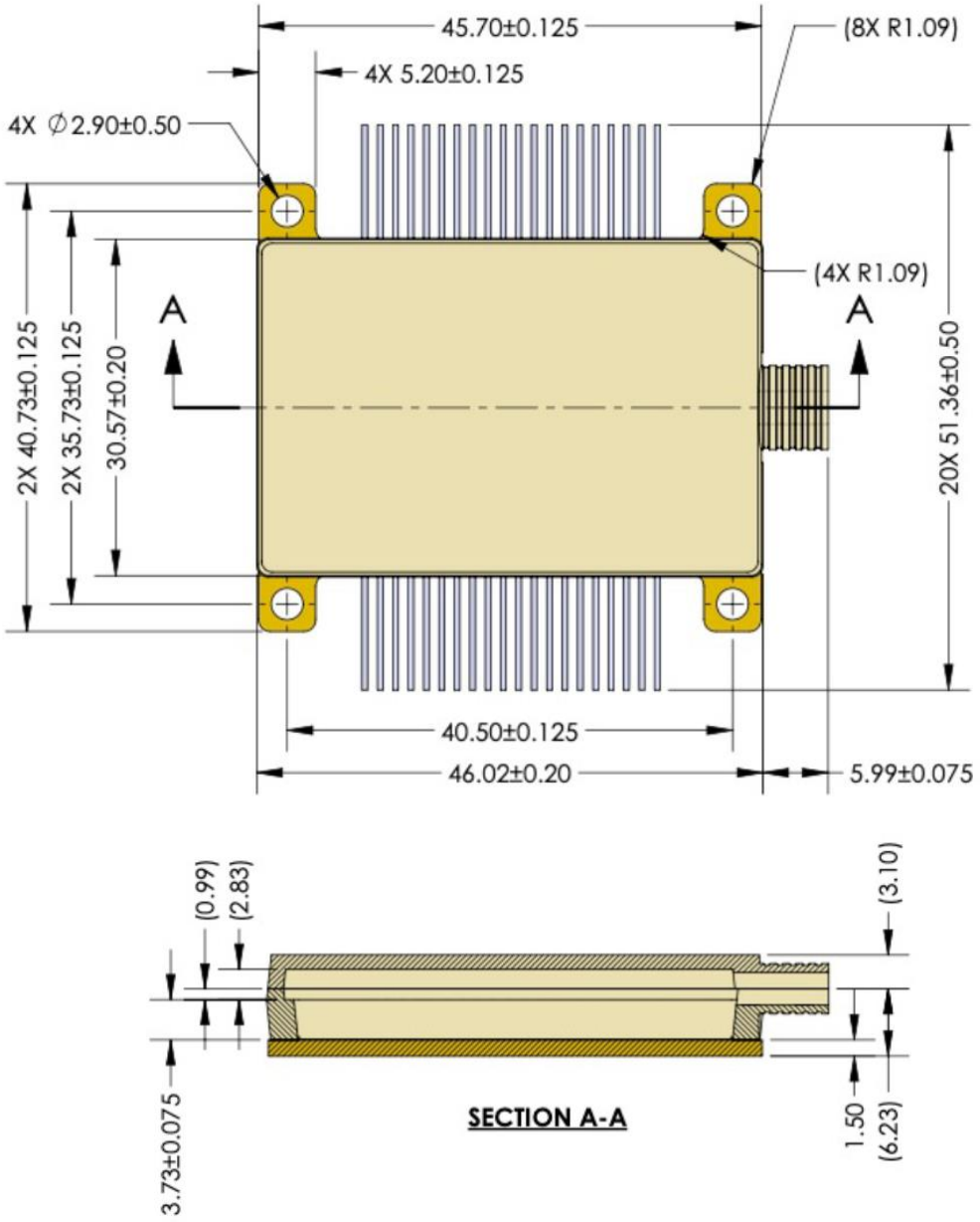
Build Process flow



7. LID attach 8. Cable termination 9. Package singulation

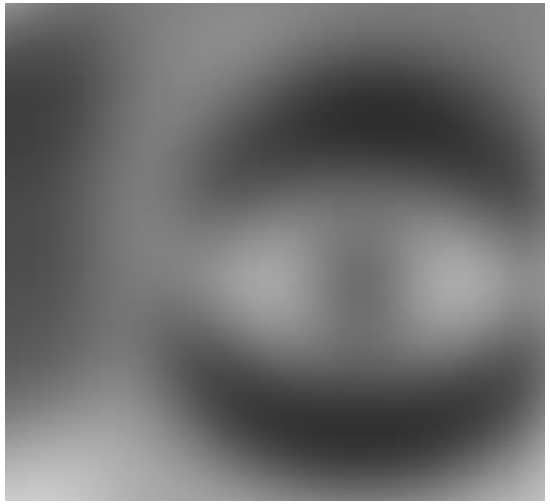
Air cavity plastic package features

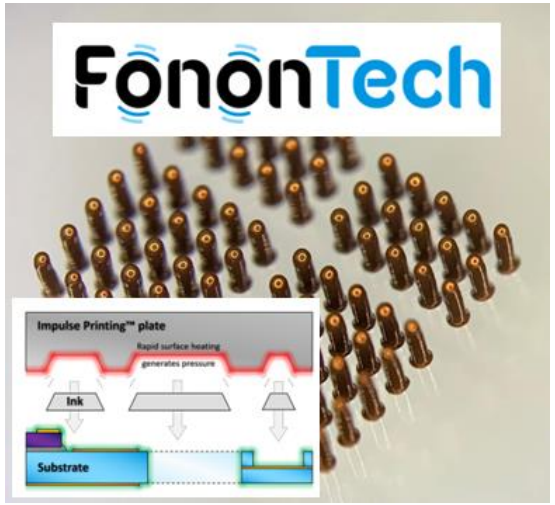
- Cost efficient, roughly 50% cost reduction BOM
- Design freedom and flexibility
- Mechanically robust package
- Automation of each process step, indexing
- Near hermetic package (10^{-8})
- Low investment cost for prototype tooling

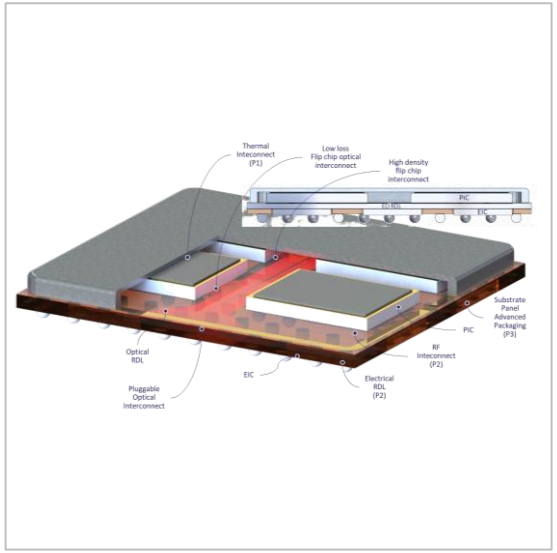


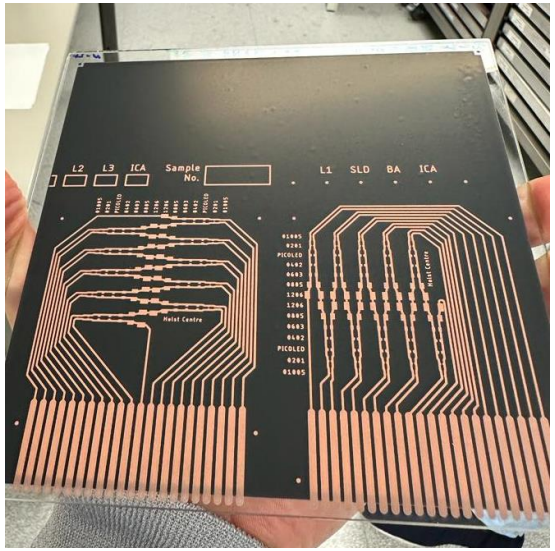
What's more to come…

- Panel level assembly platform for Hybrid Integration of Integrated photonics and Electronics
- Through polymer RF vertical interconnect Via technology featuring very high aspect ratio
- Direct Printing of Cu bumps, both at wafer level, or panel level
- Advanced packaging concepts by printing of metal inks, which potentially offers very significant advantages over established semi-additive methods









Thank you for your attention!

CITC

Chip Integration
Technology Center