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Former Professor, ESIEE Paris,
Univ-Eiffel, ESYCOM-CNRS

"Scalable Packaging of PIC Exploiting Wafer-level Optical and Electrical Interconnects"

EPIC Workshop on « PIC Postprocessing and Packaging »,
Laser World of Photonics, Munich, 2023 June 29th

About us

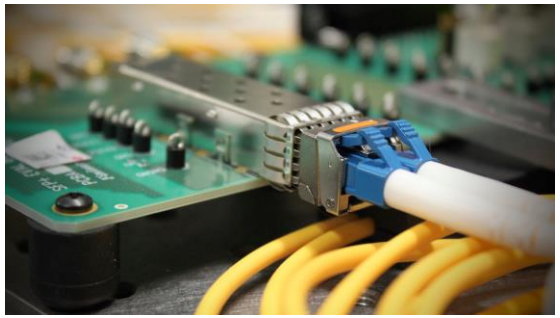
- Technological independent SME created in **2018**
- Offices and Clean Room Facilities in France, Paris region
- 10 Headcounts - **Strong R&D** > 50% PhD in Photonics
- Spinoff of CNRS research center

- **10+ years of R&D** in microfabrication and photonics integrated packaging
- 650m² cleanrooms **production-line** (Class 100) platform
- **Licensing agreement** worldwide with **exclusivity** including 6 patents

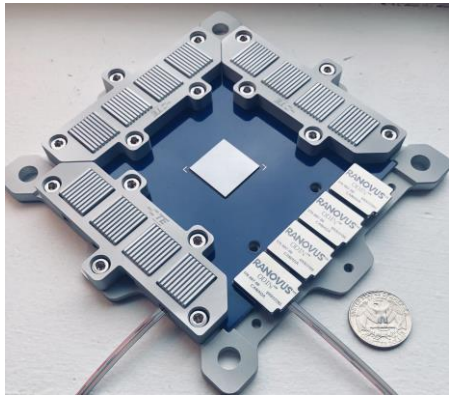
Mission: develop and commercialize fiber-to-the-chip connectivity solutions enabling the next generation optical and quantum applications

Market drivers

Pluggable Optics

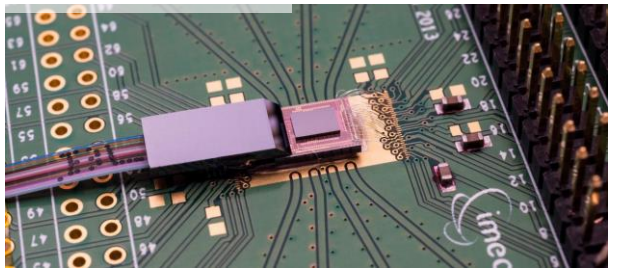


Co-Packaged Optics (CPO)



Ranovus 2021, nx100Gbps PAM4

CPO to 3D-chiplet



IMEC Si-PIC platform

- **Integration:** key to lower cost and higher density
- **Speed:** get smaller to get higher data rates
  - + Scalable and Cost-efficient model: <100$ per 100Gbit/s
- **Efficiency:** save energy and save photons
  - + Going above the 98% efficiency
- Getting light In and Out of the chip **with a new standard at wafer-level**

Optical Interconnects applications

Datacom optics

AOC, ethernet, CPO

Quantum

Photonics Hardware

Telecom

5G+ networks

3D Sensing

LIDAR

AI

Optical computing

Size ↓ Speed ↑ Density ↑

Among these markets, PIC are moving up very rapidly.
Quantum market itself is putting needs with 10000+ wafers per year in 2026+ for large size PICs

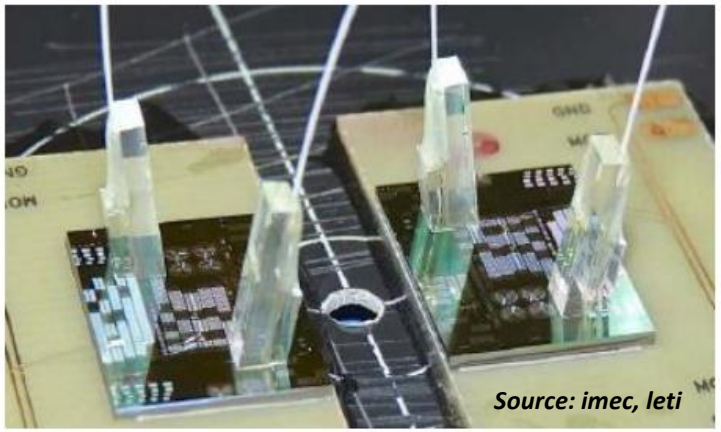
PIC challenges

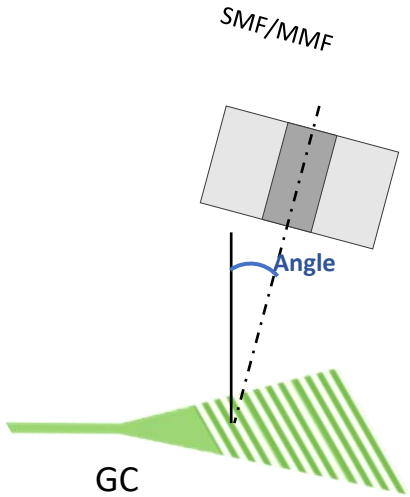
- PIC to fiber edge-coupling
  - Exhibiting intrinsic ultra low losses
    - Quantum applications are looking toward losses <0.1dB (T-98%)
    - 5G/6G or Datacom/Telecom: any 0.5dB saves 1dB electrically
  - Intrinsic low losses are not the only challenge, you need to ensure about the worst-case losses after managing the attachment and reliability tests to guarantee <0.5dB
  - Alignment tolerance is the key challenge with MFD 3-9µm (time/performance)

T(%)	A(dB)	Gom(dB)
1%	-20	-40
10%	-10	-20
50%	-3.0	-6
70%	**-1.5**	**-3**
80%	**-1.0**	**-2**
90%	**-0.5**	**-1**
93%	-0.3	-0.6
95%	-0.2	-0.4
98%	-0.1	-0.2
100%	**0**	**0**

PIC challenges

- PIC to fiber vertical coupling through Grating Couplers
  - Controlling angles (wavelength, temperature)
  - Mechanical fiber holder fixture on the wafer





5° to 15° with λ(T)
Target <0.5dB losses over 50nm+

PIC challenges

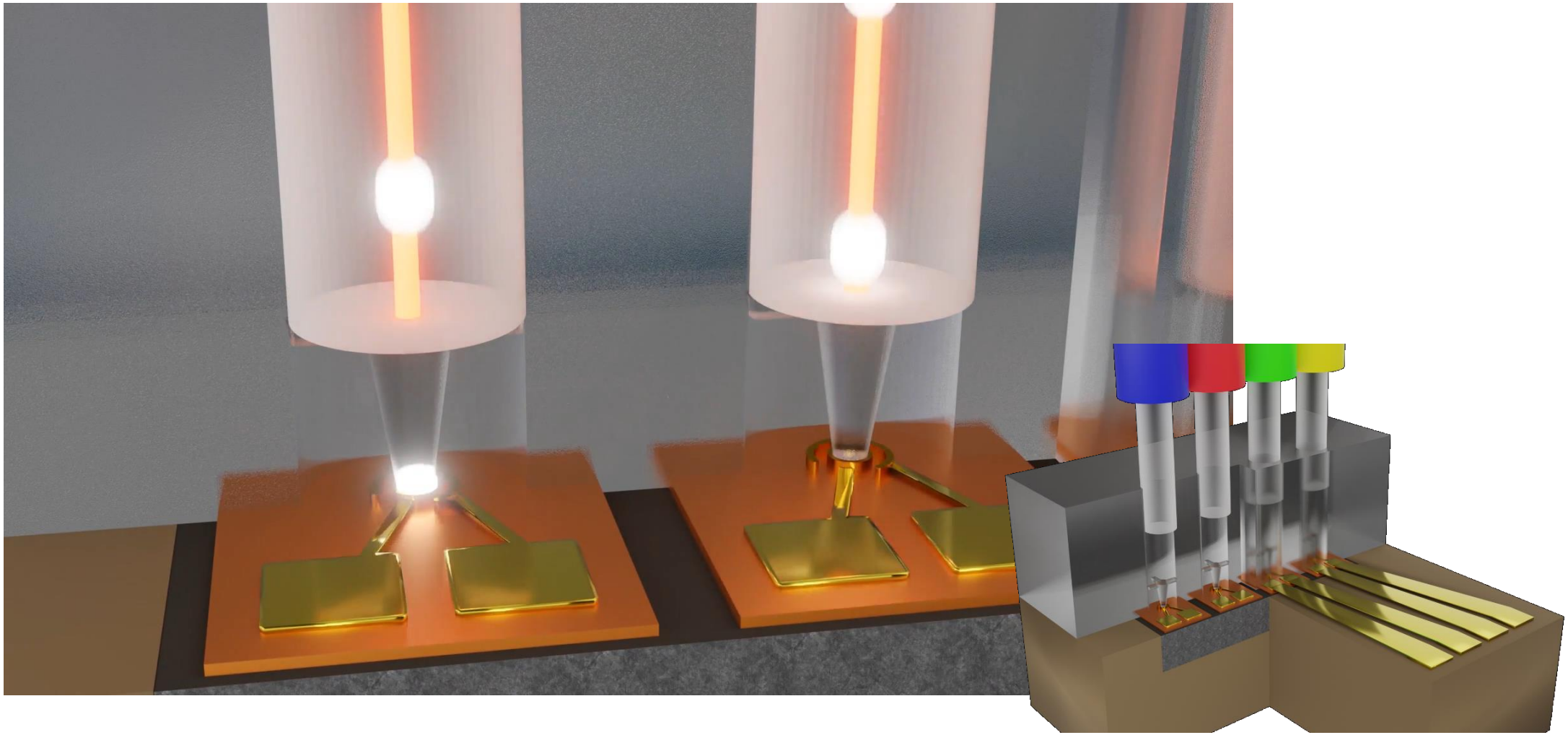
- PIC to PIC free-space links
  - Smaller PICs to reduce the development cycles / increase the yield
  - Choice on the platform of integration / tolerance of alignment

    => Short distance links (<1-3mm)

- LiDAR and free-space launch:
  - Small pitchs for the emission/reception: 30µm ··· 127µm

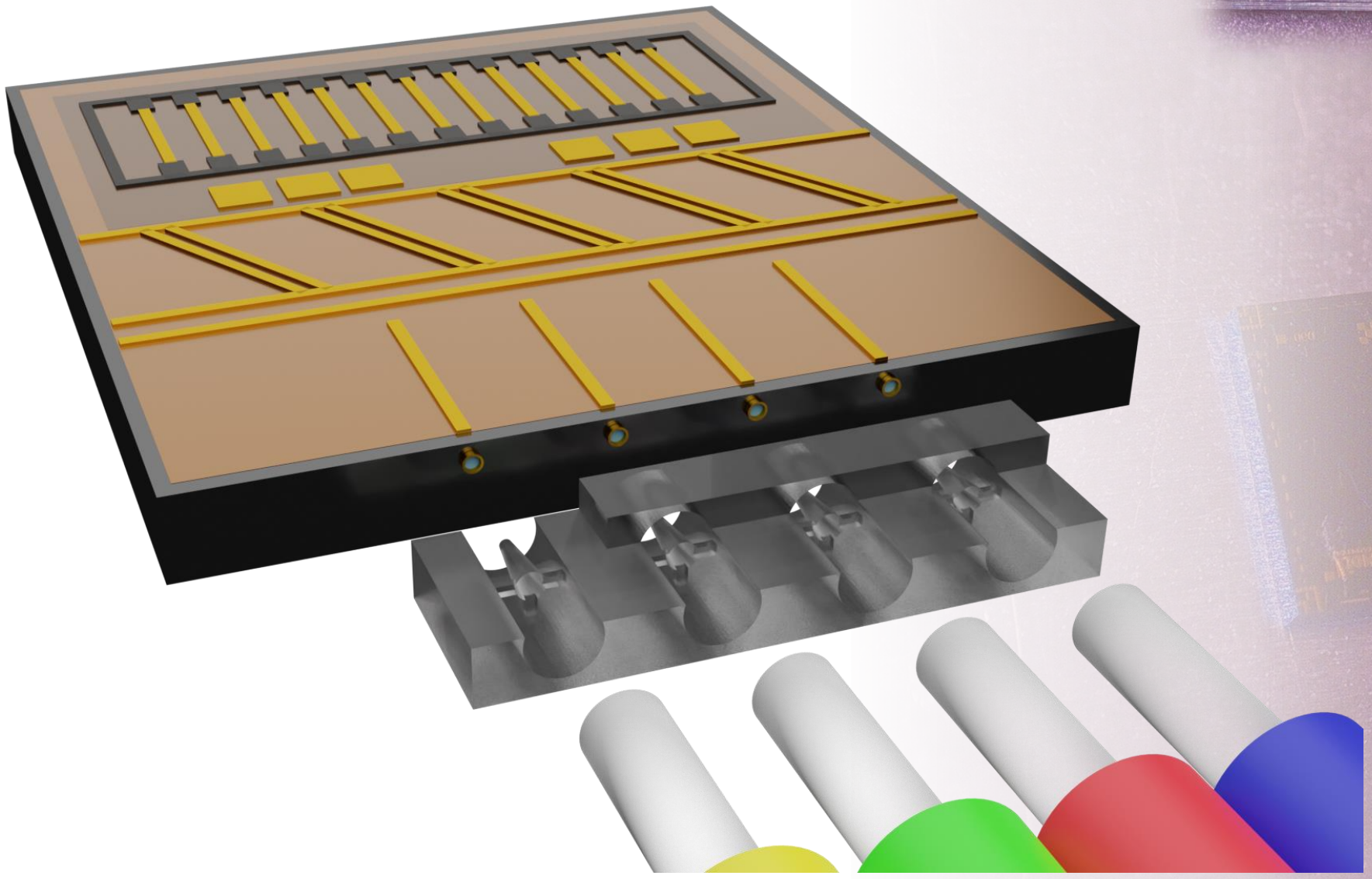
- PIC mmw-interface to drivers and FPGA/ASIC
  - Bandwidth >60GHz to address >112Gbps/224Gbps

ICON Photonics Technology

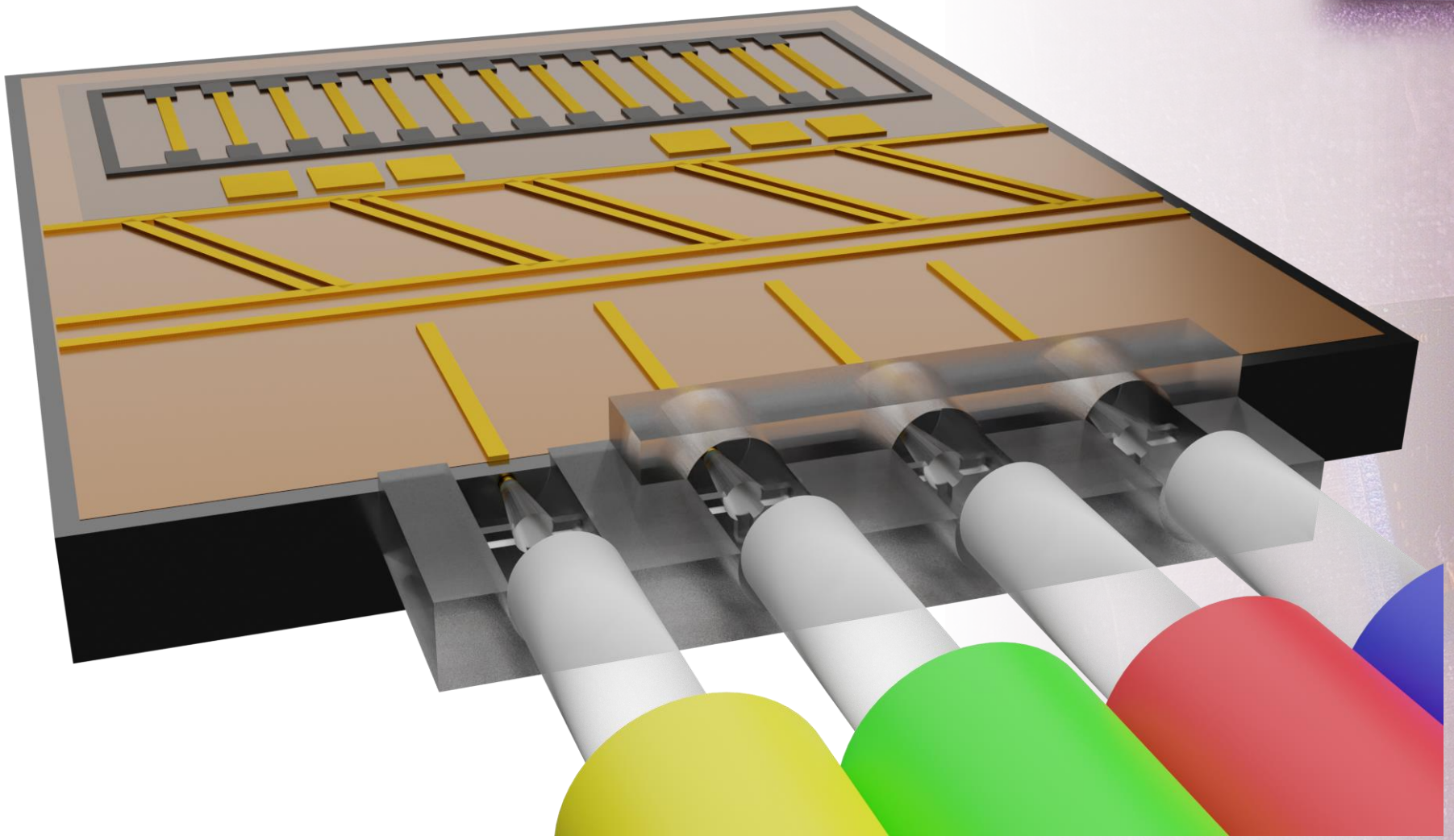


All-in-one-package: Photonics + Electronics + Mechanics integration

Focus on PIC to fiber coupling

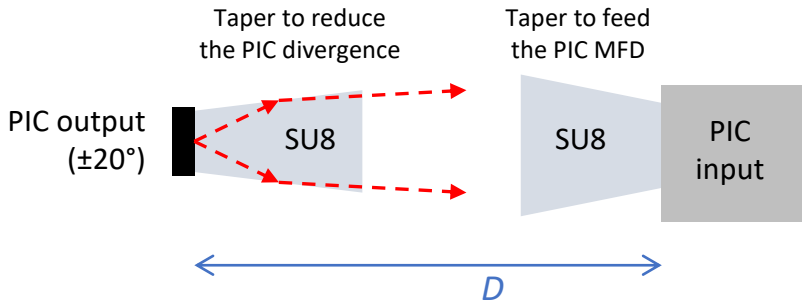


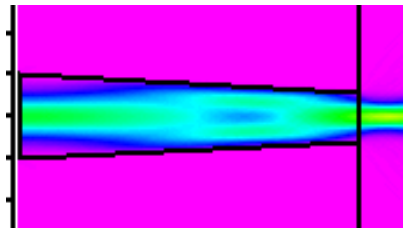
Focus on PIC to fiber coupling



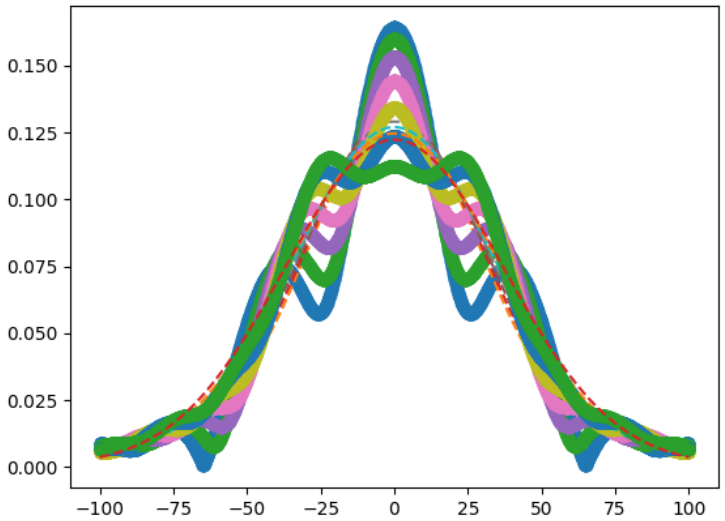
PIC to PIC / PIC to free-space

Spot size converters

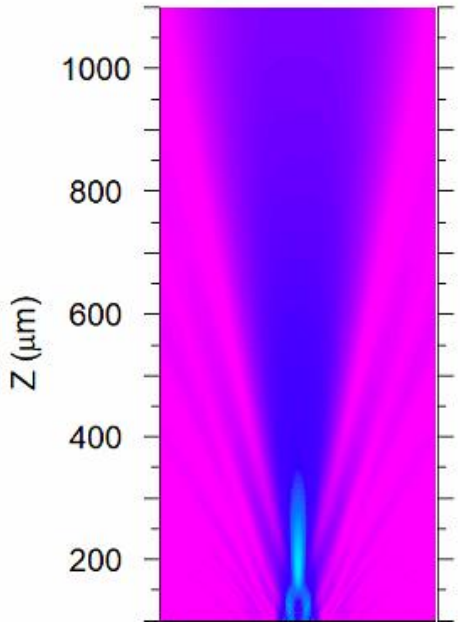




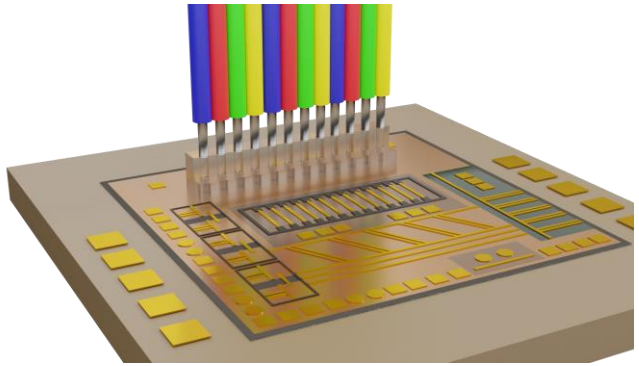
Flatbeam profiles

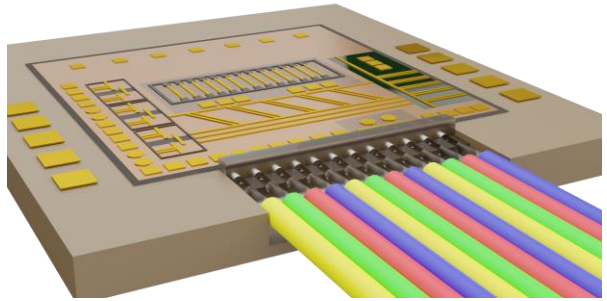


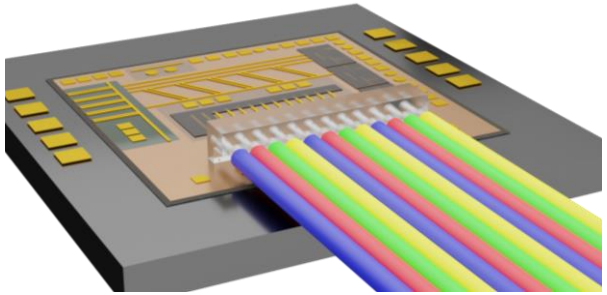
Low divergence / Collimation



Ultra-low-loss coupling solutions as a service







Surface I/O array

MMF, SMF, MCF
Top / back-side
PD, VCSEL, GC-PIC (<0.5), SNSPD, TES
Both silicon interposer and full-wafer possibilities

Edge I/O array

EEL, DFB, DBR, Edge-PIC
SSC, MMF, SMF
Both Silicon interposer and standalone possibilities

Surface to Edge I/O array

Upcoming

SMF and MMF

Coupling loss <0.1dB

70µm to 10µm (MMF)

50µm to ~1µm (SMF/MCF)

Fiber holder with passive alignment

SMF

Coupling loss <0.5dB

Active alignment (standalone)

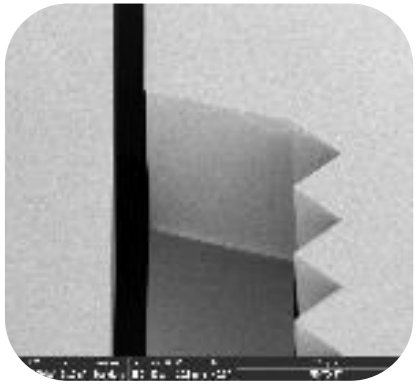
Passive alignment (clipping option)

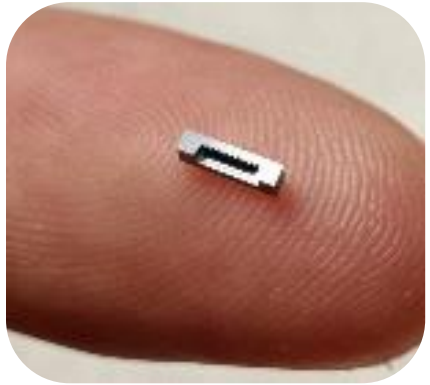
Advantage of surface I/O array

For all :
- Zero-Air-Gap option or ARC
- Si interposer up to mmw

Off-the-shelf product offer

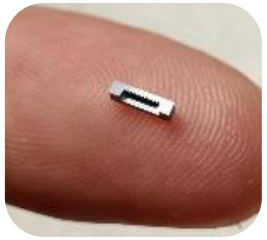
V-groove replacement solutions (FH)

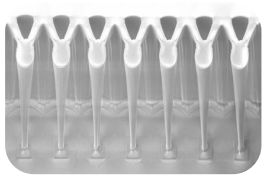


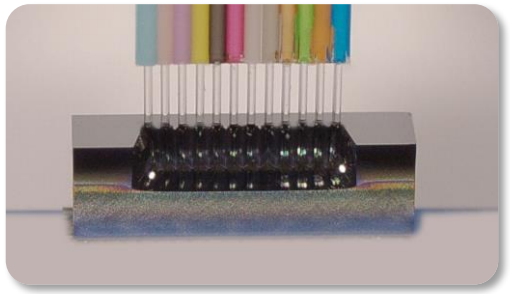


ARC termination option available

Fiber-Array-Units

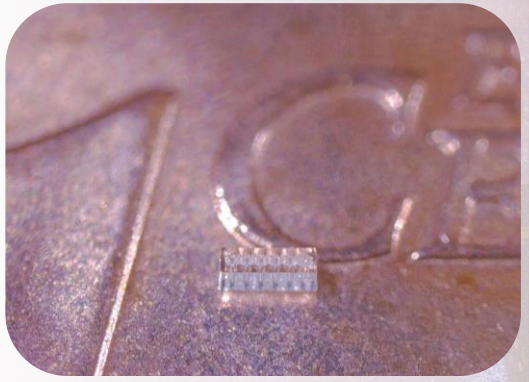


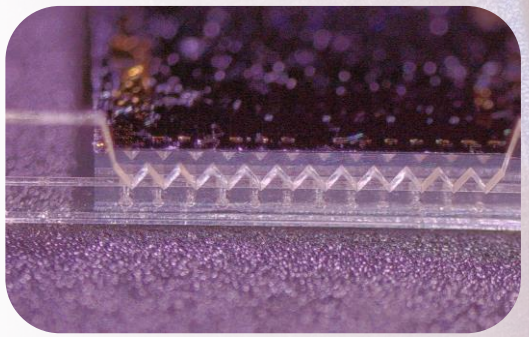




ARC termination option available

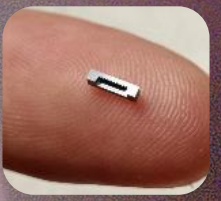
Standalone SSC - Beamshaper

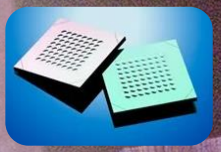




ARC termination option available

FH + SUSS





We design and produce for you

Off-the-Shelf Components

Manufacturing Services

Standard Products

1

› *Fiber-array-Units (FAU), V-groove replacement Solutions (FH)*

Multi-Project Wafer Runs

2

› *Semi-custom products and assembling services*

Custom Design and Prototyping

3

› *Custom-made prototypes to the customer technology and applications*

Manufacturing and Quality

4

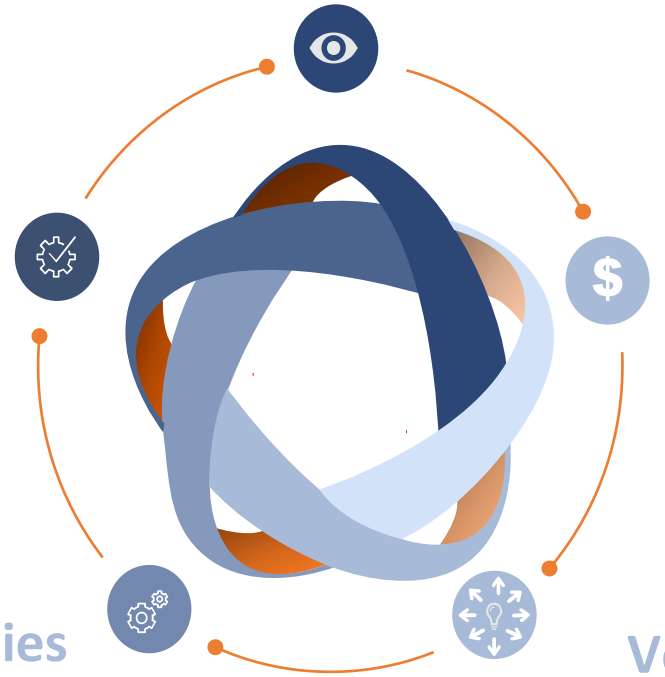
› *Low, Medium, up to High-volume production*

One-stop-shop from design to industrialization

Thin-film Polymer Benefits?

Optical Properties

› **High transparency** (from 500nm up to 5µm)
› Low coupling losses (<0.5 dB and <0.1dB)
› **ARC compatible / Fiber refractive index continuity**



Reliability

› **Telcordia compliance**
› Mechanical stability
› Chemically resistant
› Thermal stability
  › **Cryogenic** temperatures <100mK
  › **Reflow compatible up to >350°C**

Cost effectiveness

› Material
› **Wafer-level process**
› UV mask lithography

Mechanical properties

› High aspect ratio
› Adhesion & Bonding
› Biocompatibility

Versatility

› Contact mask design
› **Monolithic and hybrid options**

From °mK cryogenic to high-temp >350°C conditions

Invitation to visit ICON Photonics @ECOC 2023

ECOC 2023

Glasgow, Scotland
October 2023

2-4 October 2023, Booth #830

- Showcase of products and services
  - Fiber Array Units (FAU)
  - V-groove replacements (FH)
  - Chip to Fiber Interconnects
  - Si-interposer solutions

Thanks

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www. icon-photonics.com