PIC-based system development: From idea to product

EPIC Technology Workshop on PIC Post-Processing & Packaging at the LASER World of PHOTONICS

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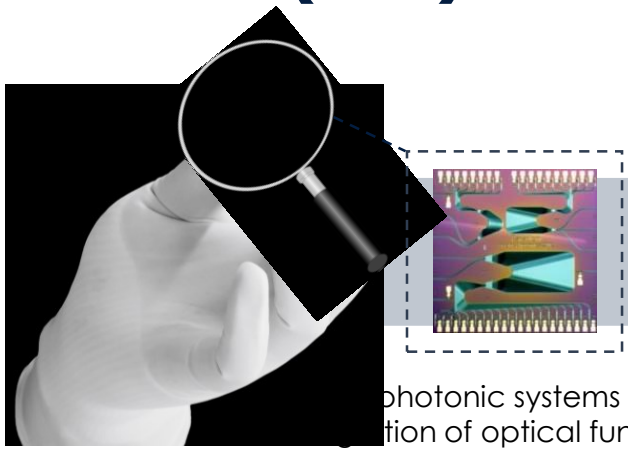
29 June 2023

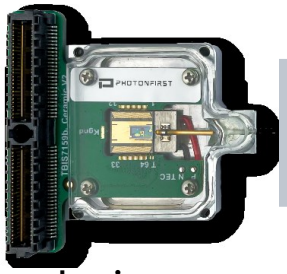
PHOTONFIRST
Integrated Photonics Sensing

JePPIX
Platform for Photonic Integration

PhotonFirst develops and produces Photonic Integrated Circuits (PIC)- based sensing systems



hotonic systems are based on **PICs**:
tion of optical functionalities onto a chip

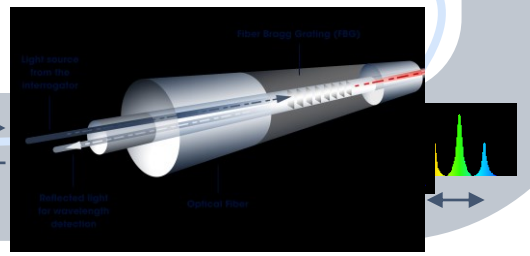


PIC **packaging**: connecting and protecting the PIC to and from the application environment

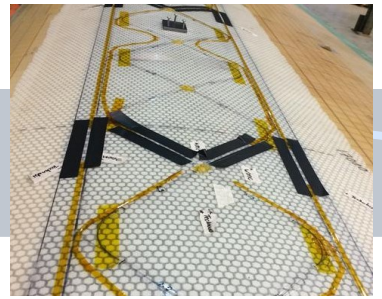
MEASUREMENT AND ANALYSIS OF:

STRAIN PRESSURE TEMPERATURE

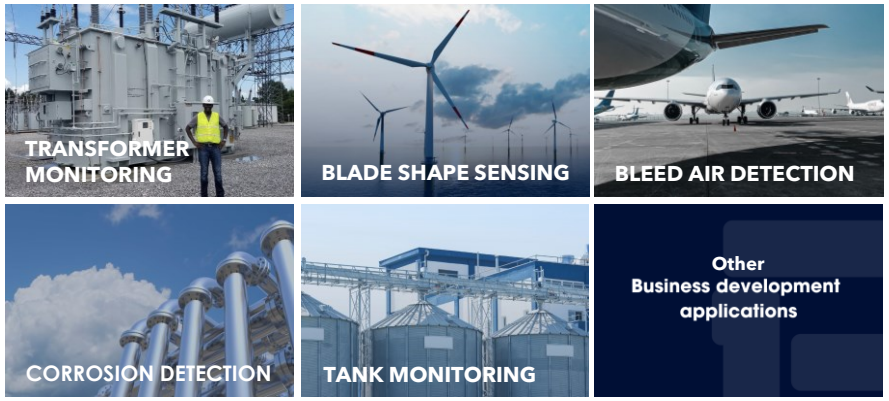
SHAPE ACCELERATION VIBRATION



Fiber with fiber bragg grating (FBG)



Customer's asset (for example wind turbine)



PIC Packaging: To Connect and Protect

Environmental conditions external

- Temperature (Env. range, dynamics)
- Mechanical (vibrations, shocks, stress)
- Radiation (sunlight, radiation, EMI)
- Materials (reactivity, oxidation, humidity)
- Operational (electric current, IR light)

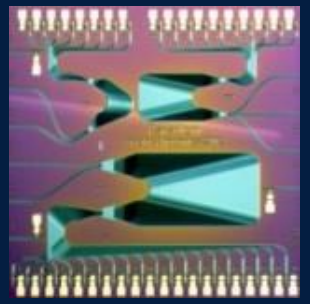
Environmental needs internal (PIC)

- Temperature setpoint, stability
- Mechanical (connectivity, stress)
- Radiation (radiation, EMI)
- Protection (humidity, hermiticity, coatings)
- Operational (electric current, IR light)

In packaging the application and PICs meet:

- User needs and use (environment) conditions
- PIC function and functional (environment) conditions

From Concept to Product



Technology readiness levels (TRL)

The TRL levels for a PIC based system in development:

TRL 1 – Concept

Idea, basic calculations, reference in publications

TRL 2 – Theoretical study

Analytical study, computer model, ASPIC building blocks defined

TRL 3 – Feasibility study & experiments

Analytical & laboratory tests. Separate building blocks on test bench

TRL 4 – Demonstrator / Proof of Principle (Will the architecture work?)

Full ASPIC tested on test bench or in basic package, laboratory electronics and software

TRL 5 – Functional model (Is the architecture working as specified?)

Chip packaged in dedicated package with dedicated electronics and hardware

TRL 6 – Prototype

Complete system in housing, tested in laboratory or simulated environment

TRL 7 – Implementation / pre-series TPD

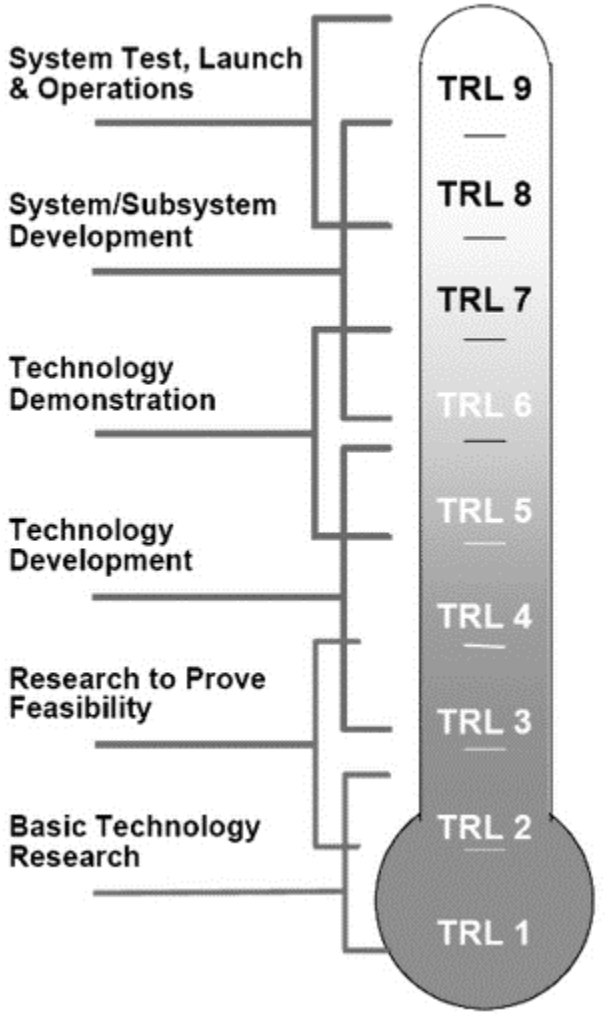
Actual system in actual application

TRL 8 – Qualified product

System qualified by testing and demonstration

TRL 9 – Final product

Fully operational system (repeated orders according TPD)



Conceptual & Theoretical study (TRL 1-2)

A development starts with an idea or customer request:

Translate idea or request into requirements:

- What should the system measure
- In which environment should the system operate
- What regulation should the system meet (Law, safety, et
- What should be the lifetime of components
- Performance vs Cost

TRL 3 Feasibility study (Simulation and experiments)

Analytical & laboratory tests. Separate building blocks on test bench

Design of a PIC in this phase to explore feasibility:

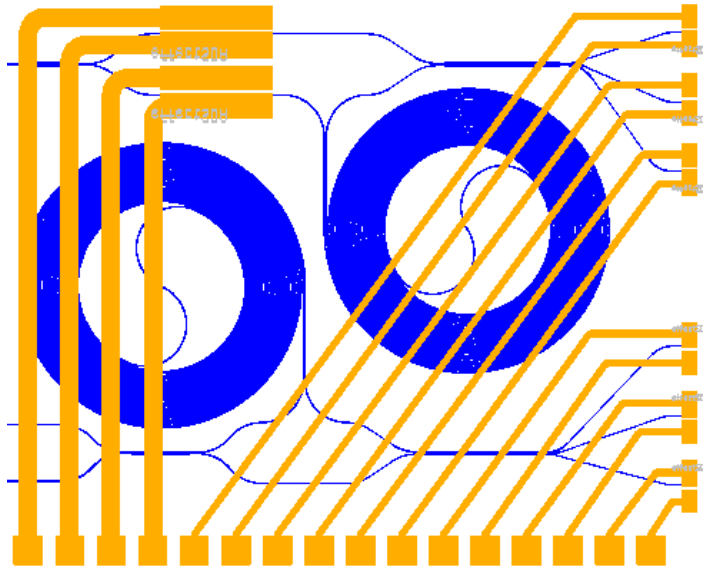
- Explore the building blocks required,
- Which building blocks are available and known
- Development of new building blocks in this phase

Think on how the chip should be tested:

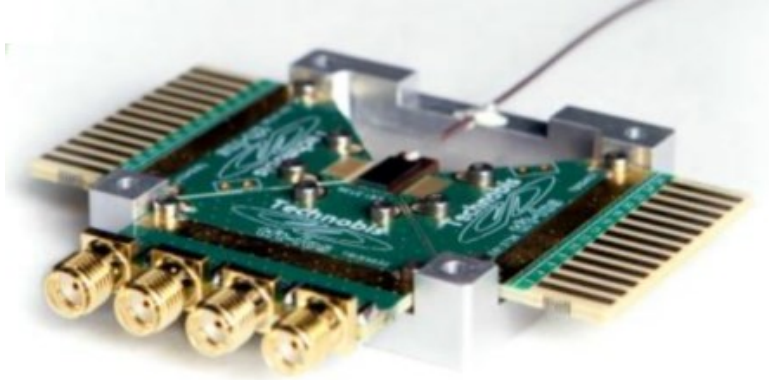
- Separate test circuits of critical buidling blocks
- How will optical connection be made? *(PIC-PIC, PIC-fiber?)*
- Can you make all the design conclusions based on the test-circuits?

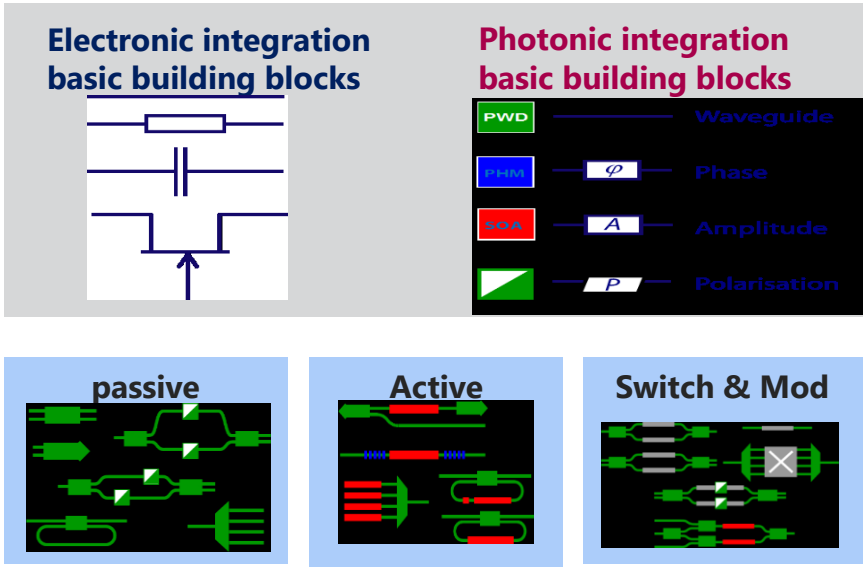
“Make your life easy”

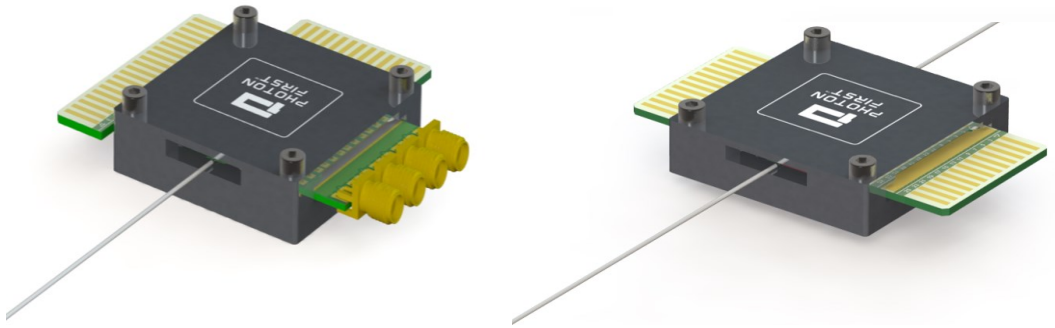
- Developing a package or new test setup is expensive.
- Make your PIC design compatible with existing test setups
- Make your PIC design compatible with existing packaging solution



From idea to proof of concept (TRL 3-4)

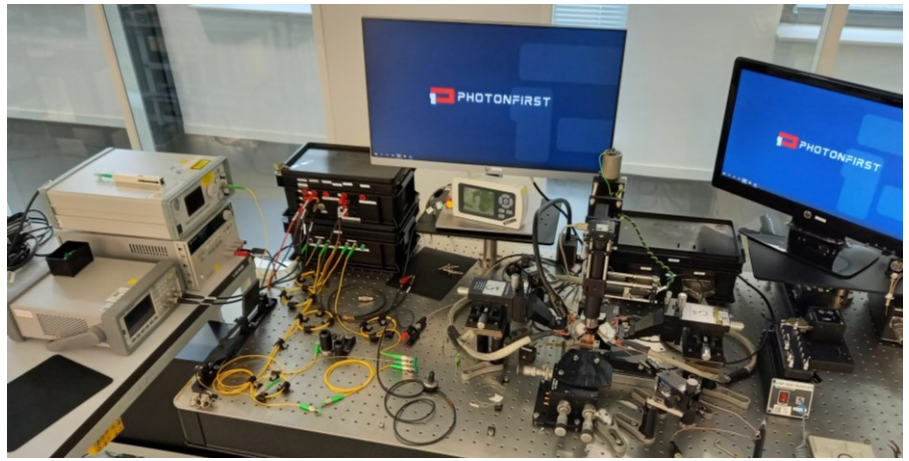






- From building blocks to overall integrated design
  - Foundry specific, design rules
- Be specific in what is new (ASPIC), requires testing
  - Aggregation of functions / Building blocks
  - Actual performance of building blocks for your features/conditions of interest
  - Design for testing / demonstrator packaging

- Generic test packages, ADC/DAC modules
- Test benches for opto-electronic testing

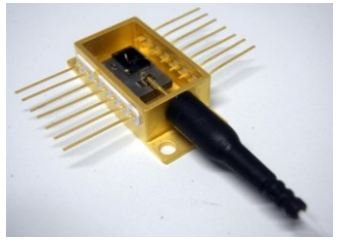


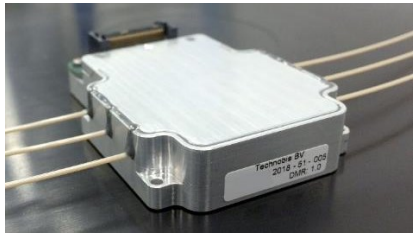
From demonstrator to prototype (TRL 5-6)

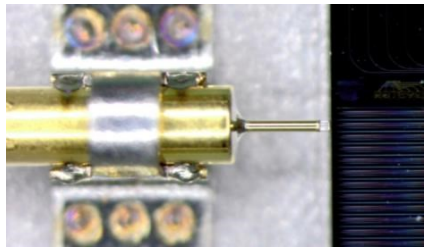
Selecting/developing the right package

- Connectivity
- Protection

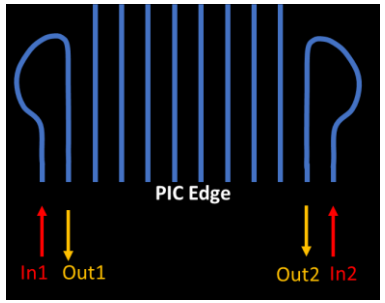
Requirements ↔ Specifications
Generic ↔ Tailored

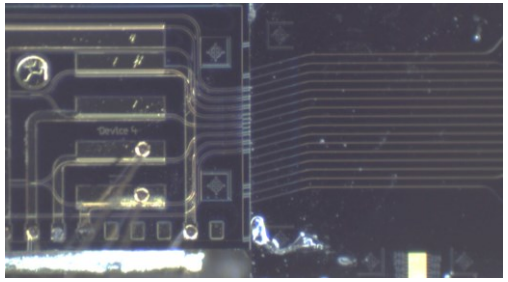




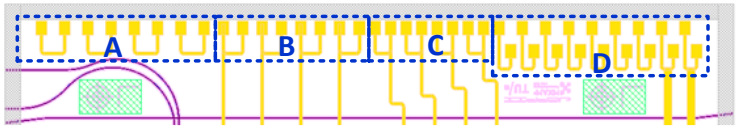


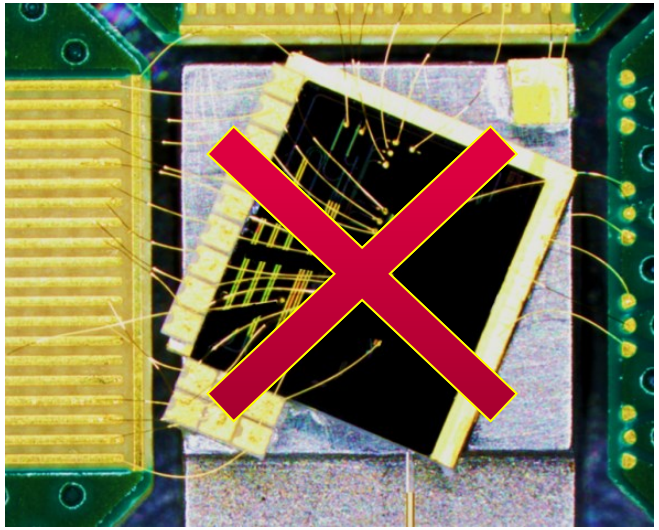
Design for assembly and test





Design the chip/package with the package/chip in mind!





Prototype and pre-series (TRL 5-6)

Complete system in housing, tested in laboratory or simulated environment

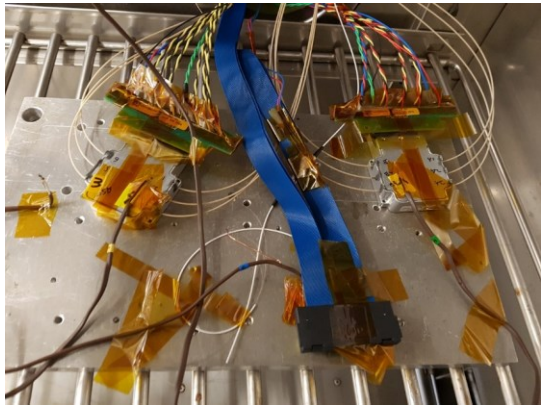
DO-160 Environmental tests

Extensive test campaigns conducted on

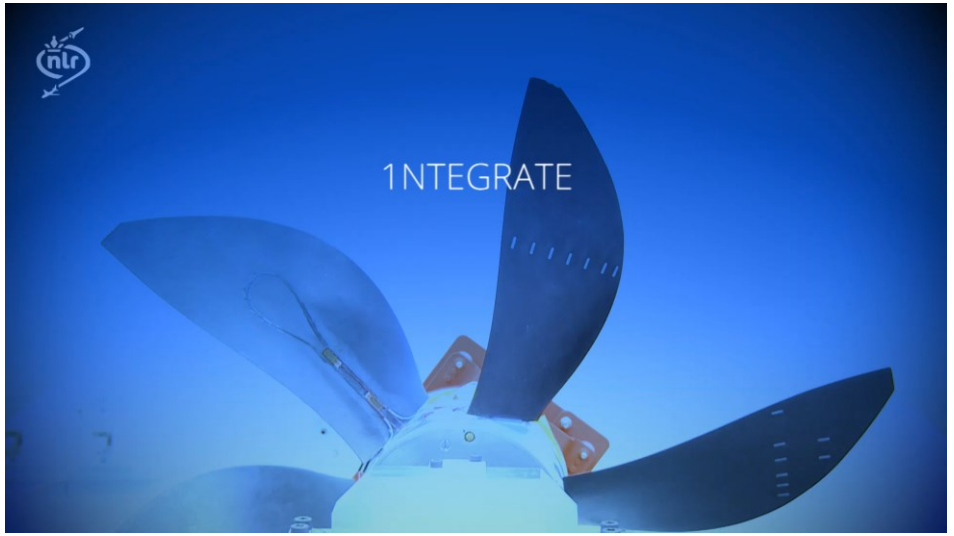
- Chip level (lifetime, ESS, functional testing)
- Package/module level
- System level

Industrial, MIL, DO-160 test categories, HALT

Proton radiation tests on PIC Interrogator modules

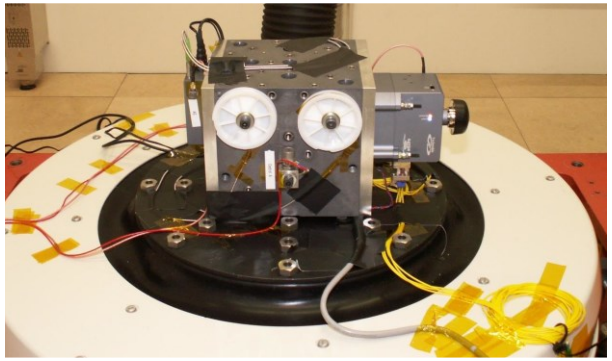


Damp heat climate test chamber



Blade monitoring application example, using a gator system equipped with ext. sync option

(Courtesy NLR, 1ntegrate)

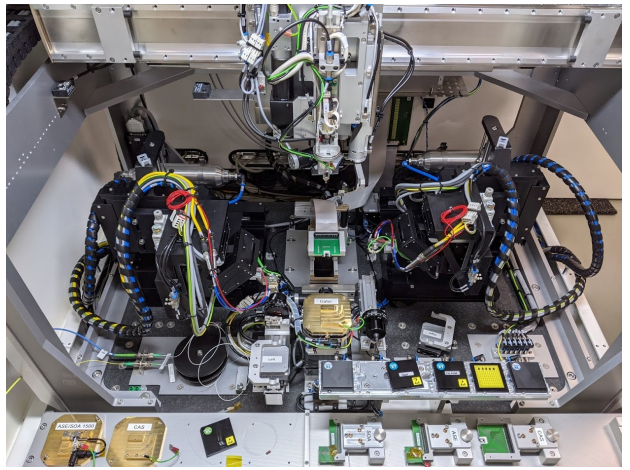


Vibration & shock testing systems for rotorcraft applications

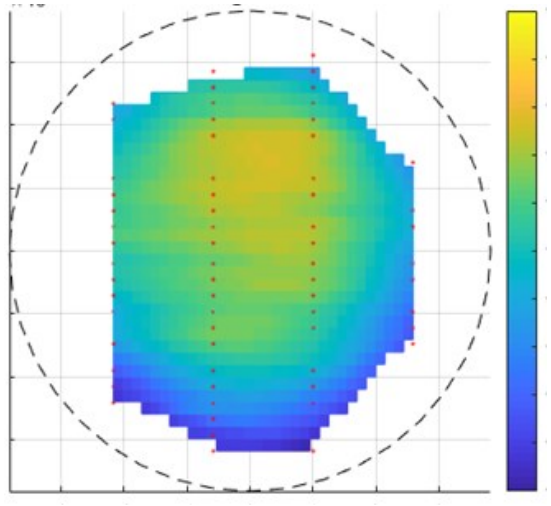
Product(ion) optimization (TRL 7-9, MRL)

- "One functional PIC, does not mean having product yet!"

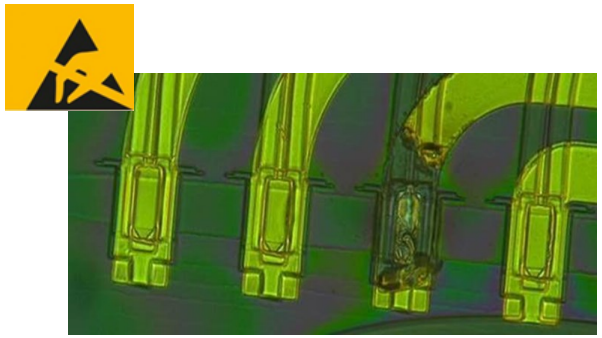
- Valuable data from production and process for end-use, design, fab
  - Fabrication tolerances, yield
  - Production control, process KPIs
  - Statistical analysis and optimization of all related production steps
  - Validation on chip, package, system



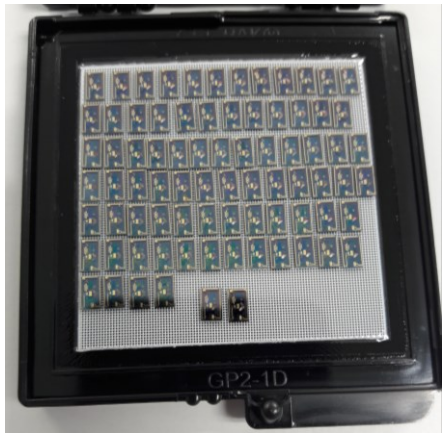
Automated Die-tester at PhotonFirst



Map of measured central wavelength (KPI) distribution of a structure across wafer position.



ESD damage on PIC Photodiode

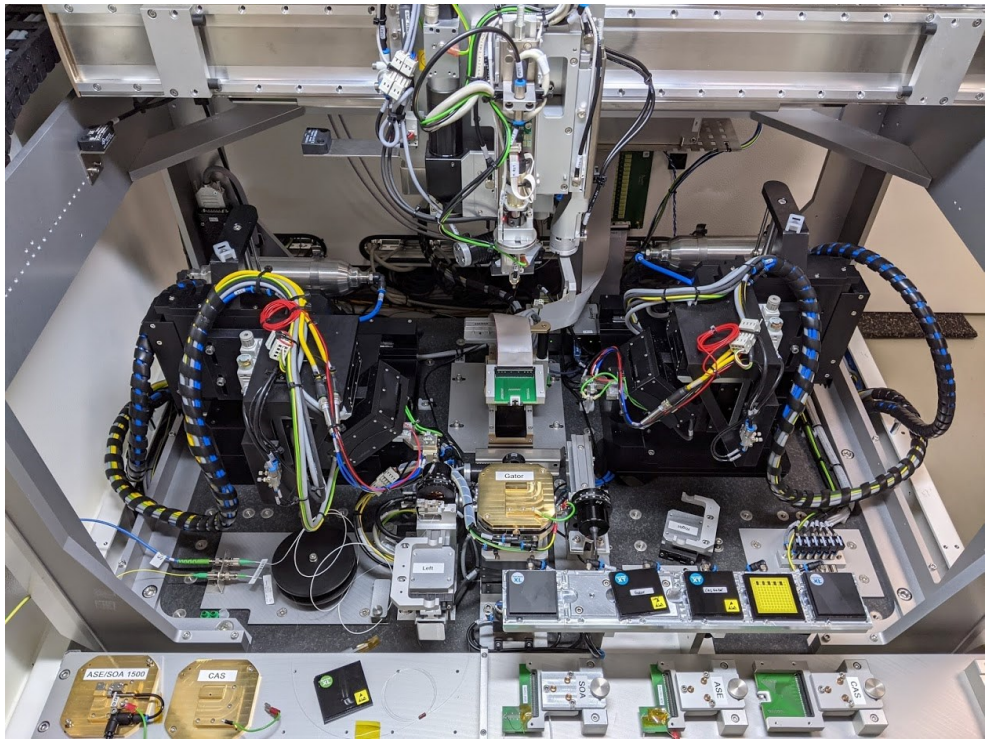


Production PIC batch in gel-pack

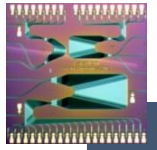
Volume PIC Testing

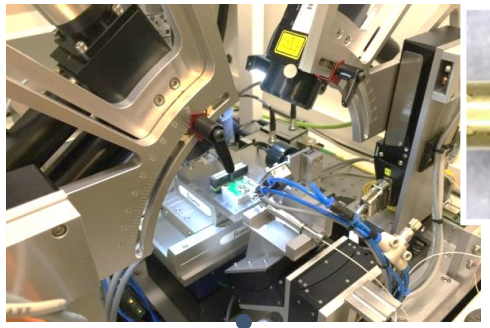
- Test facility for full opto-electronic characterization, testing, qualification

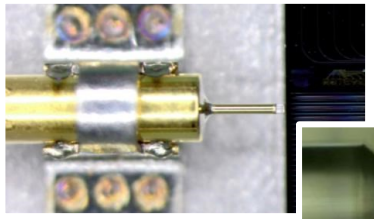
- Full die-testing process automated for volume production PICs

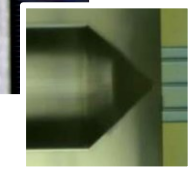


Standardized PIC packaging capabilities

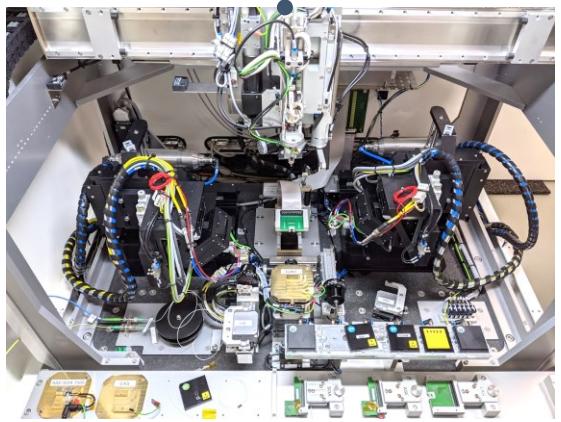


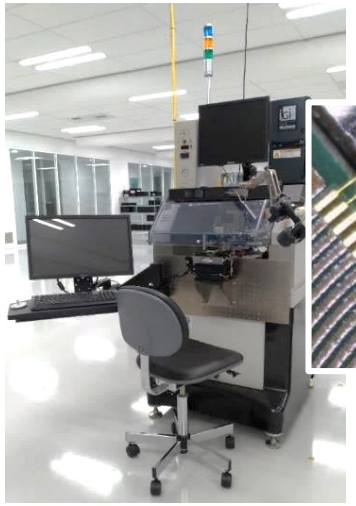


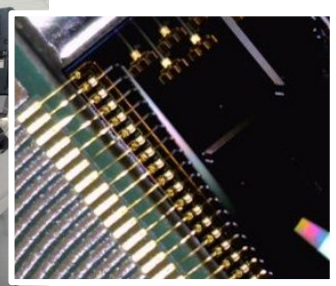




PIC Inspection → Die-bonding → Wire-bonding → Fiber-bonding → System Integrat







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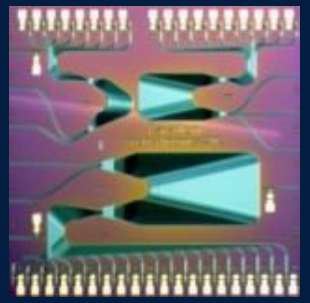

JePPIX Demonstrator Open Call

Take advantage of funding available through our Demonstrator Open Call.

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Submit the form to receive more info

JePPIX Pilot Line

Unleasing Indium Phospide PIC Technology

Design, manufacturing and testing services for pilot production

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