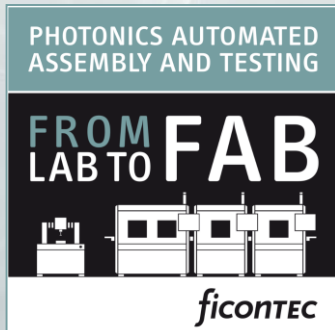


MANUFACTURING MADE LIGHT

Solutions for integrated photonics. Built to scale.

ficonTEC
photonics assembly & testing

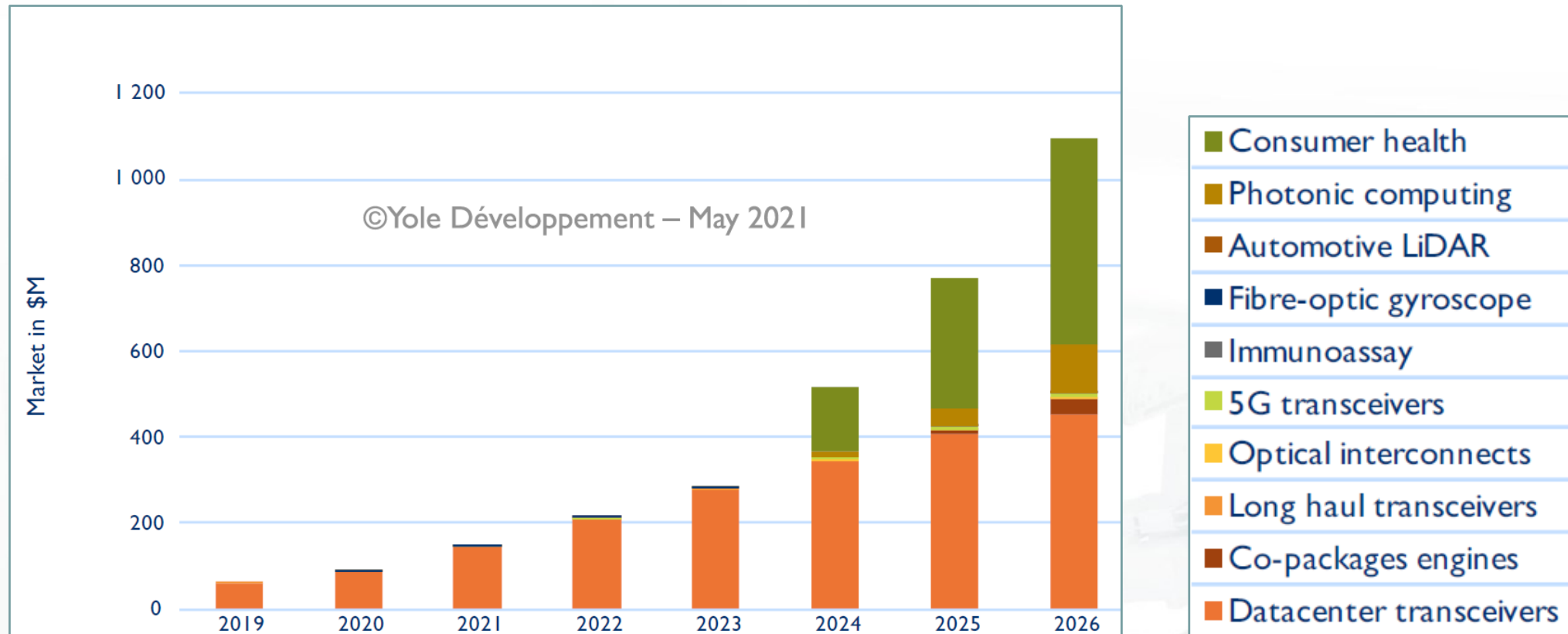


Challenges and Strategies for High-Volume Manufacturing and Testing of Co-Packaged Optics

**Augusto Mandelli, Sales & Service Director
ficonTEC Service GmbH**

EPIC Meeting, PIC Post Processing & Packaging
LWoP 2023 – June 29th, 2023

Integrated Photonics Device Forecast



Source: Yole - Special report on Silicon Photonics 2021

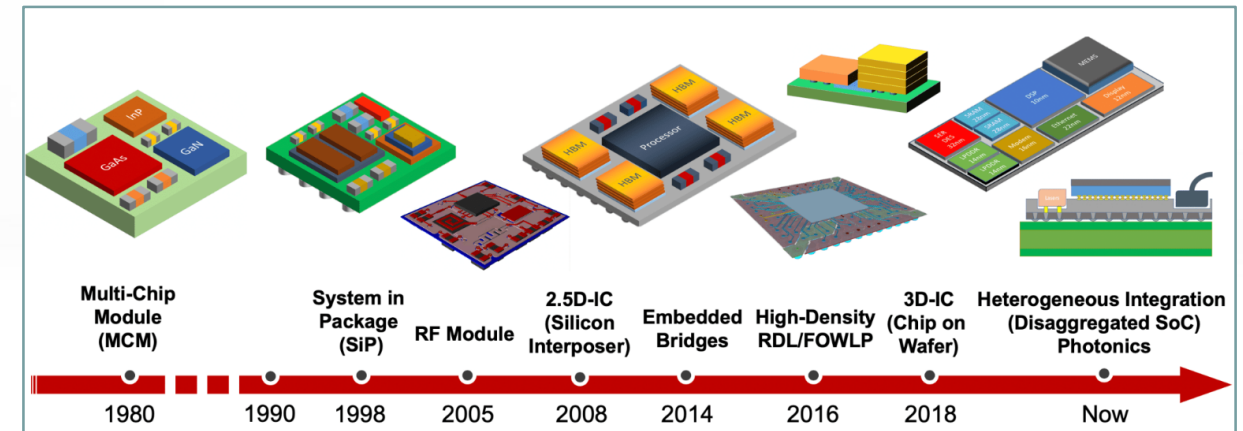
Semiconductor Evolution a Success Story

Micro-electronics has seen continued evolution since the 1960's/1970's

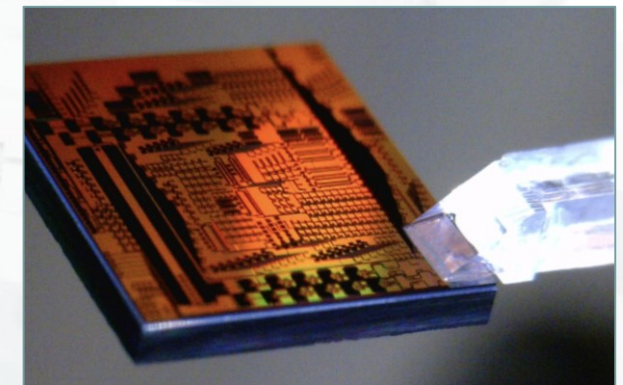
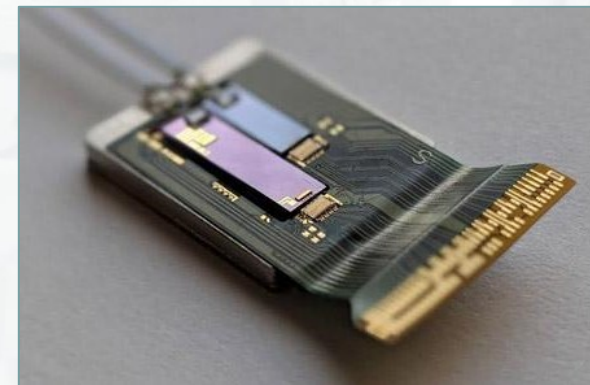
Today, ever more complex and powerful devices are all manufactured cost-effectively at wafer level. Some also now incorporating photonic elements...

Fully integrated photonic devices are the equivalent to ASICs for micro-electronics.

Photonics is today riding the same generational transition to 'micro, hybridized, integrated & monolithic'. But 35-40 years later ...

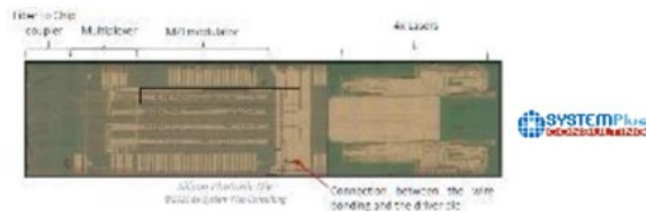


Source: Cadence



Die vs. Packaging, Assembly and Test Cost

Optical Transceiver



The Si photonic die (Intel, including laser)

Die Cost: \$10

Die Price



The Si photonic die (Intel, including laser)

Die Price: \$17

In communication packaging assembly and testing are a major % of the final systems ASP more than 80%. It is because of the need for high performance, fiber alignment...



System Price

Intel CWD4 transceiver (end-system)

Transceiver retail price: \$150

Consumer Health

ASP used in forecasts



The Si photonic die (including laser)

Die Price: \$18

In consumer, assembly and testing are less stringent compared to communication (contact measurement). The ASP delta between die and system is from higher margins.



Smartwatch retail price: \$699+

Source: Yole - Special report on Silicon Photonics 2021

HVM in Photonics Assembly is not a new Thing



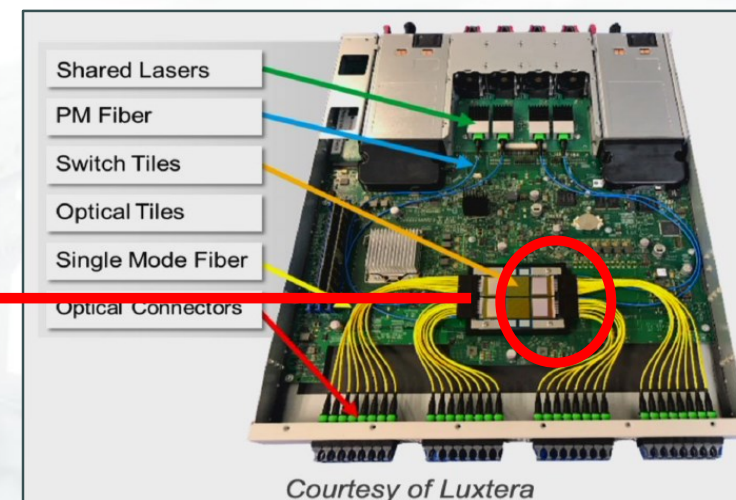
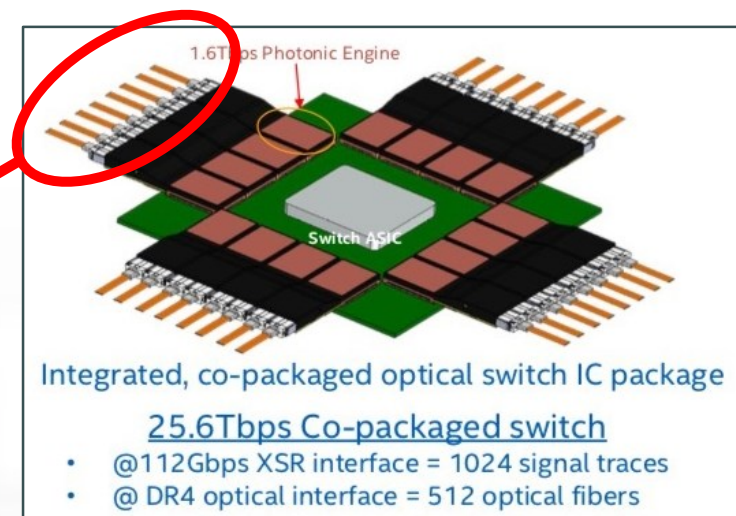
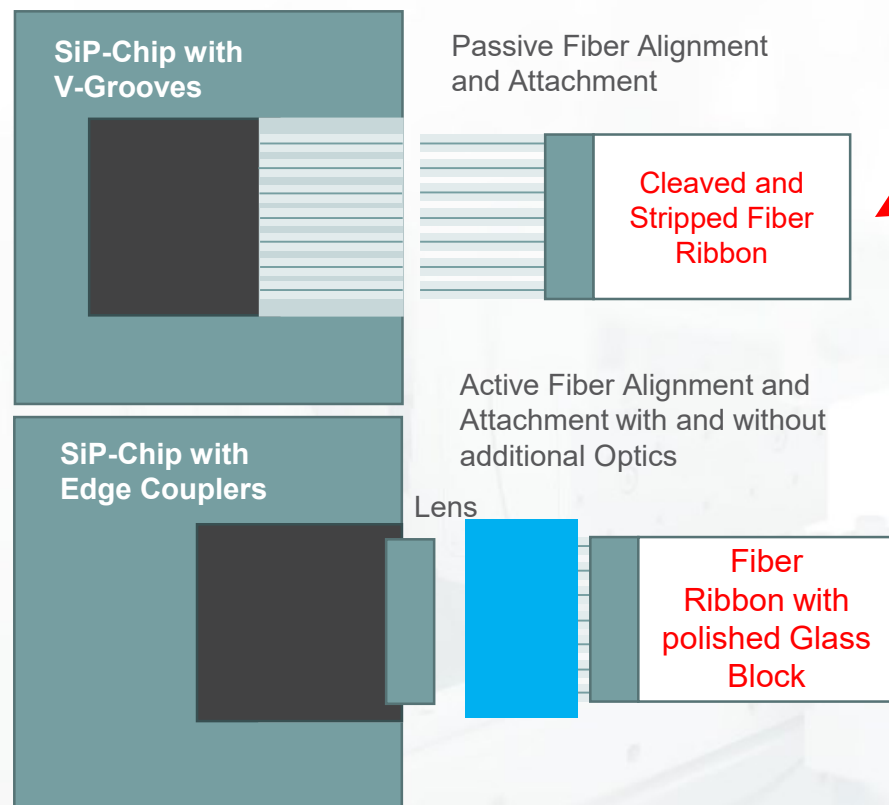
Optical Air purity sensor for a German Tier 1



Mass production site in Thailand with over 150 machines, incl. automatic module handling (cassette to cassette)

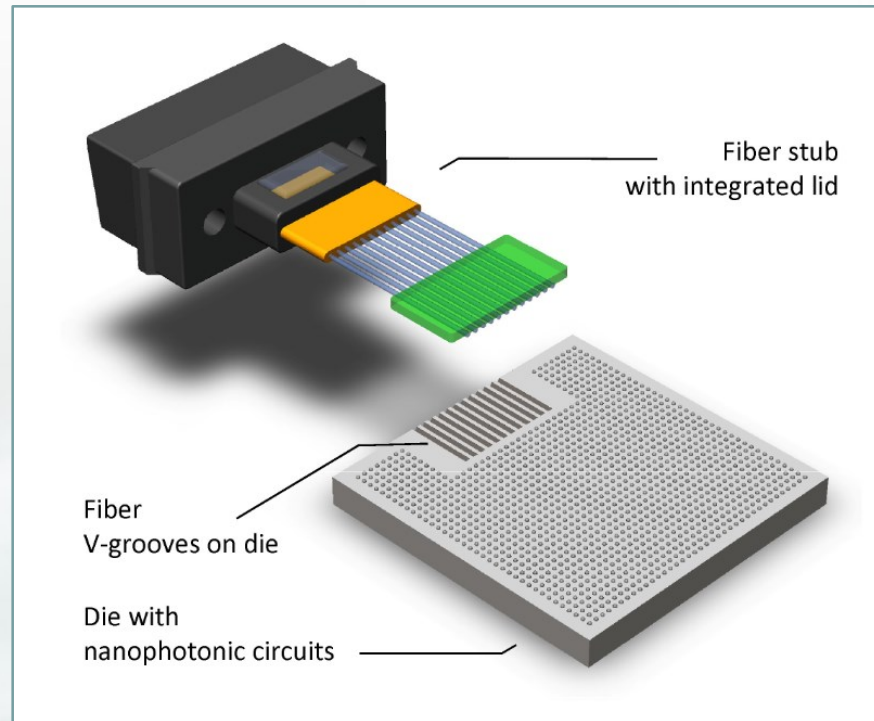
Assembly Strategies in Co-packaged Systems

Active vs Passive Assembly



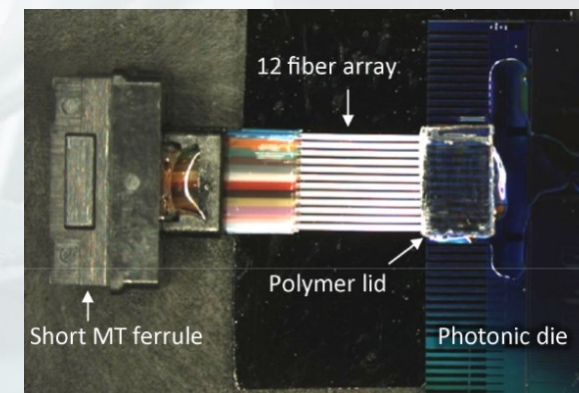
Source:
https://community.cadence.com/cadence_blogs_8/b/breakfast-bytes/posts/the-photonics-summit-2019

Passive Ribbon in V-groove Placement as an Example



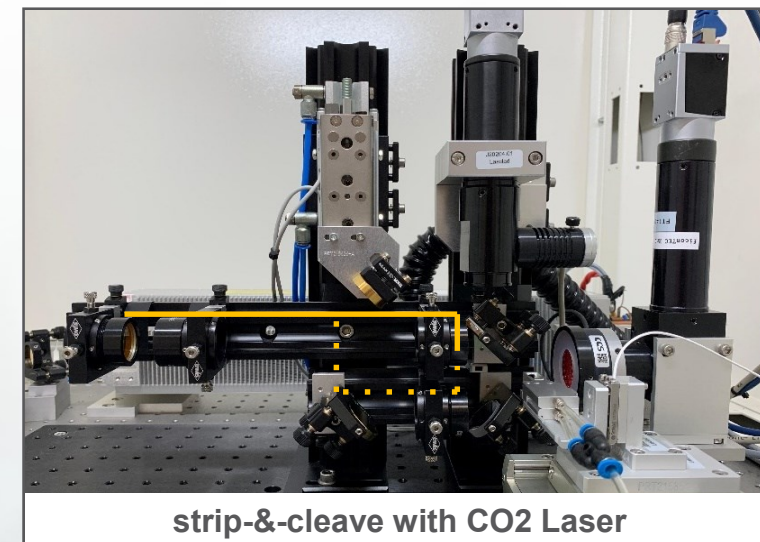
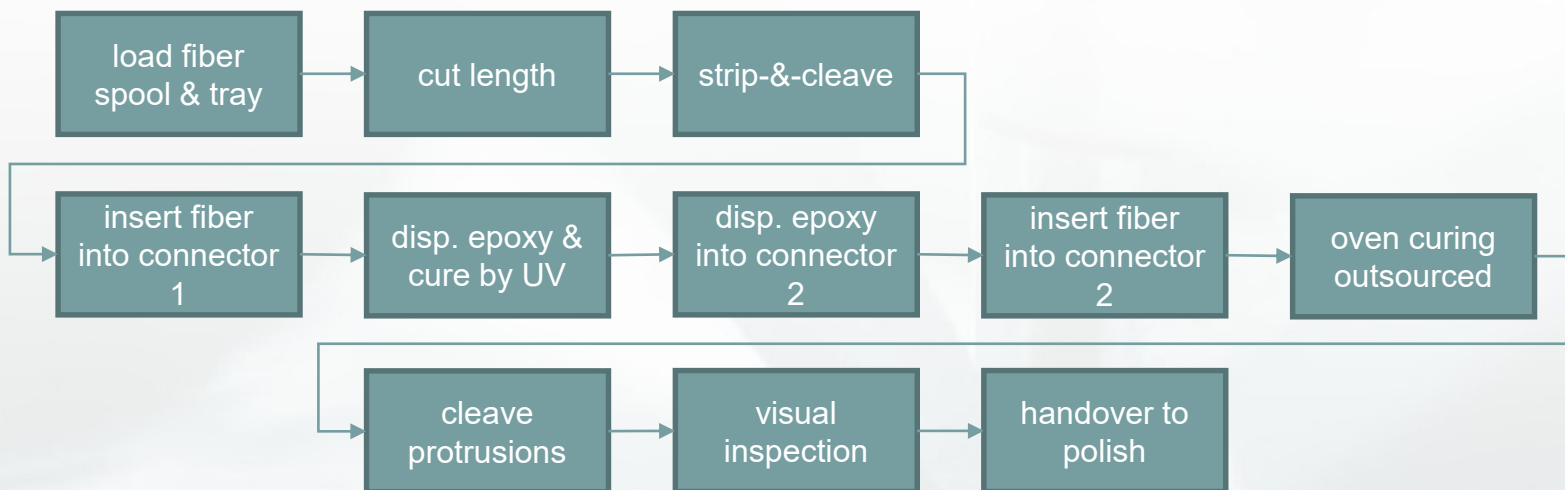
<https://researcher.watson.ibm.com/researcher/files/us-tymon/p329.pdf>

- Etched v-grooves in PIC
- V-grooves match to waveguides
- Insertion of fiber arrays
- Passive process



Automated, self-aligned assembly of 12 fibers per nanophotonic chip, T. Barwicz et al., ECTC 2015

F1600 – Fiber preparation workflow



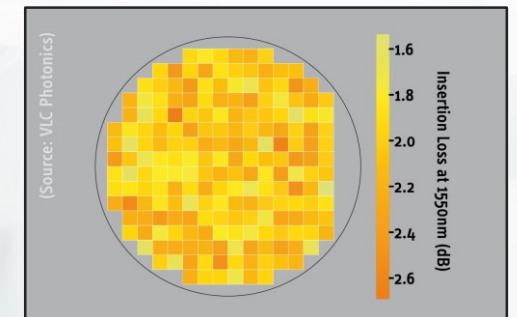
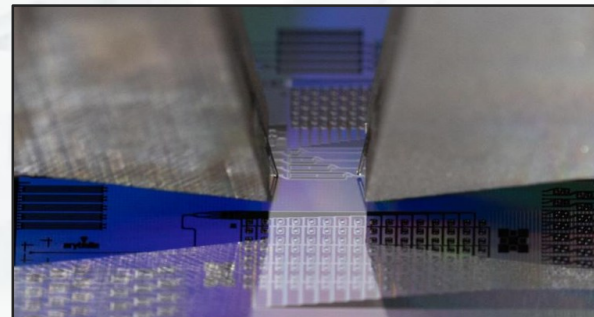
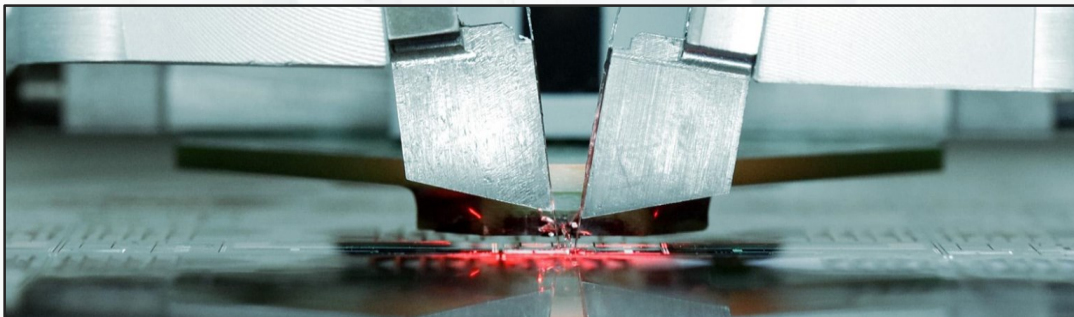
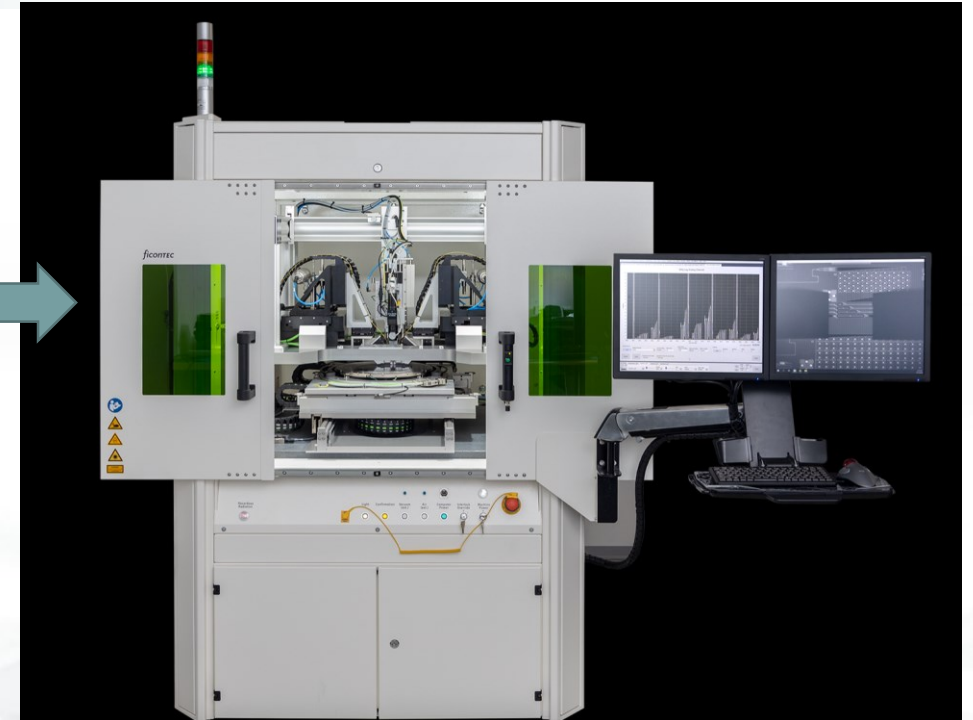
FIBERLINE

Automated Fiber Ribbon Insertion

Wafer-level Test – Transition from 2018 to 2022 (and beyond)

Overview of Photonics Handling and Test Demonstration

- Overall test solution
 - ficonTEC integrated prober and test system
 - Optical test performed by Coherent Solutions
 - 200 mm photonics demo wafer with optical waveguide and grating coupler
 - Capable of electrical and optical test
- PXI products highlighted
 - Tunable laser source
 - Optical switches
 - Optical power meters
 - Optical signal analyzer (OSA)



WAFER TESTLINE

Fully Automated Wafer-level PIC Test Systems



- 4-64 Channels
- Alignment in etched trenches
- No grating couplers necessary
- Basically wavelength independent
- Mode size can be adjusted to PIC

29.06.2023

- Lowering the overall “cost of test” is paramount to scale production & adoption up
- HVM is nothing new
- The photonics industry is still far from the level of standardization of the electronic industry; collaboration and standardization efforts at all levels is a must

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Thank you