LUCEDA PHOTONICS

# PDKs of the future – Enabling a modular design ecosystem

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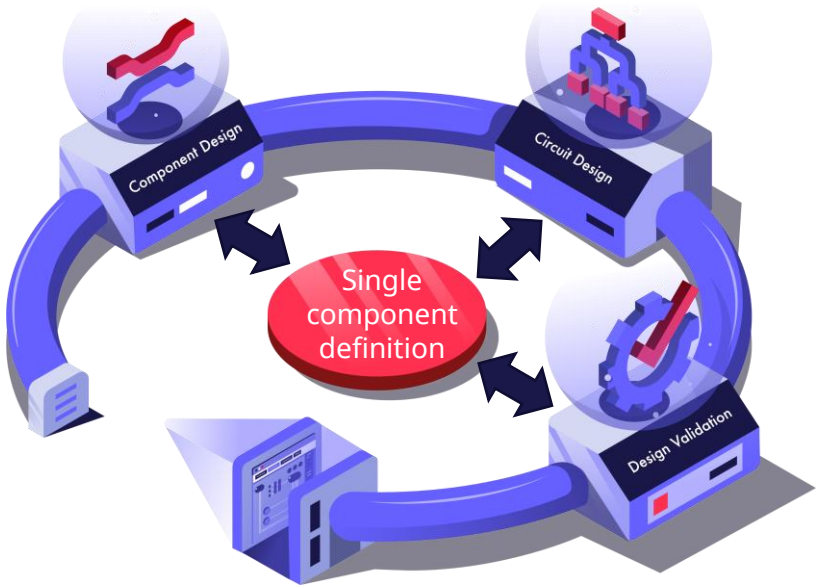
EPIC TechWatch - ECOC

# Luceda Photonics

python powered

"Help photonic IC designers enjoy the same **first-time** right experience as electronic IC designers"

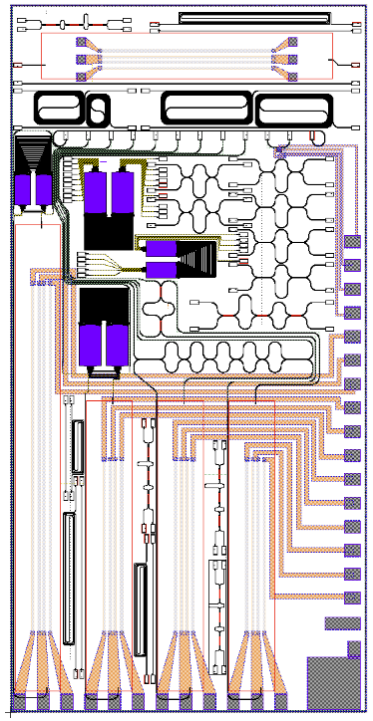
## IPKISS Photonics Design Platform



# Level 1

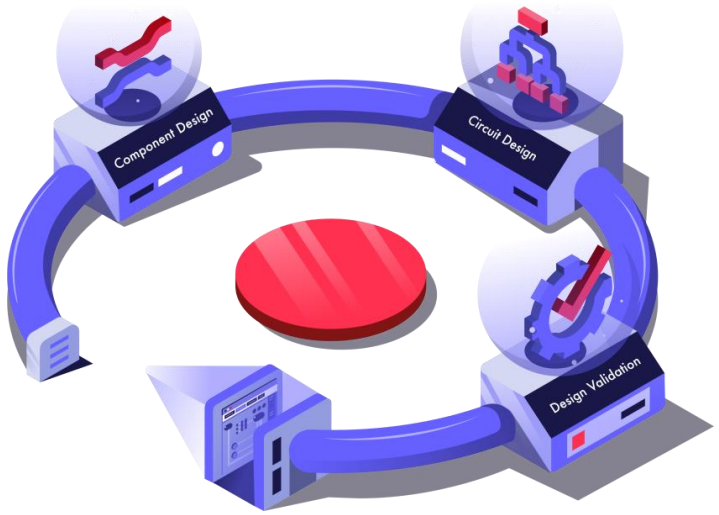
1 Designer

1 Foundry



1 Design

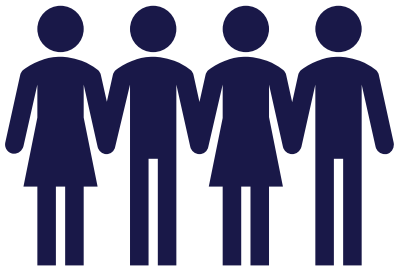
# IPKISS *PDKs*




- Power of IPKISS: layout + models + simulation
- Python-based PDK for maximum flexibility
- Automated testing and quality assurance
- Export to OpenAccess, iPDK, uPDK standards
- Vast offer of PDKs from around the world

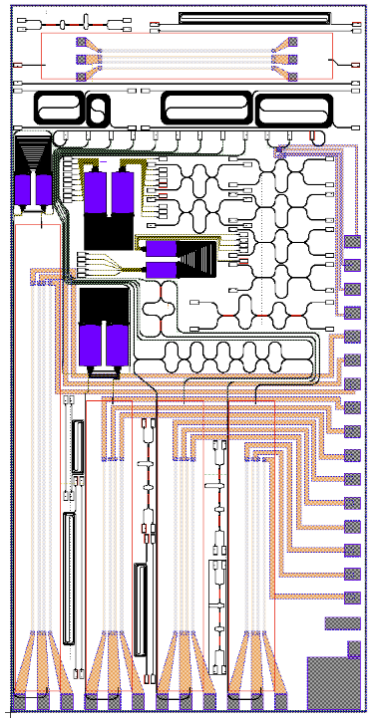
python powered

# Level 2



Design team

1 Foundry

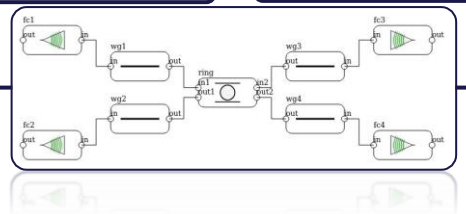


1 Design

# What are our customers doing?

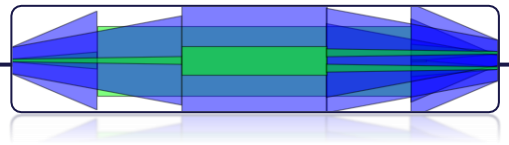
## Optical circuit IP creation

- Parametric cells (PCell)
- Circuit design
- Circuit layout
- Circuit simulation
- Simulation analysis
- Mask assembly & prep (DRC clean)



## Optical device IP creation

- Parametric cells (PCell)
- Device layout (artwork)
- Device simulation (camfr / others)
- Compact model generation
- Simulation recipes

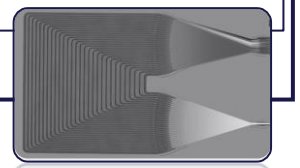


## IPKISS PDKs

imec, amf, leti, SiEPIC, CompoundTek, LIGENTEC, pix4life, imec, tower, SMART PHOTONICS, Fraunhofer HHI, Tyndall, UMEC, VTT, AIM PHOTONICS, SILICON, SITRI

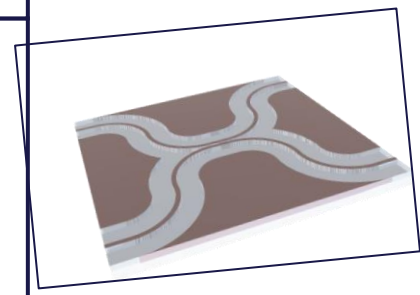
## Optical IP toolboxes

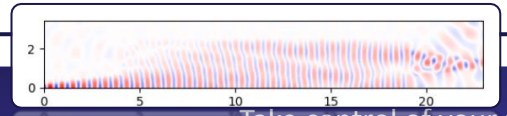
AWG Designer



## Device simulation

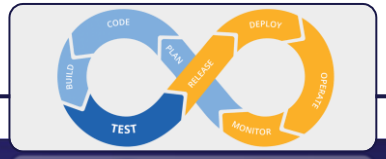
- Camfr (EME)
- Custom-built links
- Link with Ansys Lumerical
- Link with CST Studio Suite (Dassault)



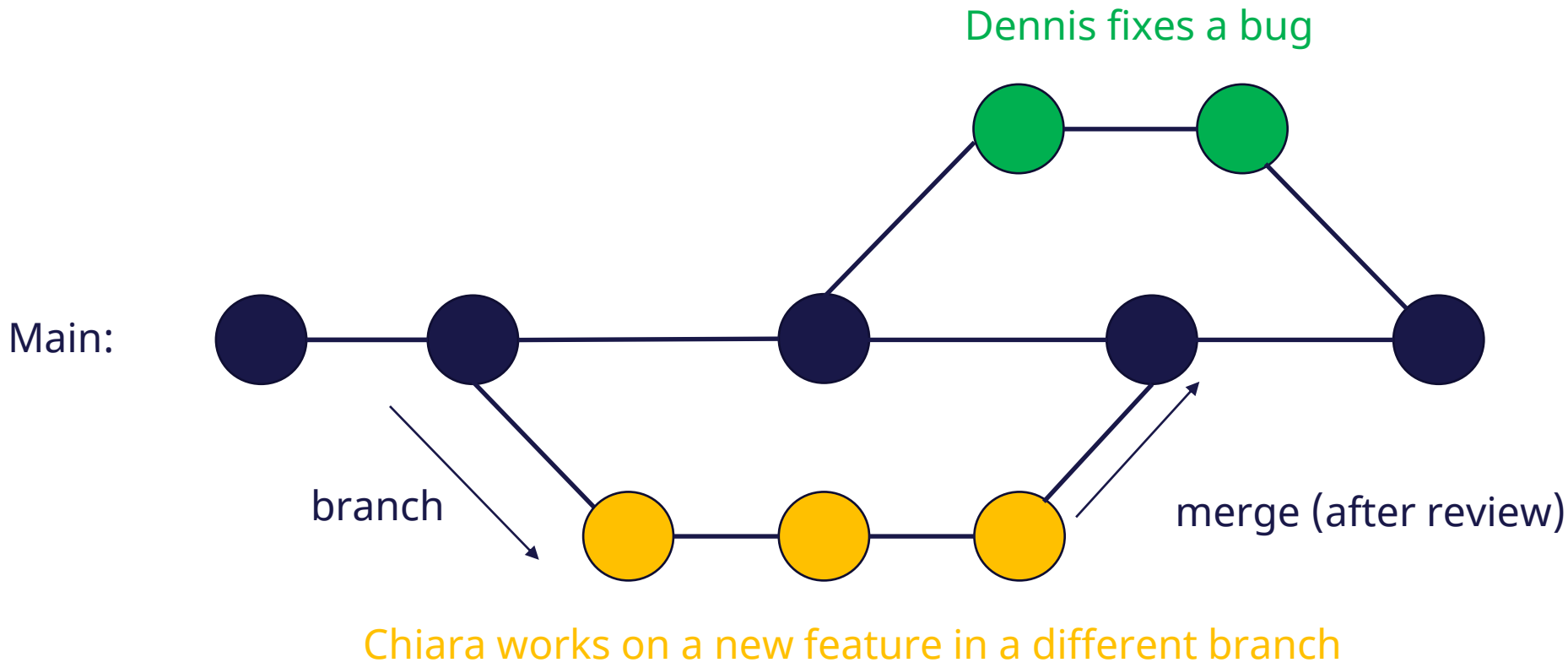



## QA, IP maintenance and infrastructure

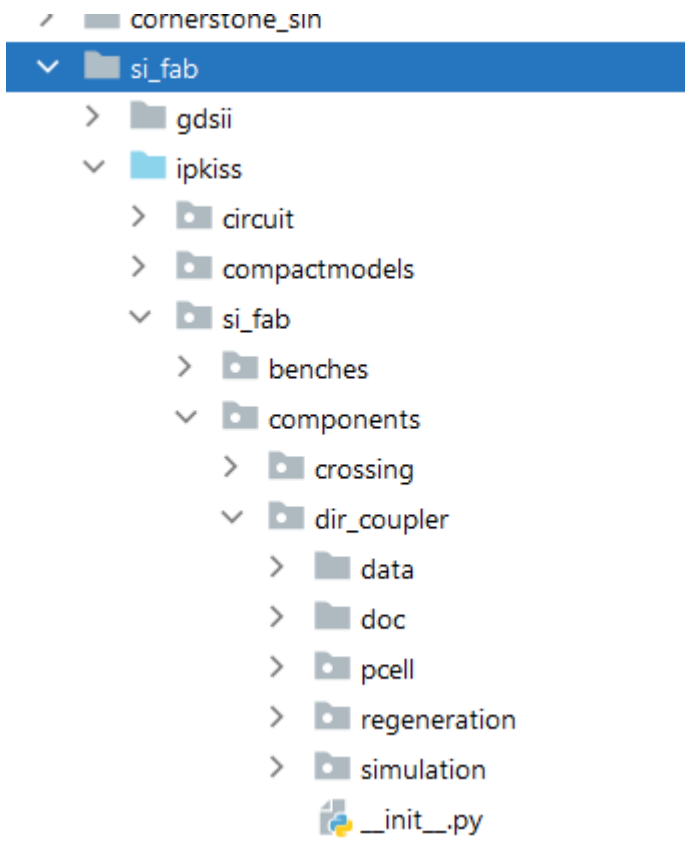
- Set up test suites
- Test reporting
- Automate testing
- Set up documentation
- Maintain infrastructure

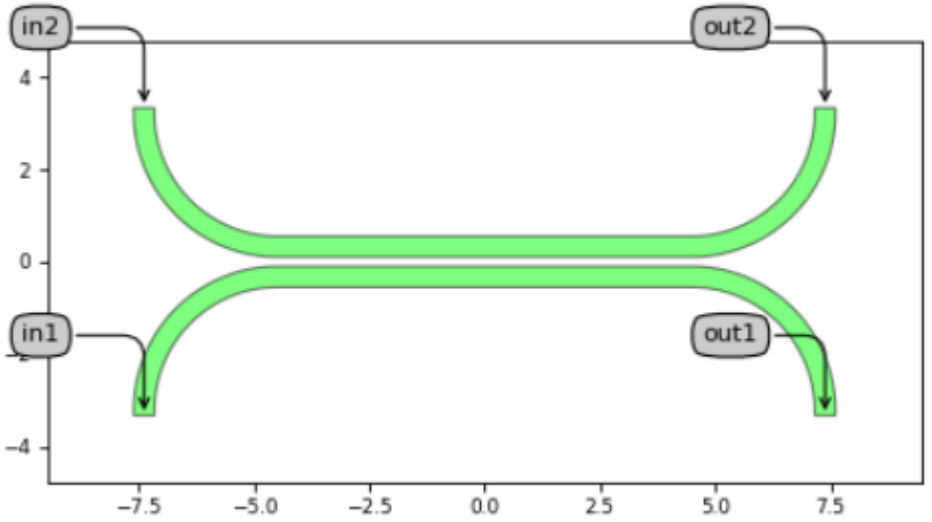


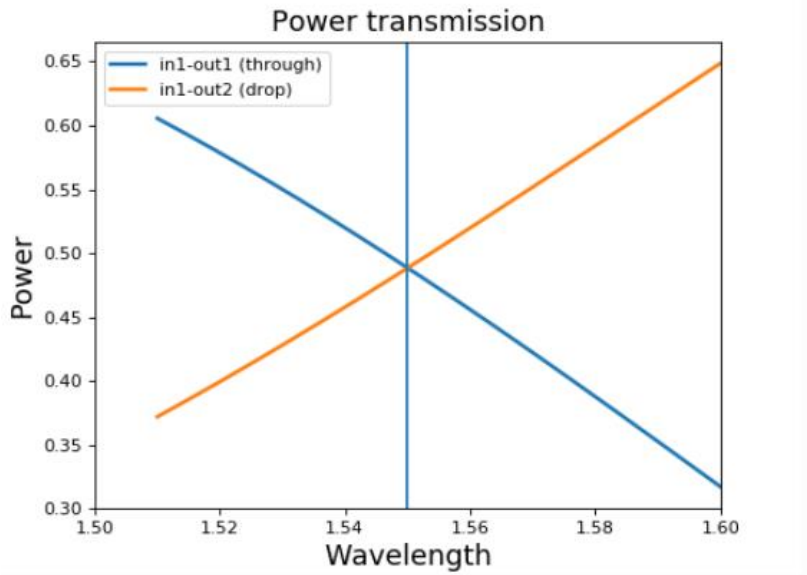
# Version control



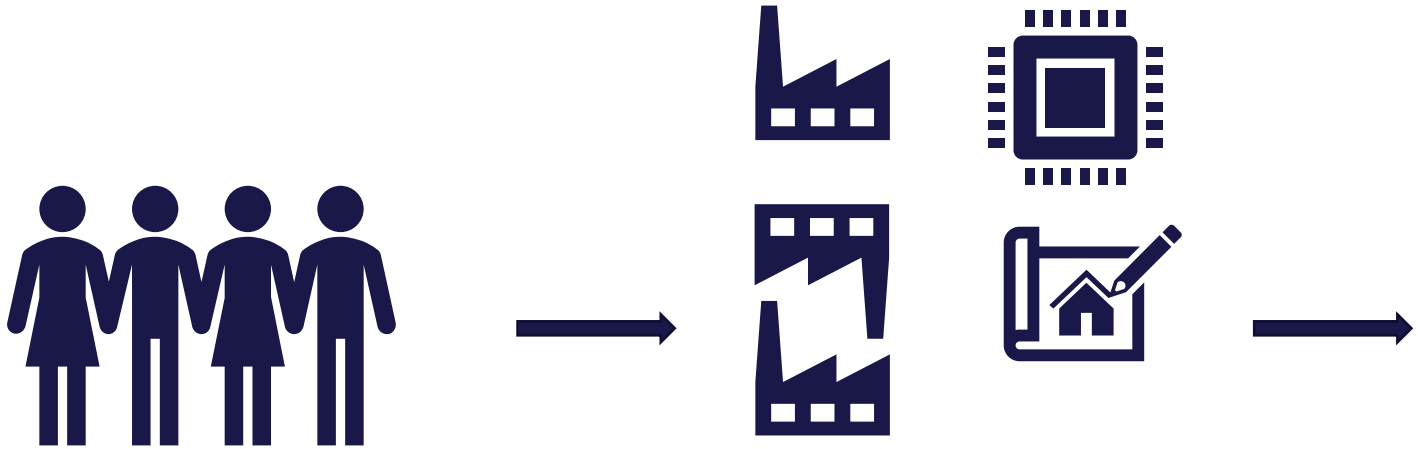
# Example – Directional coupler



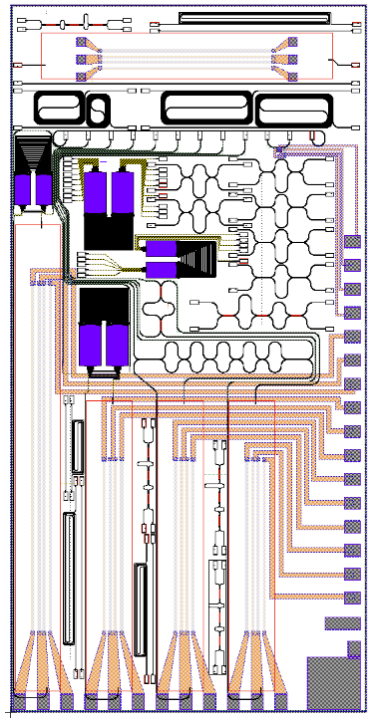



# Level 3

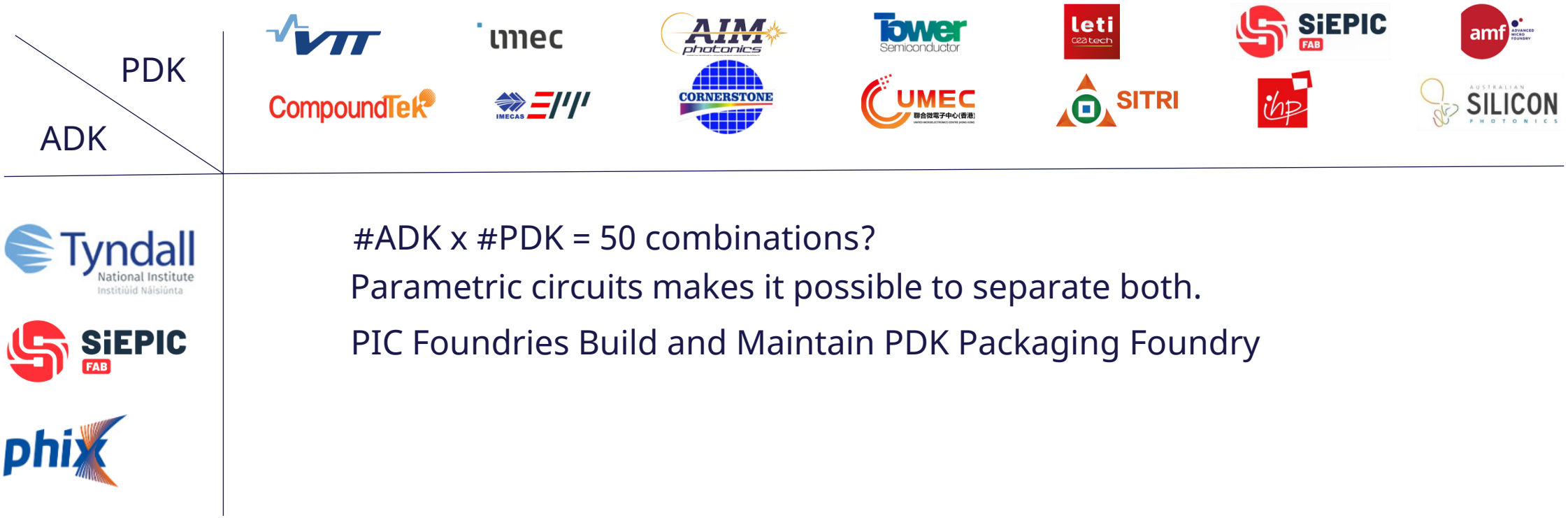


- Packaging Foundries
- Interposers
- Design Houses
- Heterogeneous Integration



# PDKs and ADKs

```
from si_fab import all as pdk
from tyndall_packaging.all import UniformPackagingArray
```




#ADK x #PDK = 50 combinations?

Parametric circuits makes it possible to separate both.

PIC Foundries Build and Maintain PDK Packaging Foundry

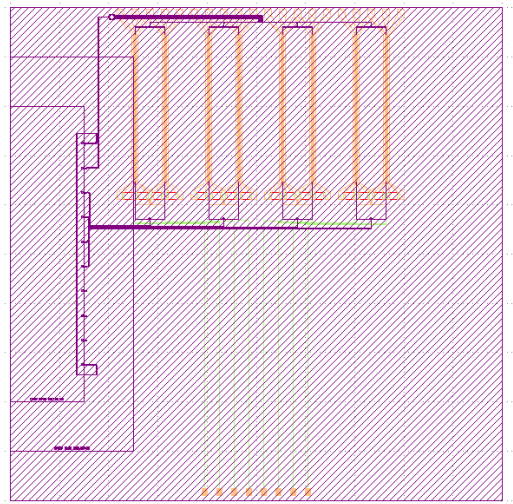
# Conclusion

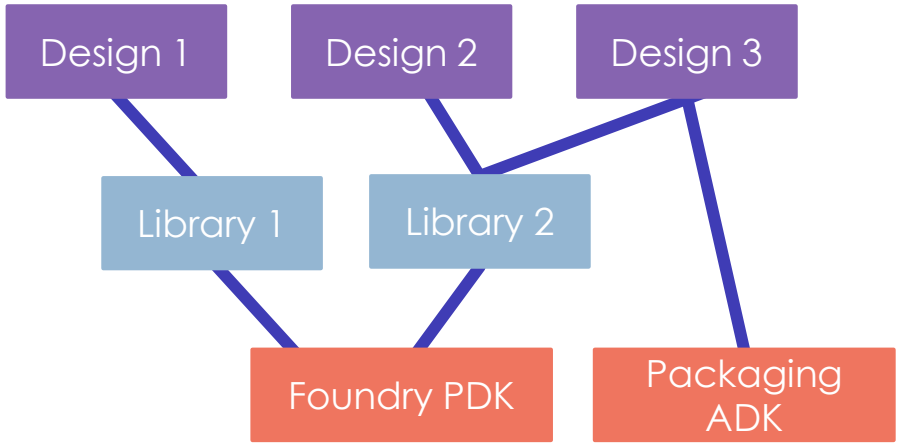
| PDK / ADK | VTT | imec | AIM photonics | Tower Semiconductor | leti | SiEPIC FAB | amf |
|---|---|---|---|---|---|---|---|
| | CompoundTek | IMECAS | CORNERSTONE | UMEC | SITRI | ihp | SILICON PHOTONICS |
| Tyndall National Institute | | | | | | | |
| SiEPIC FAB | | | | | | | |
| phix | | | | | | | |

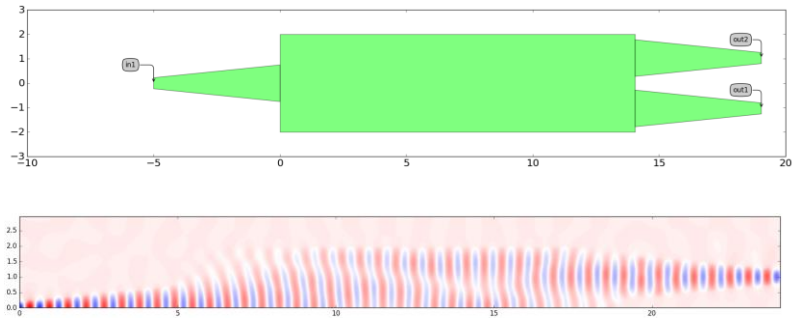
#ADK x #PDK = 50 combinations?

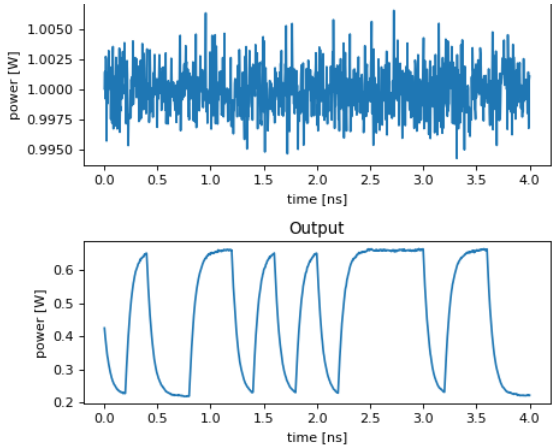
Parametric circuits makes it possible to separate both.

PIC Foundries Build and Maintain PDK Packaging Foundry

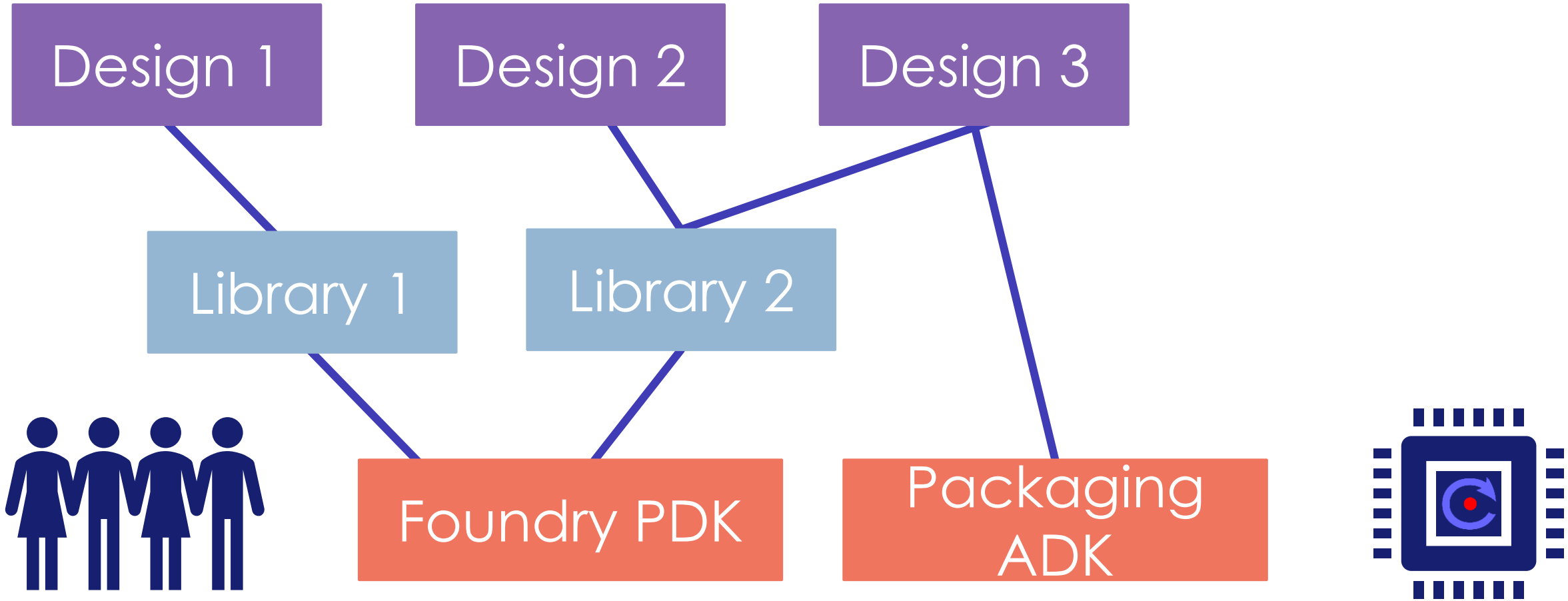




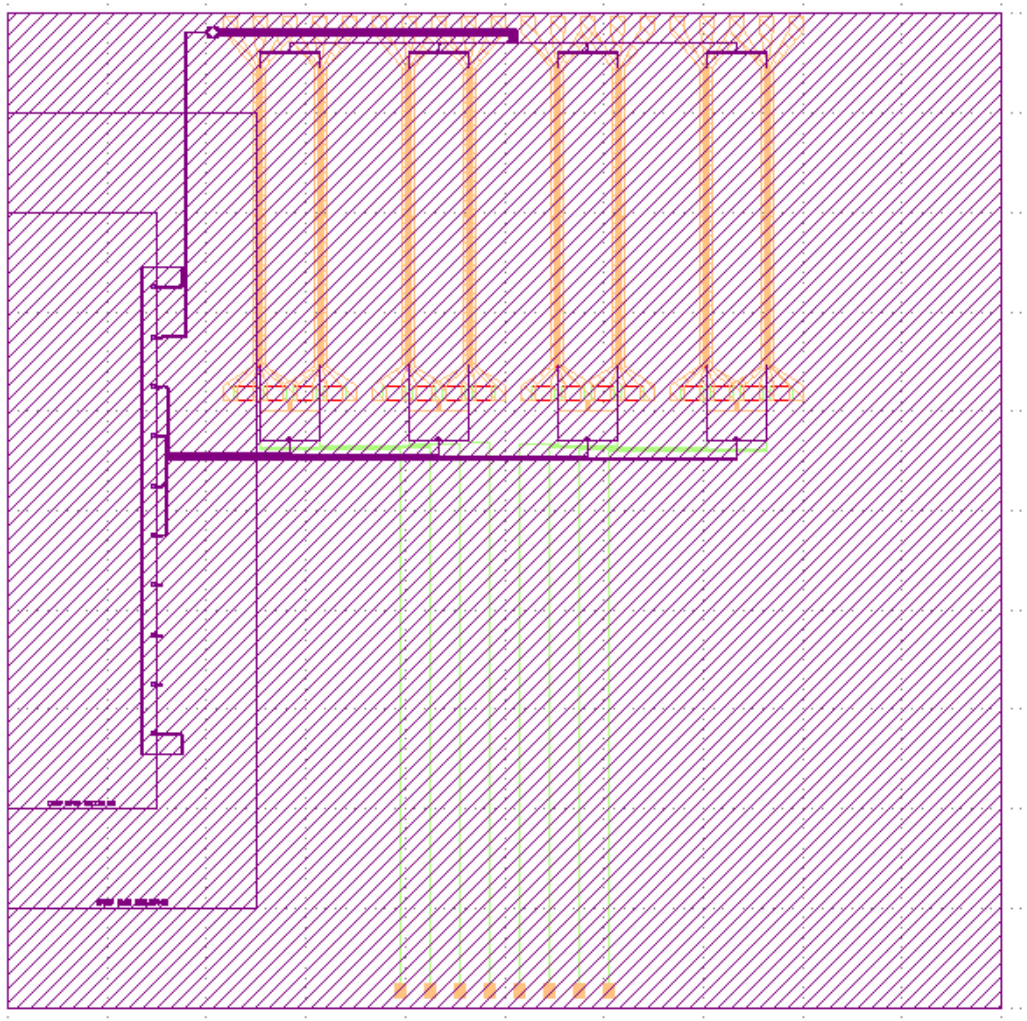



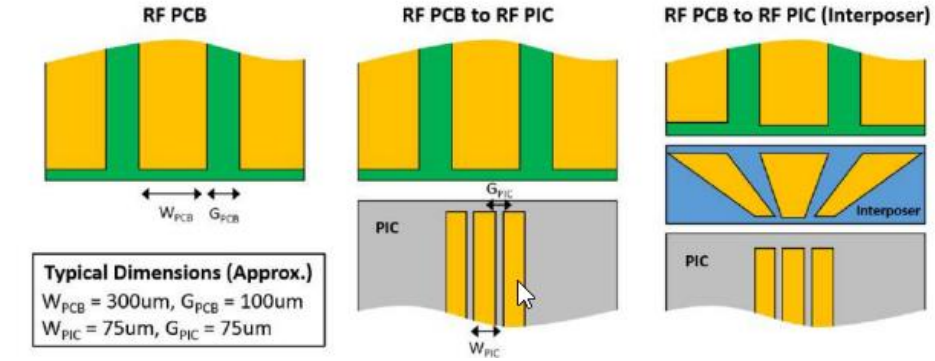


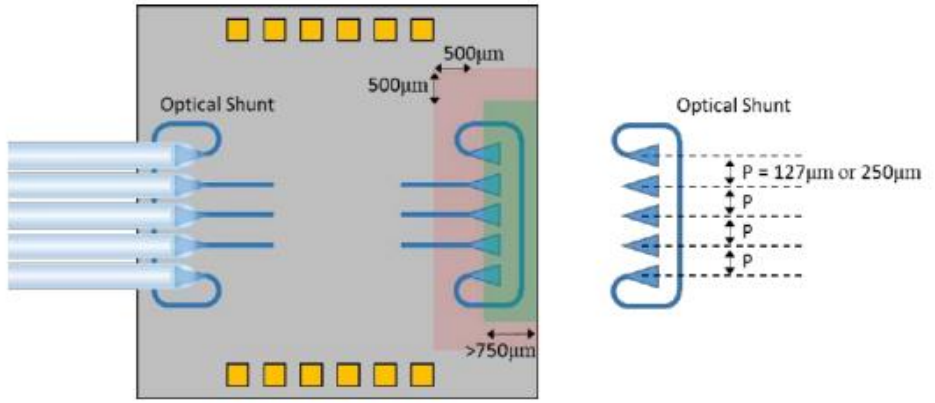
# IPKISS IP Management



# Example 2: Packaged 4-Lane Modulator





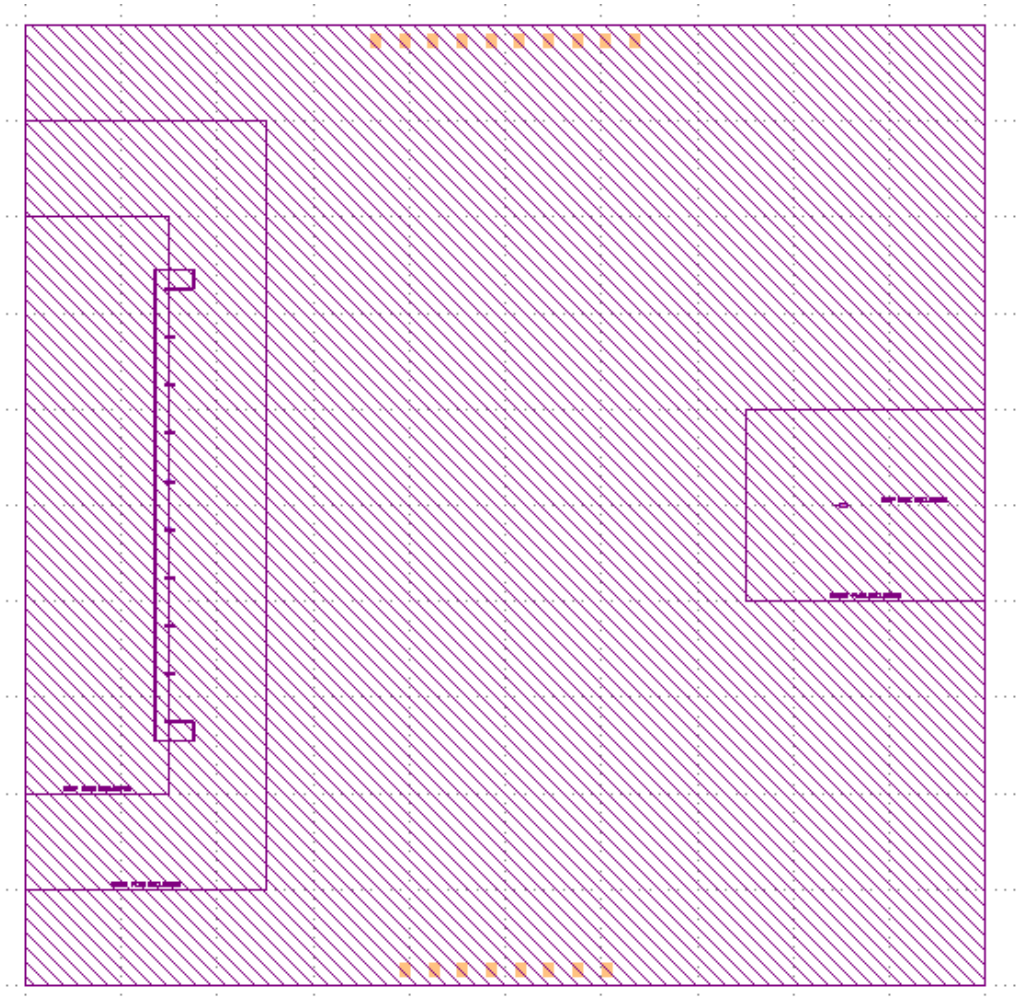




Tyndall National Institute
Institiúid Náisiúnta

# Respect the packing foundry rules

```
from si_fab import all as pdk
from tyndall_packaging.all import UniformPackagingArray

packaging_arrray = UniformPackagingArray(
    n_o_user_west_gratings=8,
    n_o_user_east_gratings=1,
    n_o_north_bondpads=10,
    n_o_south_bondpads=8,
    bondpad=pdk.BondPad(metal1_size=(50, 70), metal2_size=(50, 70)),
    grating=pdk.FC_TE_1300(),
)
packaging_array_lv = packaging_arrray.Layout()
packaging_array_lv.write_gdsii("sifab_chip_package_oband.gds")
```



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from si_fab import all as pdk
from tyndall_packaging.all import UniformPackagingArray

packaging_arrray = UniformPackagingArray(
    n_o_user_west_gratings=0,
    n_o_user_east_gratings=1,
    n_o_north_bondpads=10,
    n_o_south_bondpads=8,
    bondpad=pdk.BondPad(metal1_size=(50, 70), metal2_size=(50, 70)),
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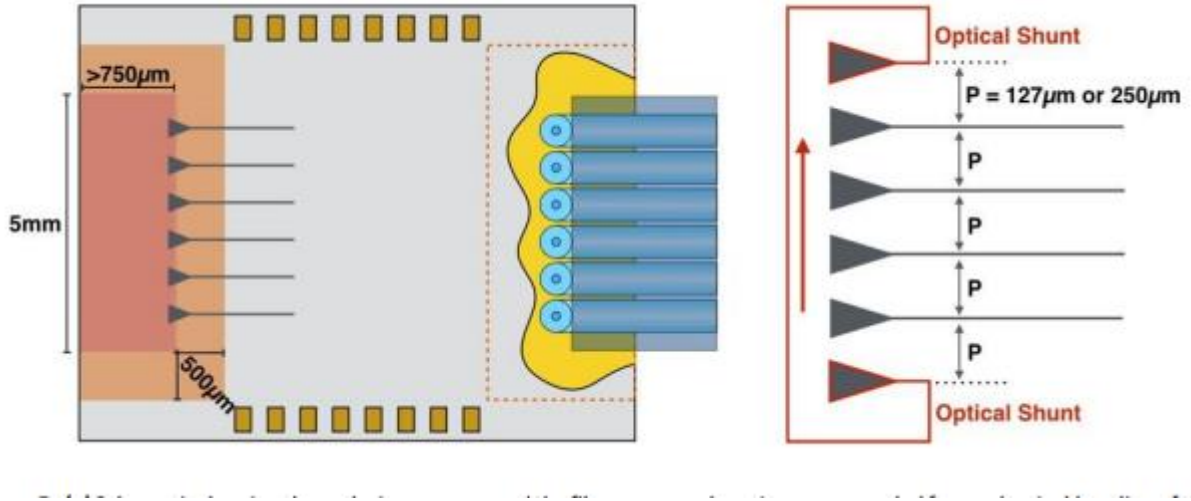


Instance causing the error:
<UniformPackagingArray PCell
'TYNDALL_PACKAGE_1'>
Cause of the error: You can't have only 1 grating on your chip.
Properties causing the error:
n_o_user_east_gratings --> 1
n_o_user_west_gratings --> 0

Process finished with exit code 1

)

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packaging_arrray = UniformPackagingArray(
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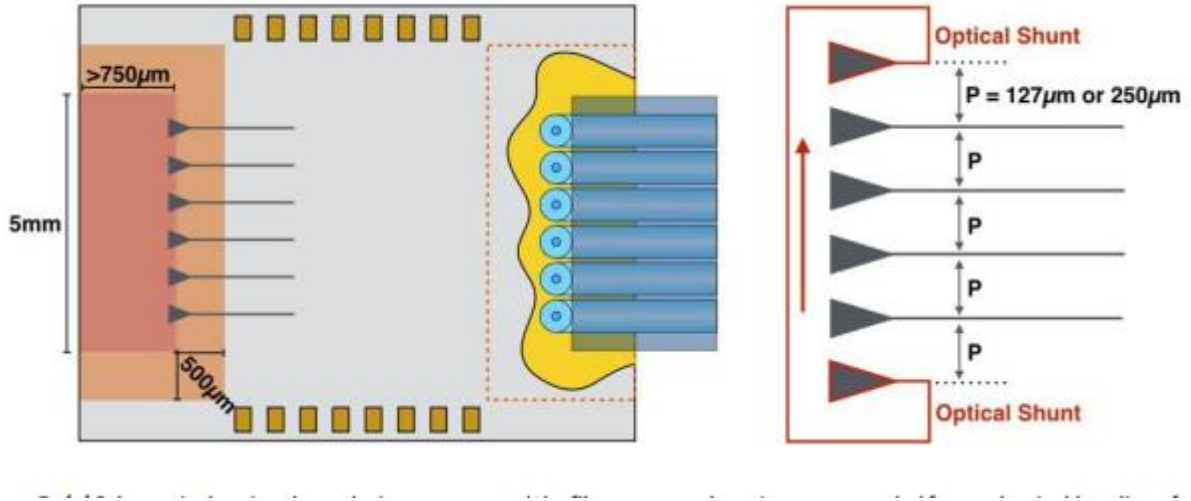


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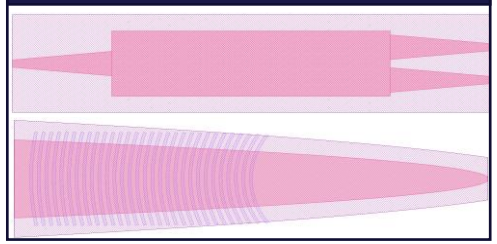
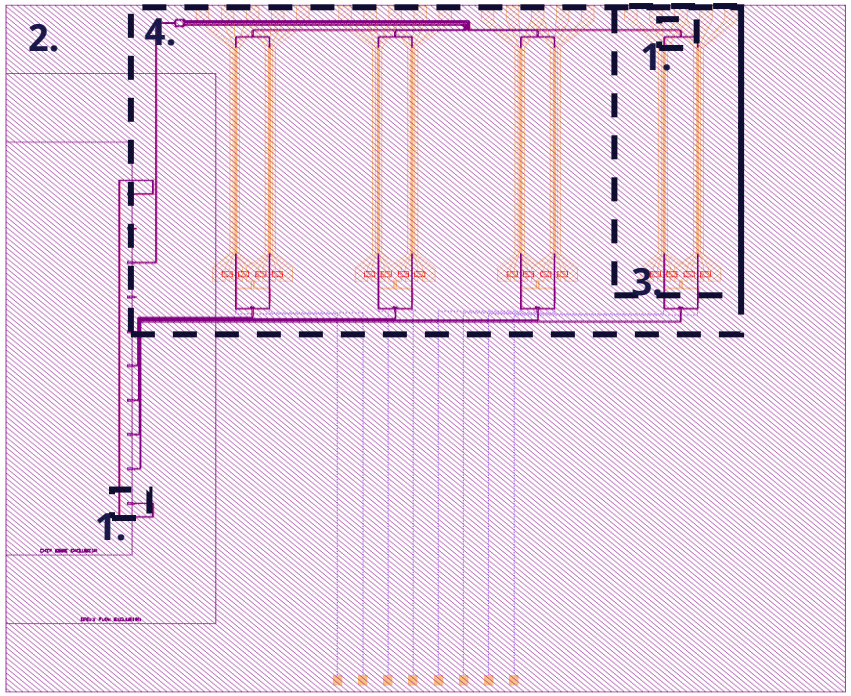
Process finished with exit code 1

# Sources

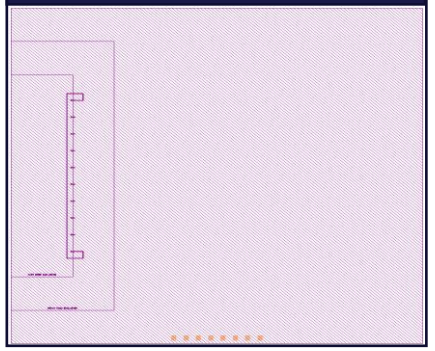
1. SiFab PDK



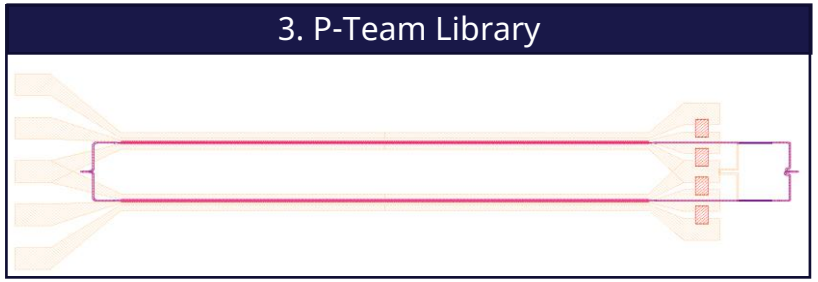
2.



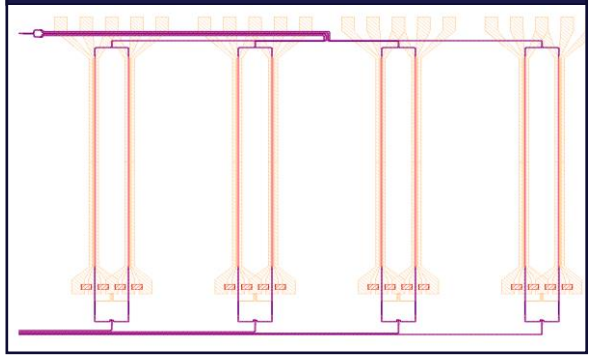

2. Tyndall Packaging ADK



3. P-Team Library



4. 4-lane MZM design



# What can we do for you? What can you do for us?

- Designers get a state-of –the-art design solutions
  - Well maintained IP
  - Managed dependencies
  - Rapid iterations
- Supply chain partners get to
  - Focus on their core added value
  - Maintain and distribute their added value without comprising business logic
  - In an open environment ready to integrate with others.
- Talk to us:
  - Technical specification
  - Business logic

# We are hiring!

## Open positions

Sales engineer

Application engineer

Apply

**Luceda People | Chiara: Science and core skills, a powerful combination**

Chiara, who works as a Marketing, Sales & Application Engineer, appreciates the diversity her job entails. In additional to technical work, Chiara is also responsible for sales and marketing, which tu...

Read interview

## Connect with us on LinkedIn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Connect with Joris


Connect with Chiara

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