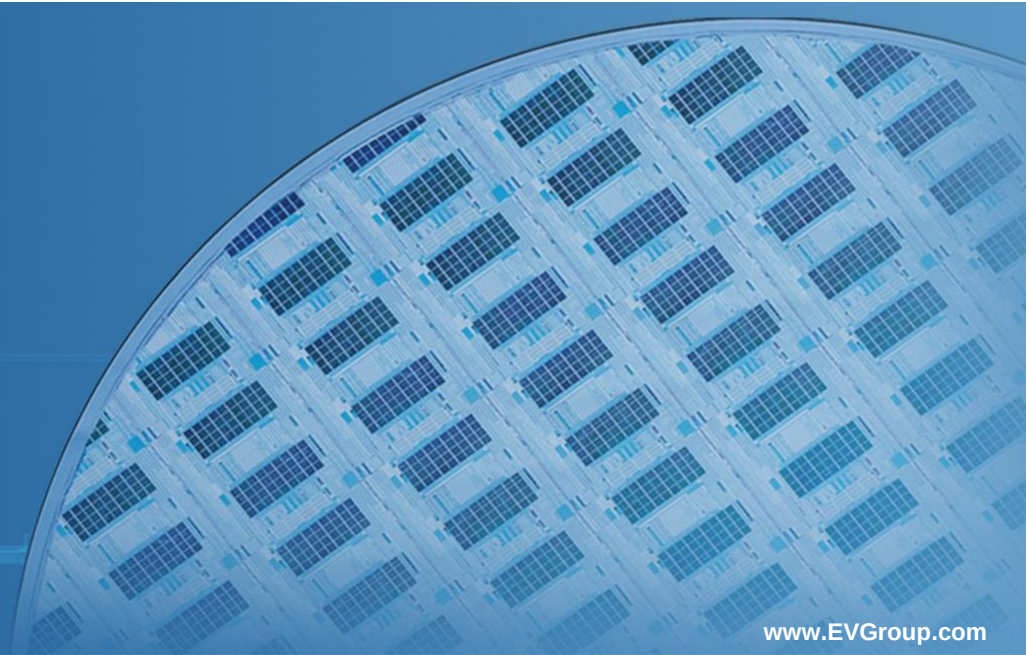
Wafer Bonding: Enabling microLED Display Revolution

Dr. Anton Alexeev, Business Development Manager



EVG Enables Full Process of µLED Displays Fabrication

Metrology

Wafer cleaning

Hybrid Bonding

Nanoimprint Lithography

Collective die to wafer transfer

Low temperature bonding

Color Conversion

Glass bonding

Resist processing

Temporary bonding

High precision bonding

Metal bonding

De-bonded carrier wafer

µLED Mass transfer

Waveguide NIL

Adhesive bonding

De-bonding

Wafer-level optics formation

< 8'' EPI wafers

12'' Carrier wafer

Reconstituted 12'' wafer

CMOS driver wafer

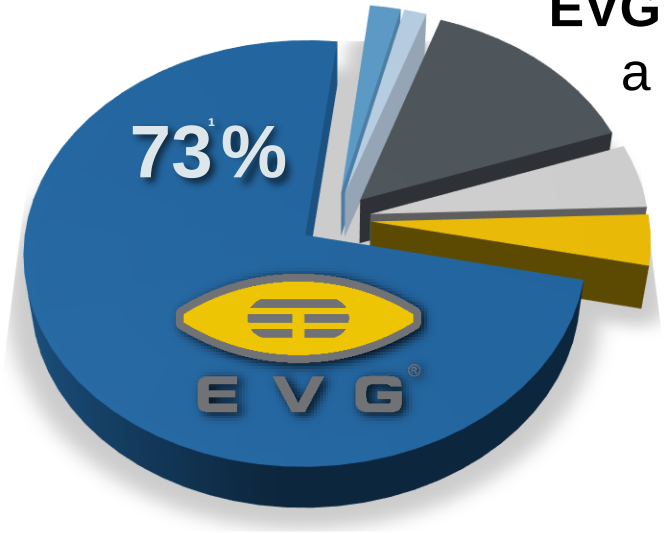
Singulated micro display

AR glasses

Wafer Processing → **Epitaxial Transfer** → **µLED Fabrication** → **Optics Formation** → **Waveguide Integration**

Executive Summary

Micro-Displays



EVG is an indisputable market leader in **wafer bonding**, a **key technology** for **µLED displays** manufacturing.

Our solutions go beyond bonding and enable many **µLED display** solutions for the industry leaders.

Process Development → **In-house Pilot Manufacturing** → **R&D and HVM Equipment**

Our Bonding Expertise

- Hybrid
- Fusion
- Plasma activated
- Adhesive
- Metal diffusion
- Wafer to wafer
- Die to wafer
- Temporary
- De-bonding

Other Technologies

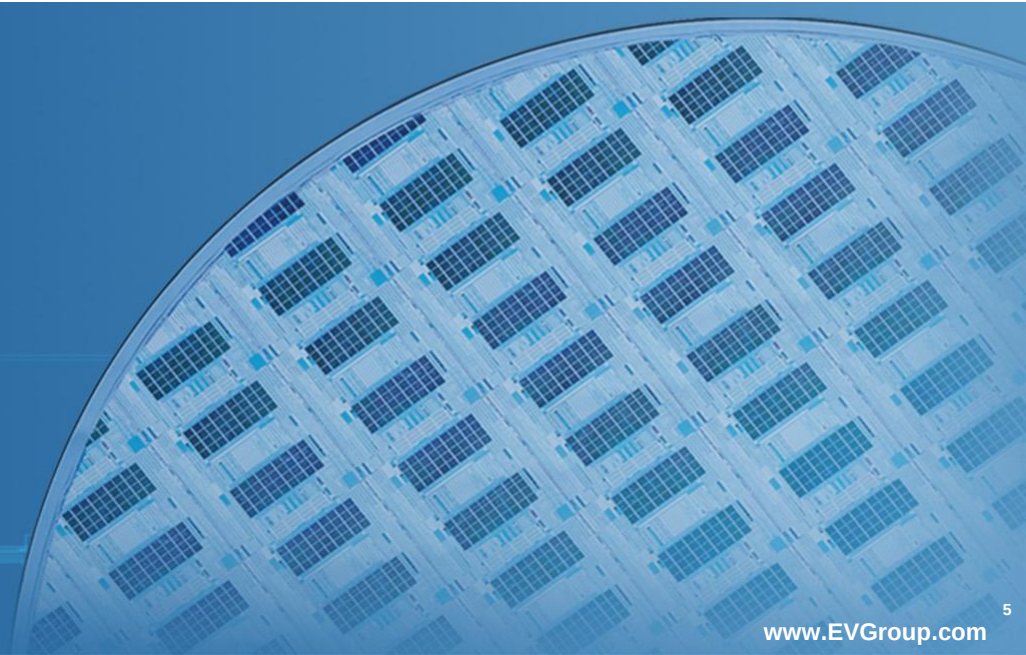
- Waveguides nanoimprint
- Wafer-level micro-optics
- Mass transfer

[1]Market report by Yole Développement 2021, permanent bonding market *"Bonding and Lithography Equipment market for more than Moore Devices"*

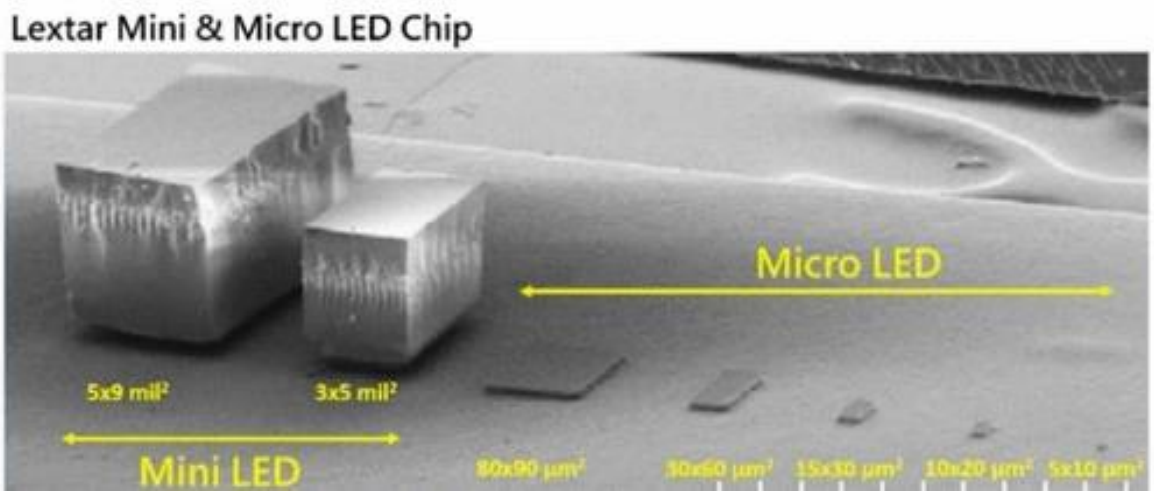
Outline

- µLED
- Display Technologies
- Analysis of Micro-display Manufacturing
- Technology Demonstrators
- Unique Technologies

µLED



µLED | Overview



µLED dimensions are <100µm.

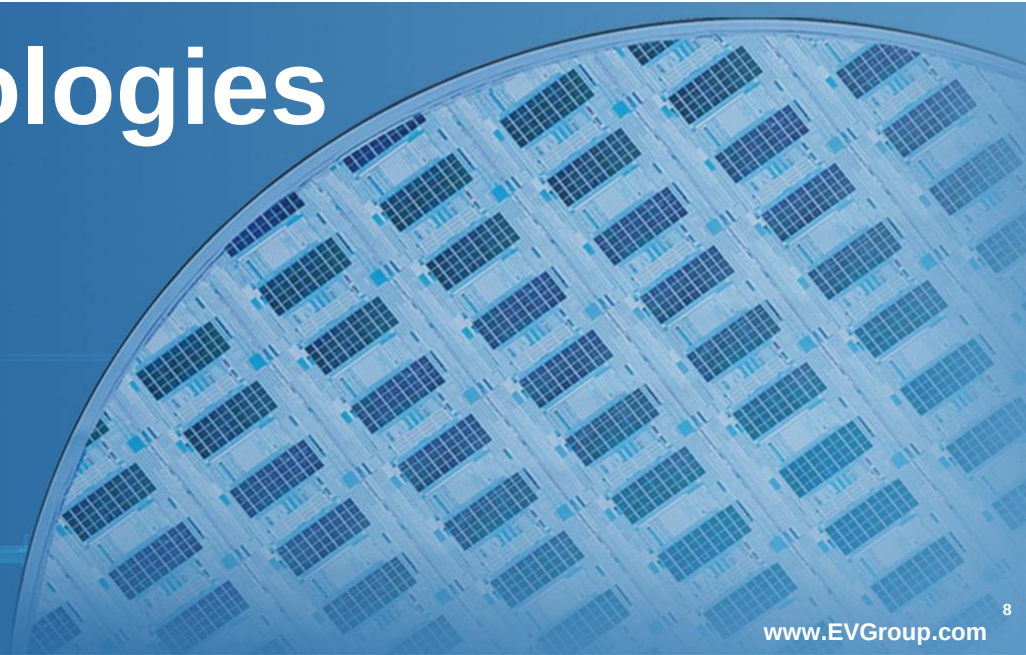
Unlike the larger counterparts, **µLEDs** must be de-attached from the substrate due to their size.

Brightness Comparison

Sun	µLED Micro-display	Eye Upper Limit	Clear Day Snow	Moon Surface	OLED Phone Screen
					
≈1Gnit	>1Mnit	≈ 200 Knit	≈ 20Knit	≈ 2Knit	<1Knit

Due to the projection optics losses and the AR image scaling the brightness of µLED micro-displays should significantly exceed the upper limit of the eye sensitivity.

Display Technologies

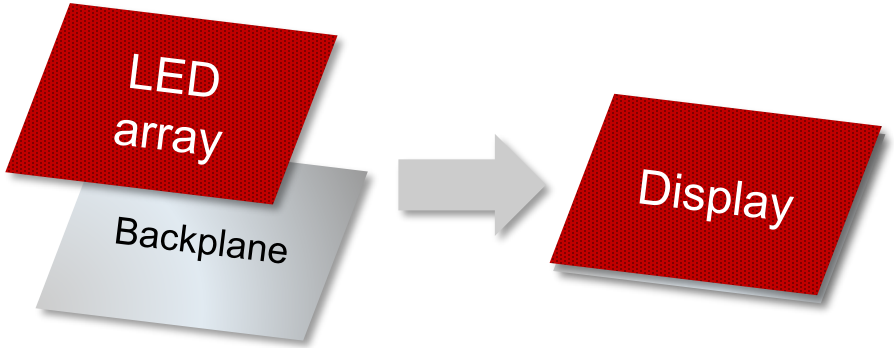


µLED Display Architecture

The backplane and µLED array designs, manufacturing and assembly methods significantly vary depending on the display type.

Two major parts of the µLED displays:

- µLED array - light emitter
- Backplane - control and input interface



Complex micro-display architecture and intrinsic difference of the EPI and backplane wafers materials and processing sets a need for advanced heterogeneous integration solutions.

µLED Display | Types

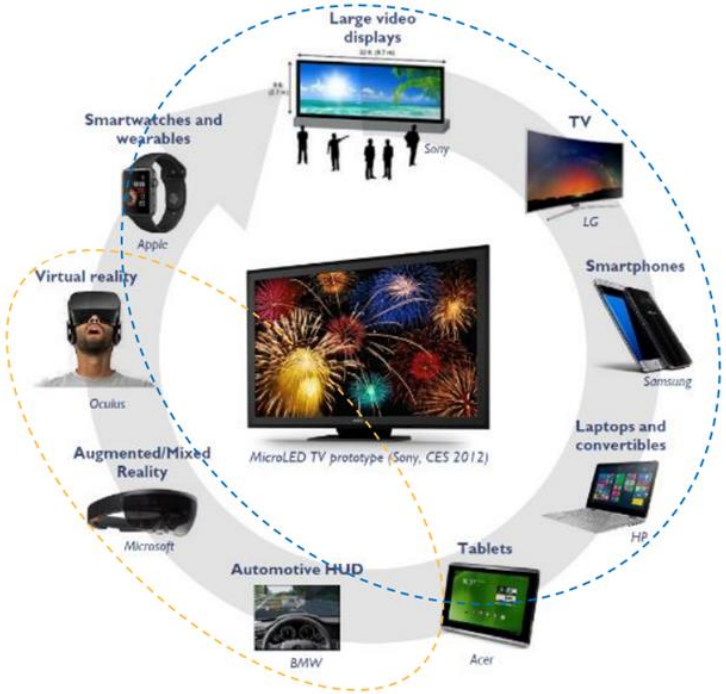
µLED display market consists of two major clusters:

- **Direct-view displays**
- **Micro-displays**

Micro-displays have very small pixel size of ≈10µm and less. They can maintain high resolution and have compact size.

This makes **micro-displays** a perfect solution for **VR, AR, HUD** and **mini-projector** applications.

Direct-view displays



Micro-displays

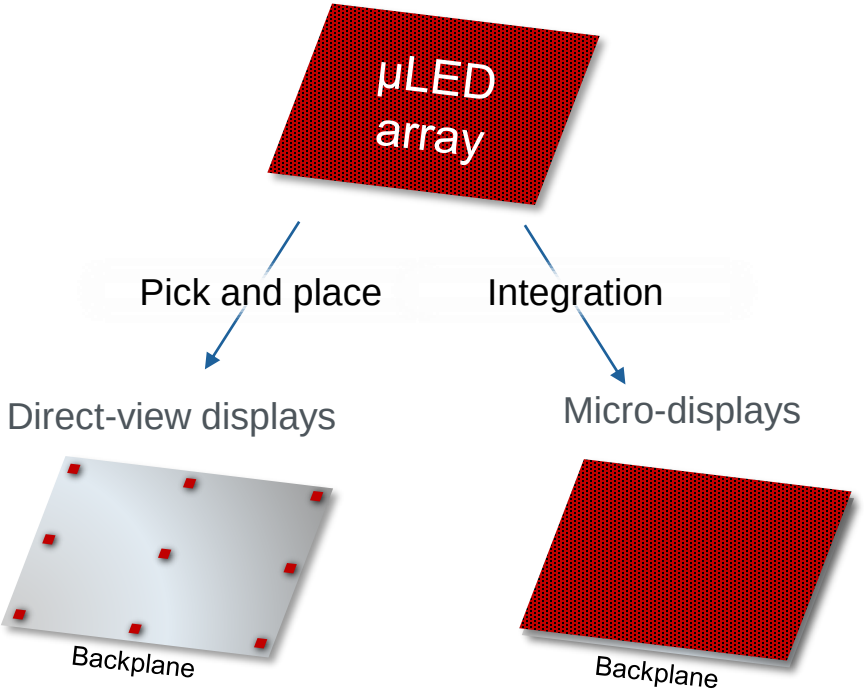
µLED Display | Architecture Type-Dependence

Due to the significant difference in the display sizes these two segments have different major bottlenecks:

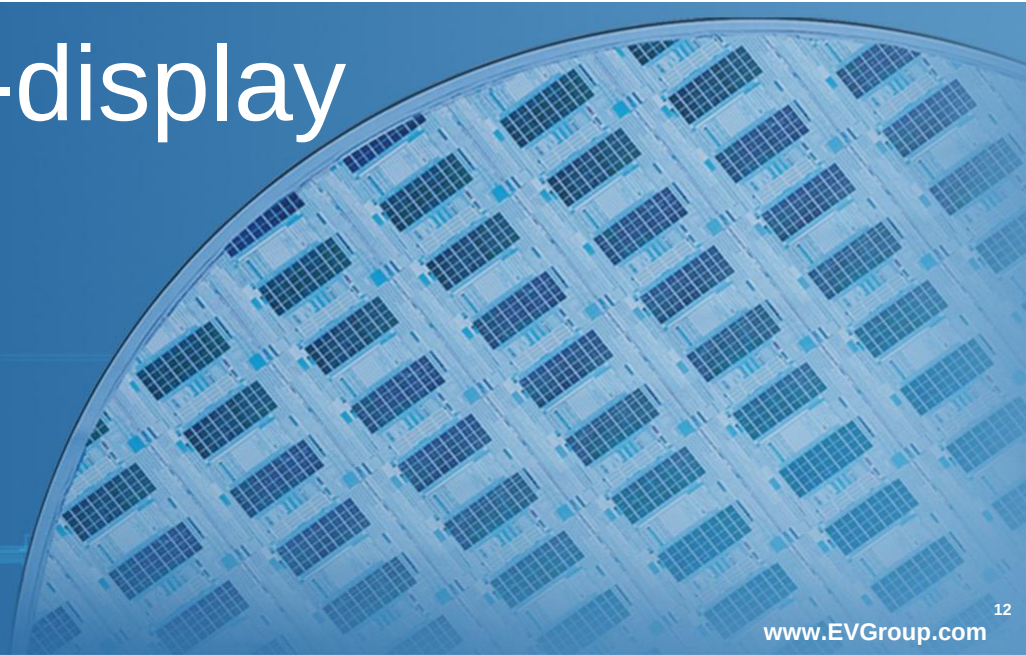
Direct-view displays are heavily dependent on the µLED mass transfer processes.

Micro display manufacturing requires to find a way to achieve extreme pixel pitch.

The integration of the µLEDs and the backplane requires advanced bonding solutions.



Analysis of Micro-display Manufacturing

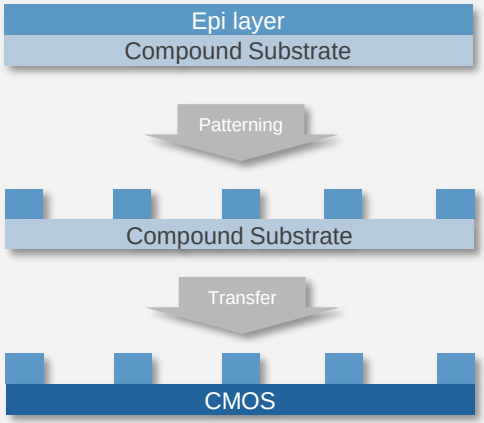


µLED Displays | Manufacturing Process

10µm 1µm

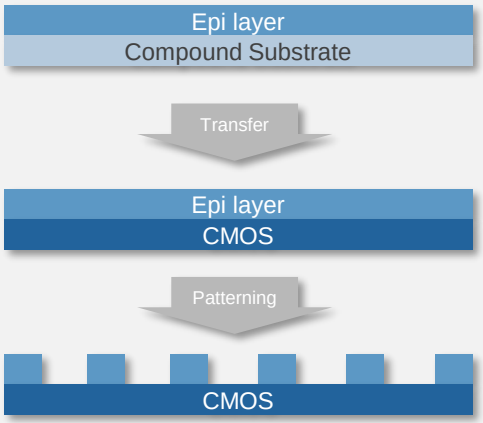
Hybridization ⟶ **Monolithic**

Singulation First



Pitch <10µm is challenging

EPI Transfer First

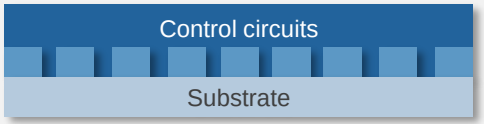


Commercialization is ongoing

EPI growth on the backplane

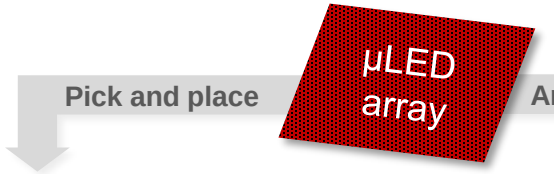
Challenging due to CMOS-EPI processing temperature mismatch

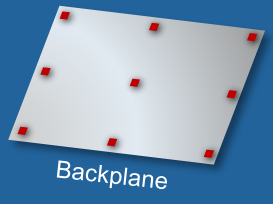
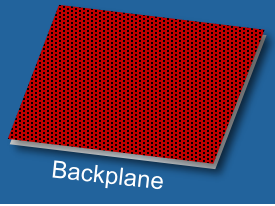
Control circuitry growth on top of a µLED array



Research is ongoing

Production Flows Overview

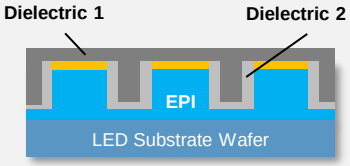


	Direct view displays		Micro Display
			
	µLED Pixel	**µLED Smart Pixel**	**µLED array on CMOS driver**
Applications	Smart watch, smart phone, laptop, TV…	Smart watch, smart phone, laptop, TV…	AR, HUD, etc
Further processing	Mass transfer	Mass transfer	Integration with optics
Bottleneck	Mass transfer of the pixels	Mass transfer of the pixels	Extreme pixel pitch

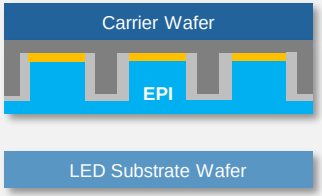
The next slides exhibit a representative but not a full list of EVG technologies for µLED displays manufacturing. The process flows vary significantly company to company.

µLED | Pixel

1. Epi Patterning + Etching, Deposition

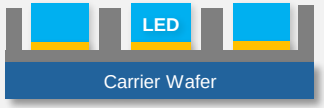


2. Adhesive Bonding, Substrate Laser Lift Off



3. GaN etching, CMP

4. Etching, Annealing



Next step: mass transfer

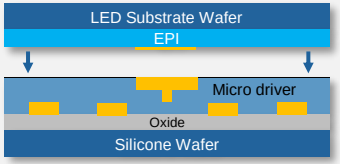
EVG Technology	Application	Equipment
Optical lithography	Patterning of the EPI wafer to singulate the µLEDs	6XX IQ aligner
Spin & Spray coating	Adhesive coating	1XX
Adhesive bonding	EPI transfer + LED transfer	5XX 850 Gemini
Laser Lift Off	EPI substrate removal	850DB

µLED pixel process is the least complicated.

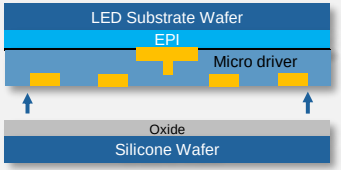
Nonetheless, advanced solutions with multiple selective-etched dielectric layers are common.

µLED | Smart Pixel

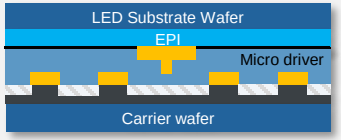
1. Adhesive bond, Metal aligned bond



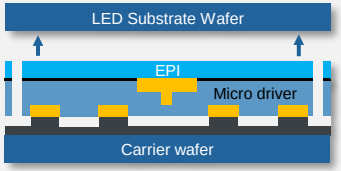
2. Debonding



3. Adhesive bonding



4. Substrate LLO, Patterning + Etching



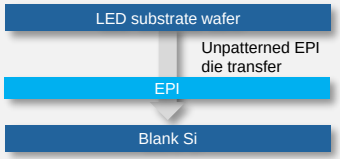
Next step: mass transfer

EVG Technology	Application	Equipment
Ultra Thin Layer Transfer	Substrate MOS Driver substrate	BondScale
NanoCleave	Alternative to Thinning and wet oxide etching	850DB
Adhesive bonding	EPI transfer + LED transfer	5XX 850 Gemini
Laser Lift Off	EPI substrate removal	850DB
Metal Bonding	Substrate MOS Driver substrate	5XX Gemini

Smart pixel process flow is more complicated and can require additional aligned bonding.

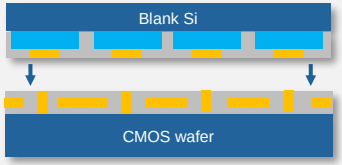
µLED | Micro Display

1. LED wafer reconstitution, planarization, patterning.

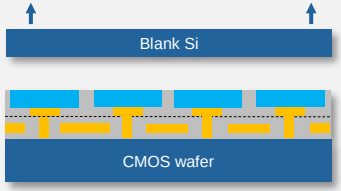


2. Reconstituted wafer planarization and patterning.

3. Hybrid bond



4. Carrier removal, optics, color conversion

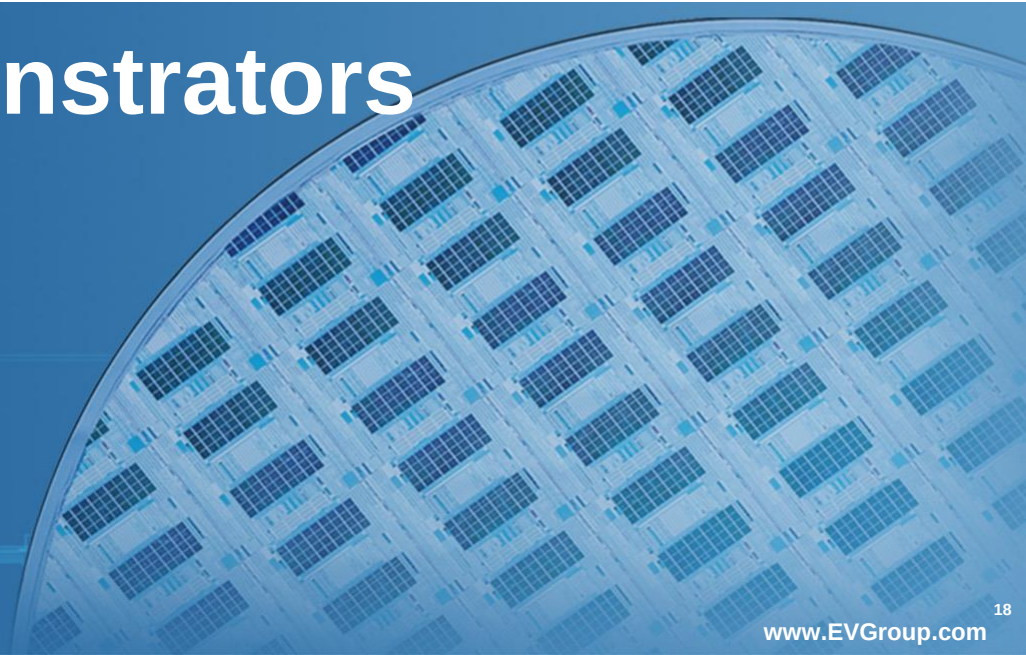


Next steps: color conversion/integration

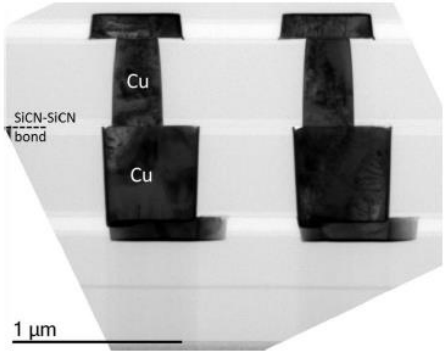
EVG Technology	Application	Equipment
Laser Lift Off	EPI substrate removal	850DB
Wafer Reconstitution	Utilization of 300mm frontend semiconductor processing	320
Hybrid bonding	Fine pitch bond of the µLED EPI wafer to the CMOS driver wafer	GEMINI FB
NIL	Optics formation	7XXX
Spin & Spray coating	Color conversion layer deposition	1XX

µDisplay manufacturing requires high precision alignment bonding to fulfill the fine pixel Pitch requirements.

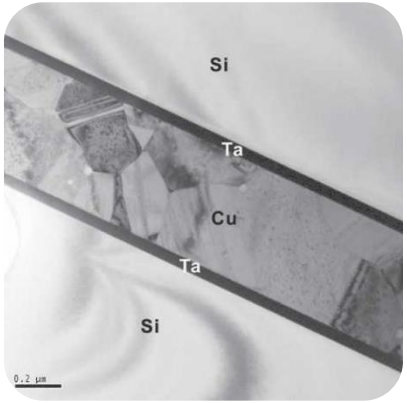
Technology Demonstrators

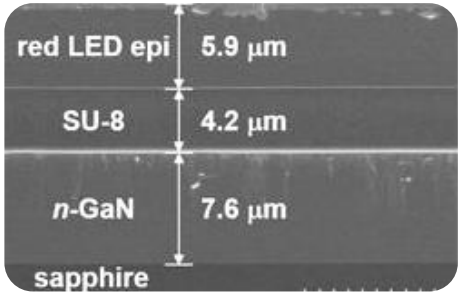


EVG Wafer Bonding Technology



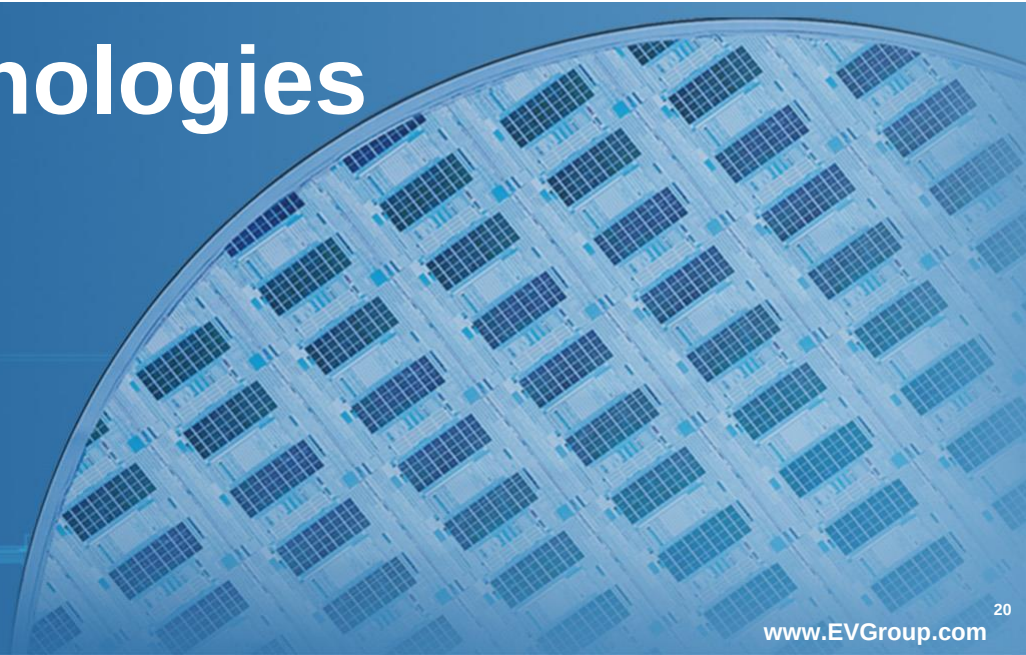
Courtesy of IMEC;
Peng et.al.; IITC 2018





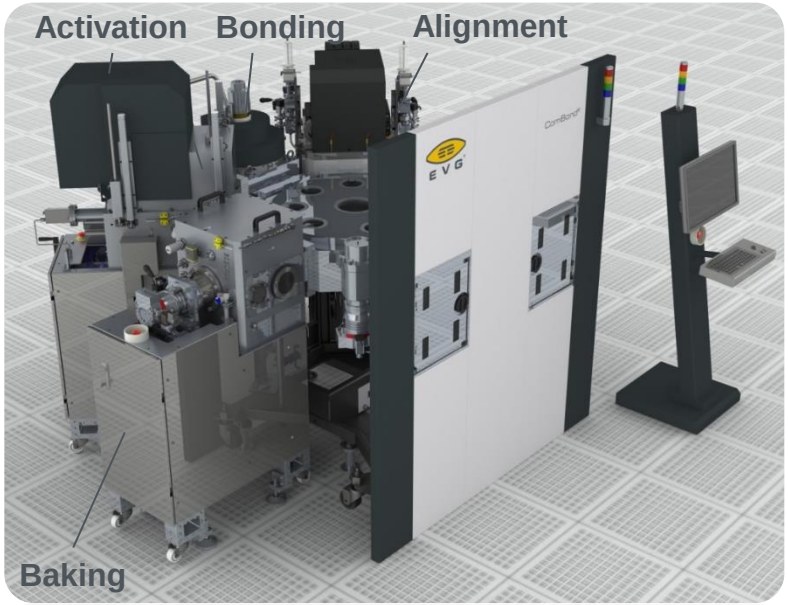
No Interlayer	Anodic	Pitch
	Fusion	2 µm
	Hybrid	2 µm
Metal Interlayer	Thermo-compression	5 µm
	Solder-based Eutectic/TLP	30 µm
Insulating Interlayer	Adhesive	30 µm
	Glass frit	

EVG Unique Technologies



ComBond® | Unique high vacuum wafer bonding platform

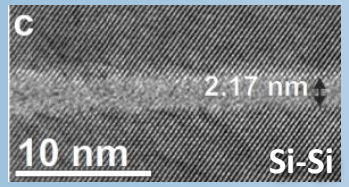
- Oxide-free metal bonding
- Optical alignment in high vacuum
- Great for the process development phase
- Enabling new products and devices

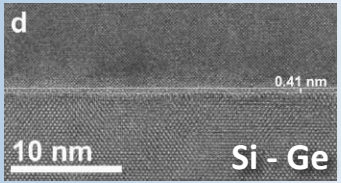


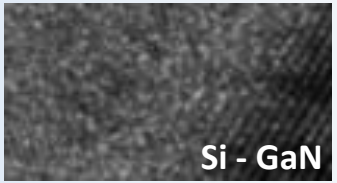
- Room temperature heterogenous integration
- High vacuum encapsulation for leading-edge MEMS devices

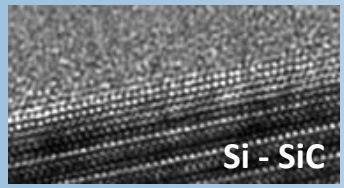
Process Results | Overview

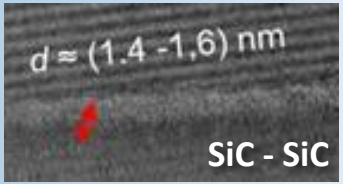
Bonding Materials	
Si (100)	Si (100)
	Sapphire
	GaN
	Ge
	$LiNbO_3$
	$LiTaO_3$
	Mo
	Si_xN_y
Si (111)	Si (100)
	Si (111)
$Si(SiO_2)$	Si
	$Si(SiO_2)$
SiC (4H)	Si
	SiC (4H)
	Poly-SiC
Poly-SiC	Poly-SiC
GaAs	InP
	Si
	SiC
Au	Au
Cu	Cu
Al	Al

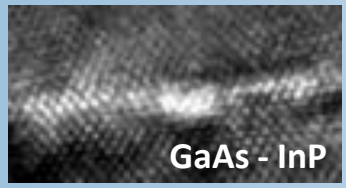


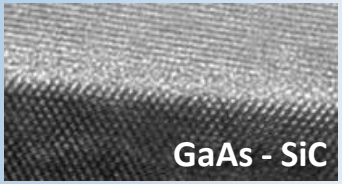


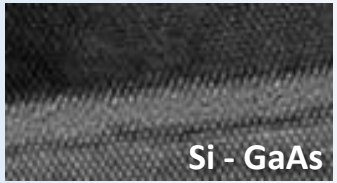


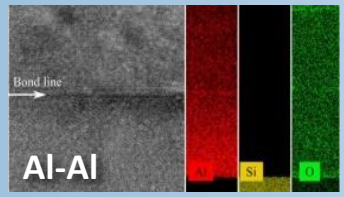


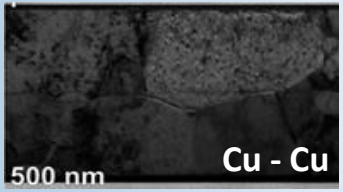






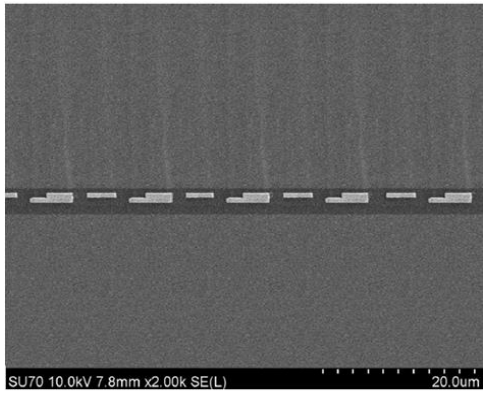




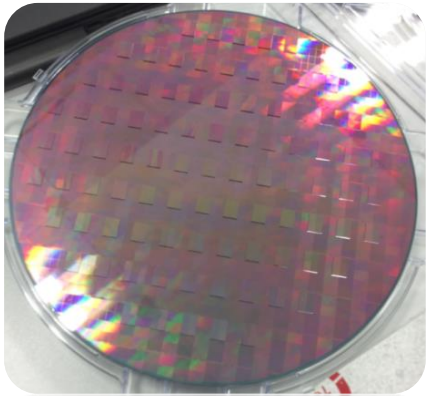


Co-D2W Bonding | Process Results – Hybrid Bonding

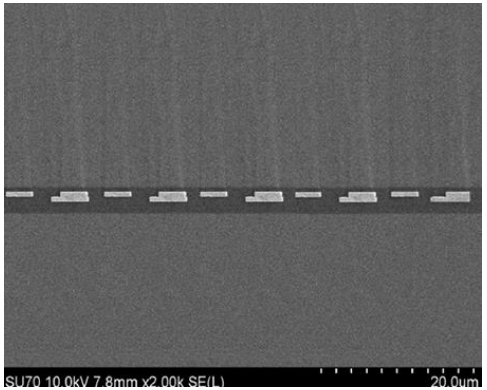
Edge Die

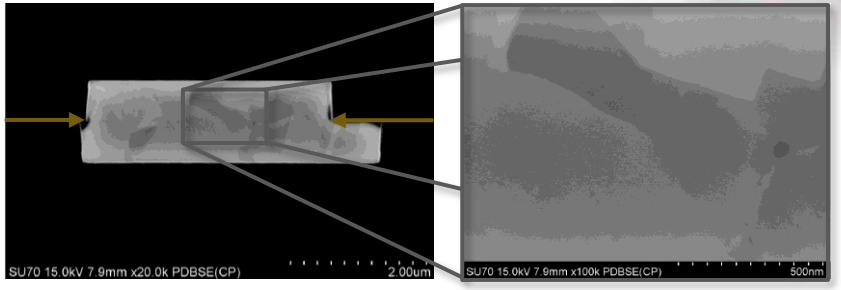


300mm 10x14 Dies



Center Die





Excellent collective die to wafer bonding performance

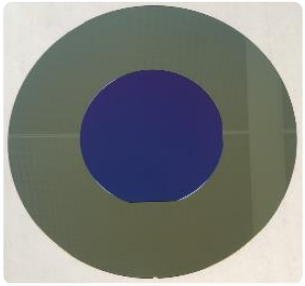
Heterogenous Wafers Bonding I Different Substrate Dimension

Bonding of wafers of different size enables seamless integration of EPI and CMOS wafers

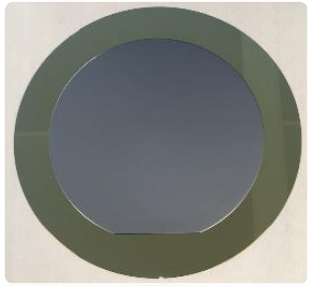
Smart View NT2 3δ < 200nm

Smart View NT3 3δ < 50nm

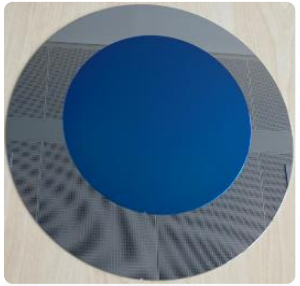
100 mm GaAs / GaN	150 mm GaAs / GaN	200 mm Si	300 mm Si



100 mm / 200 mm



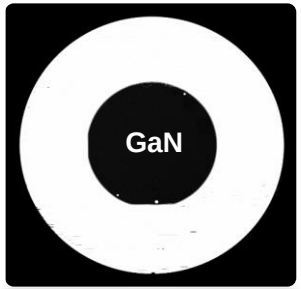
150 mm / 200 mm



200 mm / 300 mm

PVA TePla

SAM Bonding area > 99%.



100 mm / 200 mm

150 mm / 200 mm

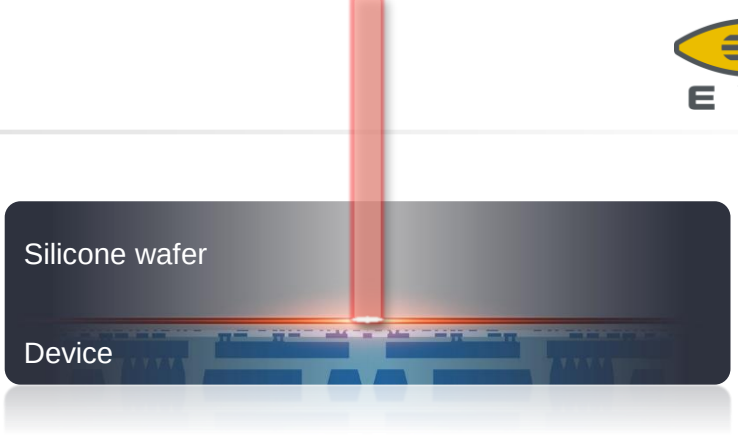
NanoCleave

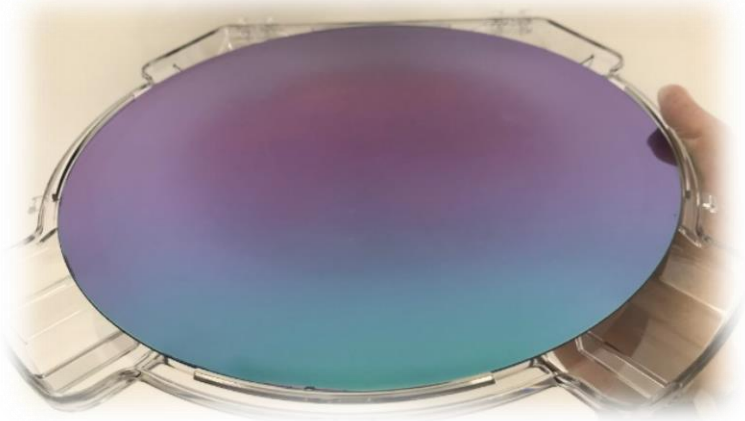
- Enables silicon wafers as temporary carriers
- Laser debonding through silicon carriers

- Nanometer precision
- Ultrathin (<10µm) die and wafer processing

- Fusion bonding compatible
- Inorganic and front-end processing-friendly

- Stable < 1000 DegC





Device DB interface

Thank you!