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W2W and D2W Bonding Technologies Enabling Next Gen Integrated Photonics

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Bonding Challenges Related to Photonics

Wafer Level

Die Level (sometimes)

Different Wafer Size

Dissimilar Materials

Different CTE

Low Temp. Process

Often, density of photonics dies << density of Si die

Very Small Dies

Tight Alignment Budget

Trough-put challenge

Wafer Bonding Process Options

Recommended bonding processes for Photonics Integration

- **Wafer bonding technologies**
  - Without intermediate layer
    - Fusion/Direct bonding
      - Sub-µ interconnect pitch possible
      - ComBond: Room Temperature
      - LT Plasma: 150 to 300°C
    - Anodic bonding
  - With intermediate layer
    - Insulating interlayer
      - Glass frit bonding
      - Adhesive bonding
        - ~ 20µ interconnect pitch
    - Metal bonding
      - Hybrid bonding
        - Sub-µ interconnect pitch
        - LT Plasma: 150 to 300°C
      - Solder bonding
        - Eutectic bonding
        - Transient liquid phase bonding
          - ~ 10 to 20µm pitch
          - 150 to 280°C
      - Thermo-compression bonding
        - ~ 5µm pitch
        - 200 to 350°C

W2W and D2W Bonding | General Overview

	Collective - D2W EVG® GEMINI®	Direct Placement - D2W EVG® 320D2W	Wafer to Wafer EVG® GEMINI® FB- SmartView® NT3
Transfer Method	Collective Die Transfer by Reconstituted Carrier	Direct placement of plasma activated and cleaned dies using Flip Chip Bonder	High Precision Wafer to Wafer Hybrid Bonding
Alignment capability	1,5 µm proven 500 nm under development	< 1 µm 200 nm under development	100 nm 50 nm under development
Challenges	Cost & Alignment Accuracy	Alignment accuracy Surface cleanliness / Surface preparation	Integration limitation
Benefits	Qualified wafer level equipment for plasma activation and cleaning	Costs Integration flexibility	HVM Qualified process UPH
Maturity	Application specific volume production proven for several years	Feasibility testing ongoing	High Volume manufacturing

→ Supporting every integration flow through volume proven surface activation and cleaning process

Wafer to Wafer bonding: Hybridization

Role of EVG : Integration of GaN μ LEDs on Sapphire to Silicon CMOS by wafer to wafer bonding

Integration

- GaN is grown and patterned on sapphire
- No active CMOS backplane on sapphire
- LEDs need to be integrated with CMOS

Standard Process flow for Hybridization

Sapphire

CMOS

μ LEDs on Sapphire (top wafer). CMOS (bottom wafer) after metallization and patterning

Sapphire

CMOS

Wafer 2 Wafer aligned bonding

Sapphire

CMOS

Sapphire removal by LLO

Mass transfer/Color conversion

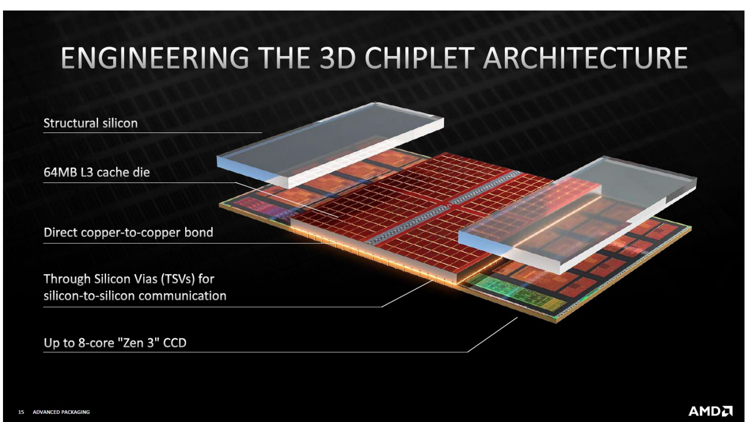
CMOS

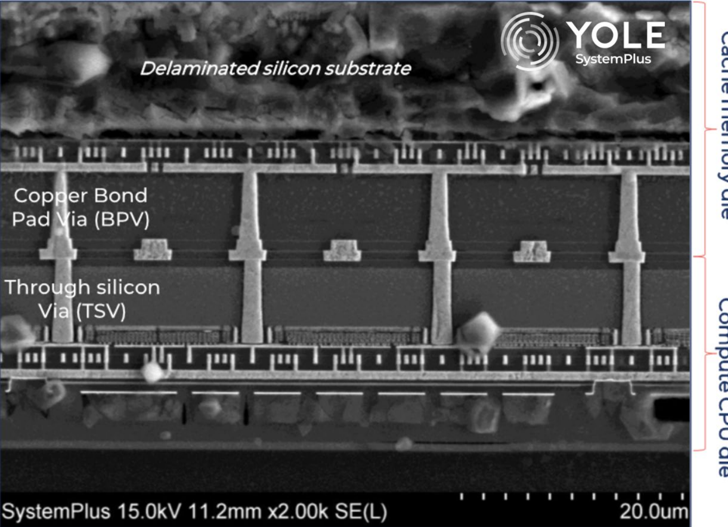
Full color display

	Low resolution (down to 30 μm pixel)	Medium resolution (down to 15 μm pixel)	High Resolution (<15 μm pixel)
Bonding type	Eutectic/Transient Liquid Phase	Thermo compression/Adhesive	Fusion/Hybrid bonding

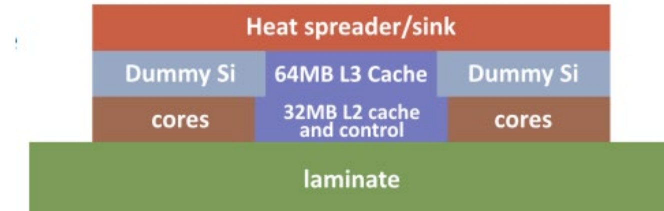
Hybrid Bonding Example: AMD's V-Cache™

- Using TSMC's SoIC with hybrid Cu-to-Cu bonding in production for desktop and laptop CPUs, gaming
  - 3X interconnect energy efficiency (vs. µbump 3D)
  - >15X interconnect density (vs. µbump 3D) •
- Thermal is a problem with 3D stacking
  - Material selection important
  - Which thermal interface material to use and how to select is critical





Package Cross-section #2 – SEM View



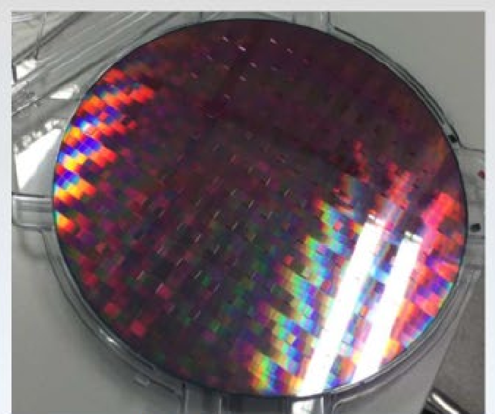
Collective Die-to-Wafer (Co-D2W) Bonding | Process Flow

Alignment Strategy
a, Local alignment key for every die
b, Global alignment key for wafer to wafer alignment

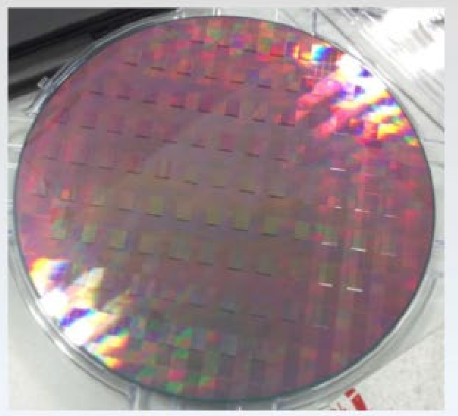
Transfer Method	Pro's	Con's	Maturity Level
Collective Die Transfer by Reconstituted Carrier	• Proven technology • Die activation and cleaning equivalent to W2W hybrid bonding • Oxide management • Reuse of carrier feasible	• Error propagation of D2W + W2W alignment • Cost of carrier prep, utilization and clean • Die thickness needs to be in narrow range	High Volume production proven for several years

EVG
D2W Bonding – Process Results

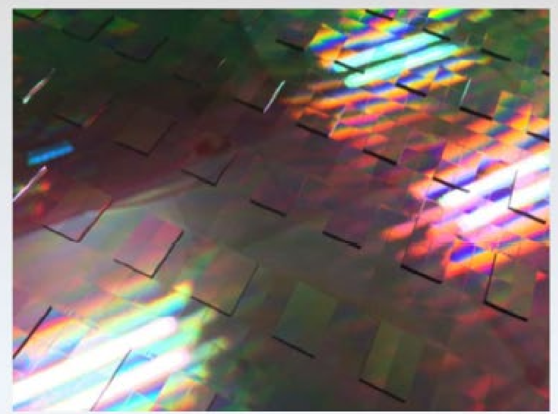
Co-D2W Bonding | Process Results – Hybrid Bonding

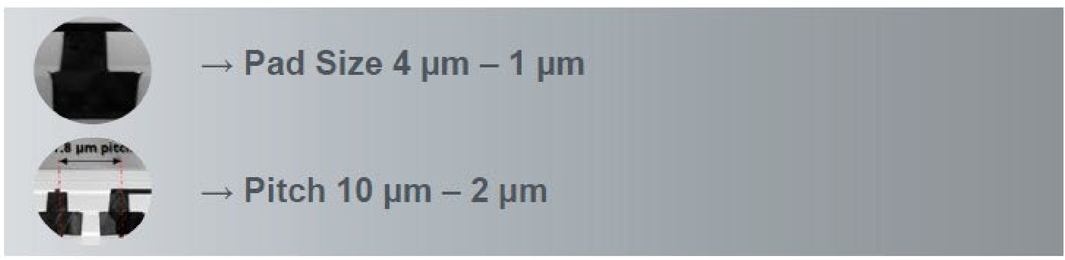


Demonstrator A - 300mm
Hybrid Bonding, 5 mm x 7 mm



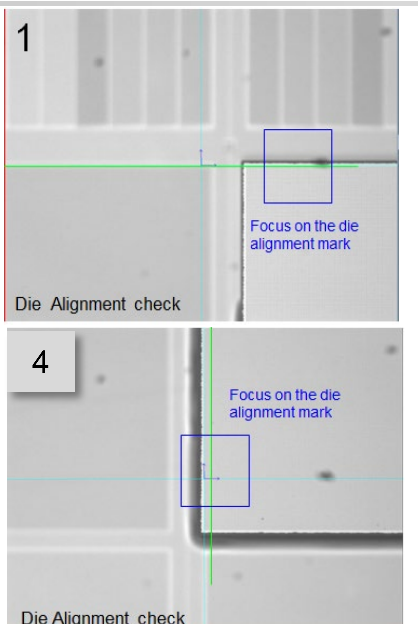
Demonstrator B - 300mm
Hybrid Bonding, 10 mm x 14 mm

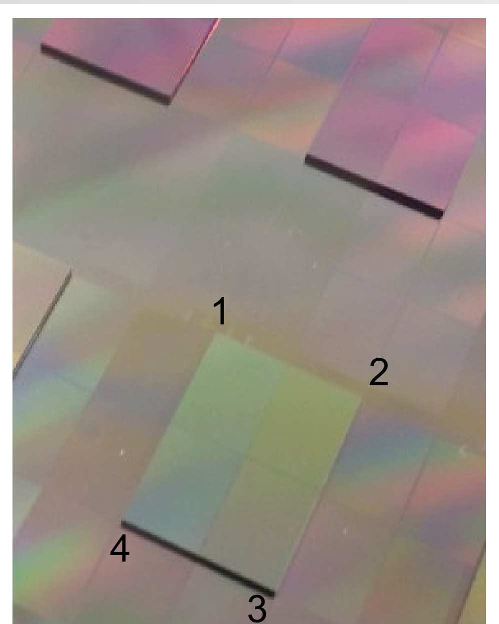


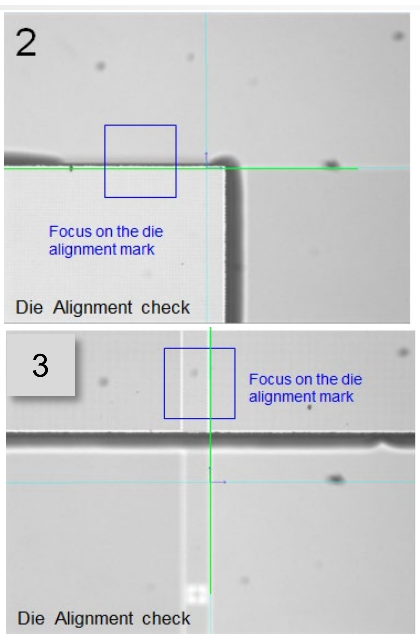


*Substrates provided under IRT Nanoelec program

Co-D2W Bonding | Process Results – Hybrid Bonding







Demonstrator	Die Dimension	Placement accuracy x 3σ	Placement accuracy Y 3σ
A	5mm x 7mm	< 2 µm	< 2 µm
B	10mm x 14mm		

Co-D2W Bonding | Process Results – Hybrid Bonding

Edge Die

SU70 10.0kV 7.8mm x2.00k SE(L) 20.0um

Center Die

SU70 10.0kV 7.8mm x2.00k SE(L) 20.0um

Bonding Interface

SU70 15.0kV 7.9mm x20.0k PDBSE(CP) 2.00um

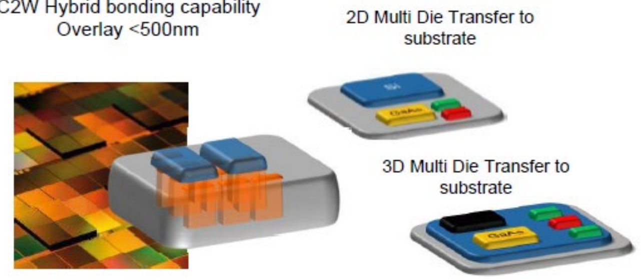
SU70 15.0kV 7.9mm x100k PDBSE(CP) 500nm

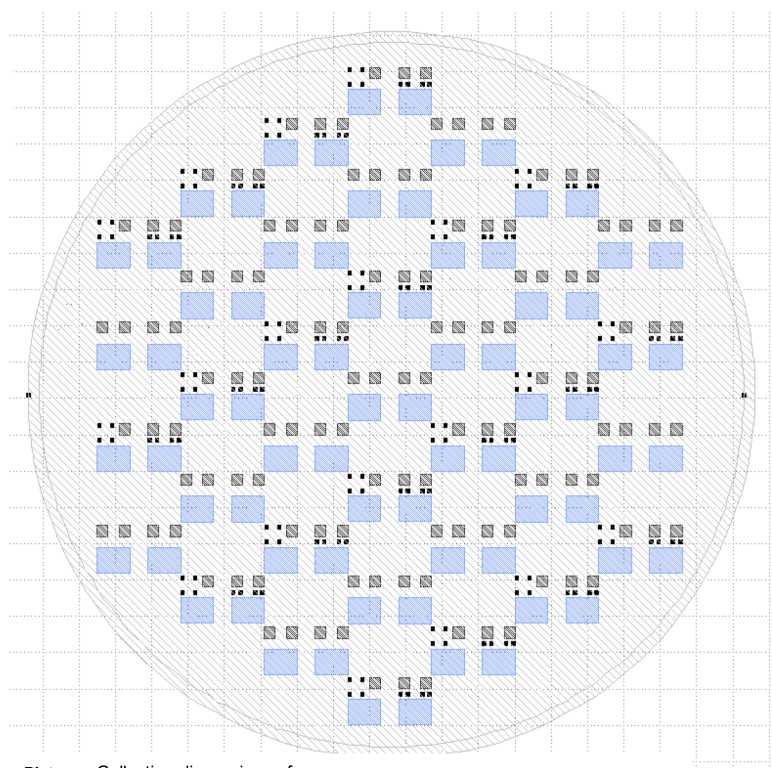
→ High Die transfer rate and alignment accuracy < 2μm

→ TEM evaluation of mechanical contact of the bonding pads and Cu grain growth across the bonding interface

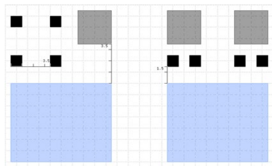
Co-D2W Bonding | Process Results – Multi Die - Direct Bonding

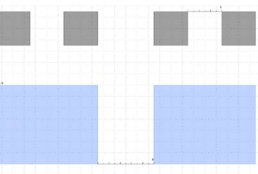
2D and 3D Multi Die transfer





Picture – Collective die carrier wafer map.





Picture – Collective die carrier wafer map – die detail.

Demonstrator A

Target wafer: 200mm Thermal Oxide wafer

Collective carrier wafer: 200mm Bare Silicon wafer

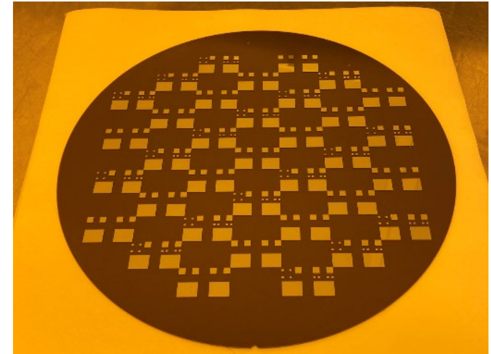
Die sizes:

- 1x1mm x350µm dies
- 3x3mm x350µm dies
- 7x9mm x350µm dies

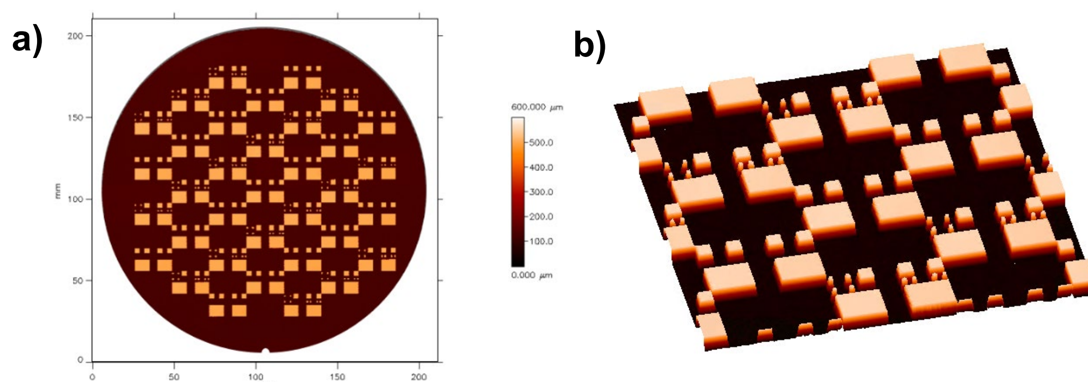
Co-D2W Bonding | Process Results – Multi Die - Direct Bonding

Post collective carrier preparation inspection

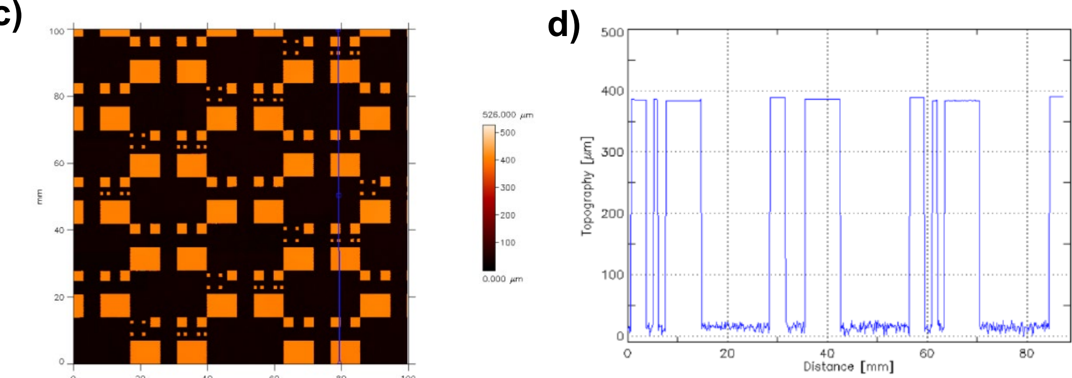
- A high-resolution die height variation (DHV) measurement was performed on the collective carrier with dies after placement using a chromatography sensor to evaluate the die uniformity / distribution.
- A die height variation < 3µm could be observed after collective die carrier preparation.



Picture – Collective die carrier wafers after die placement process.

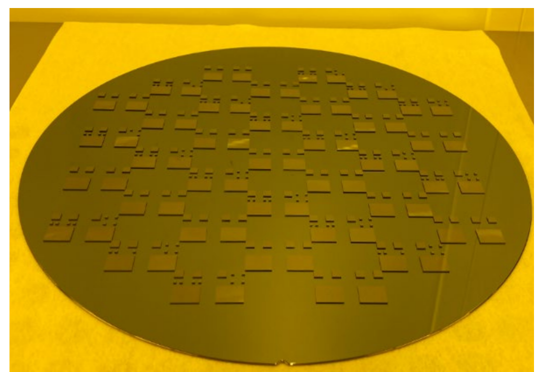


Die Height variation Measurement – a): Full scan – 2D collective carrier map; **b):** Detail scan – **3D collective carrier map.**

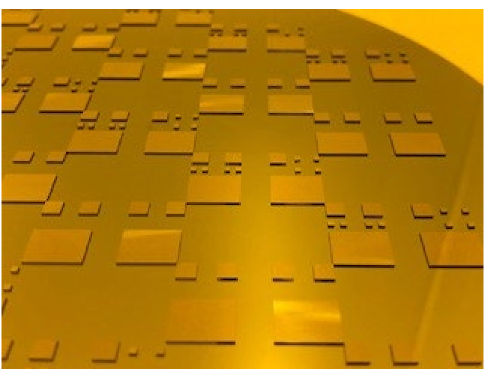


Die Height variation Measurement – a): Detail scan – 2D collective carrier map; **b):** Detail scan – DHV across the blue line.

Co-D2W Bonding | Process Results – Multi Die - Direct Bonding

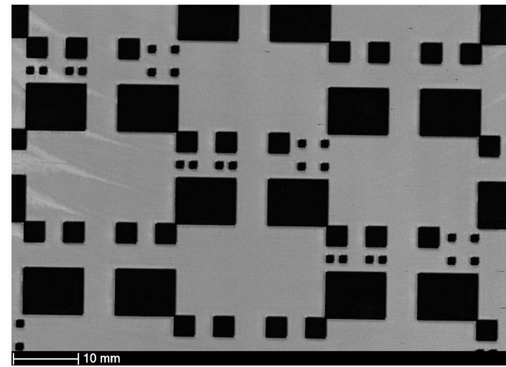


Picture – Target wafer with dies after die transfer process.

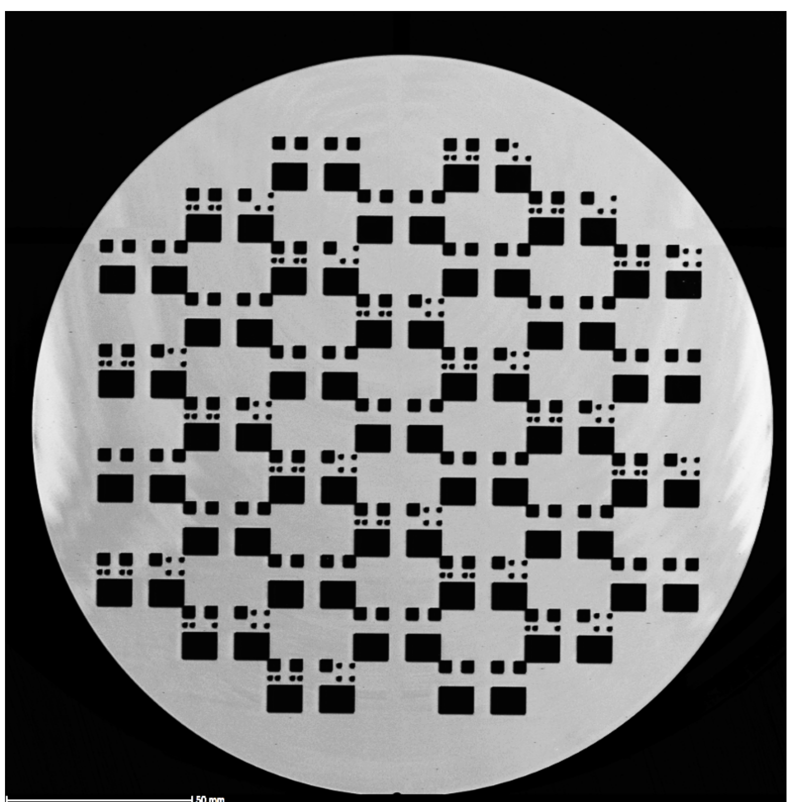


Picture – Target wafer with dies after die-to-wafer bonding process – die detail..

- High transfer yield including high bonding quality based on Scanning Acoustic microscope images (C-SAM) could be achieved.

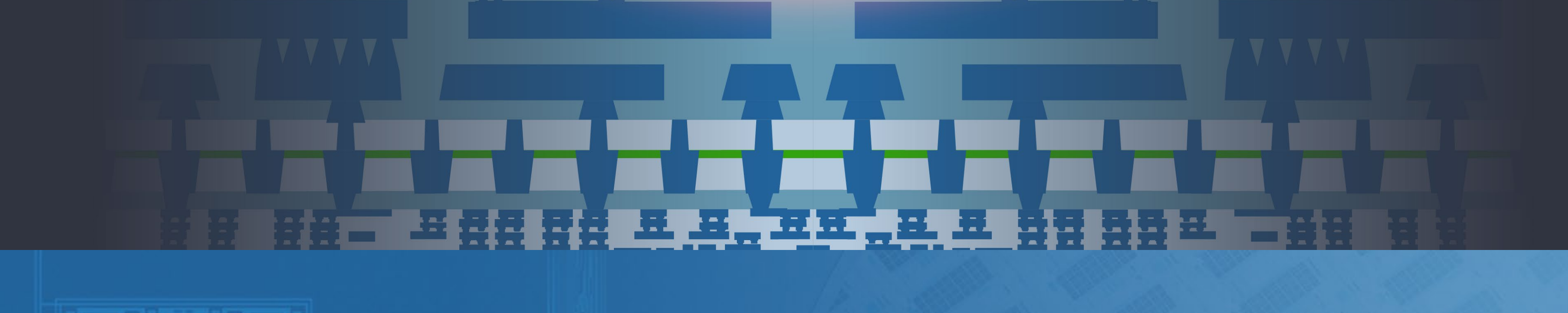


C-SAM inspection – Post annealing inspection – detail scan.



C-SAM inspection – Post annealing inspection – full scan.

NanoCleave™ IR Laser Release



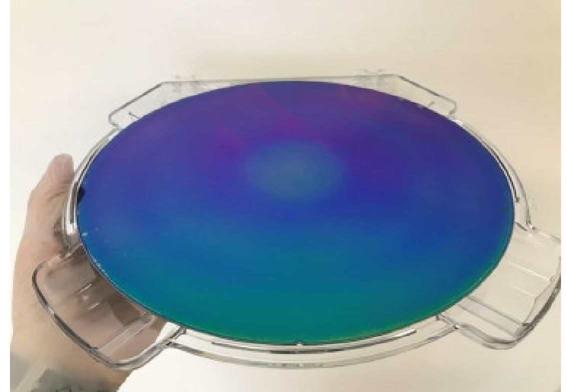
NanoCleave: A New Layer Release Technology

Enables:

- Use of Si carrier wafers
- Inorganic release layers
- Nanometer precisely defined cleaving planes
- High processing temperatures of stacks
- Room temperature release
- Extremly thin layers
- Applications ranging from advanced packaging to 3D integration to future scaling FEOL integration

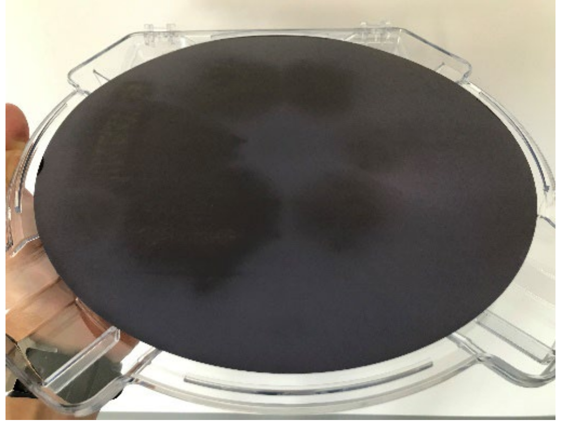
EVG NanoCleave™

- Technology is demo ready at EVG Headquarter Austria now



300 mm fusion bonded wafers released

- Layer Transfer of sub-μ layers feasible
- NanoCleave™ release layer may be below EPI growth layer



300 mm molded wafer released

200 mm temporary bonded thin device wafer released

Summary

- Photonic Applications present unique challenges for bonding applications
- D2W and W2W bonding applications co-exist for integration of photonics
- Both D2W and W2W bonding integration schemes benefit from the same bonding mechanisms. Fusion & hybrid bonding are the most popular bonding interface strategies

- Thin layer handling and release technologies complement bonding applications.
- NanoCleave^{TM} is a high temperature stable release technology compatible with Si carrier wafers

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