Presentation for EPIC Members New Product Release November 8th ‘22

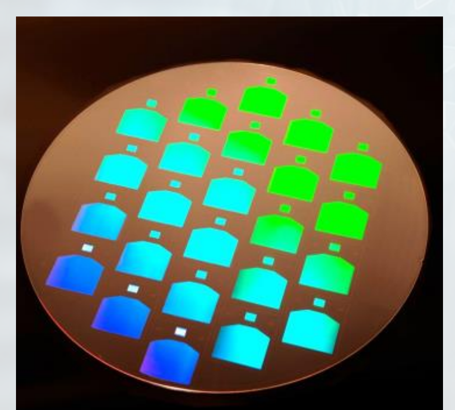
LITHOSCALE®: A Unique Maskless Exposure Tool Designed for Next–Generation Devices

EV Group | Company Overview

Leading supplier of wafer processing equipment for the MEMS, nanotechnology and semiconductors markets.

Founded in 1980 by DI Erich and Aya Maria Thallner. More than 1100 employees worldwide.

Headquarters in Austria, with fully owned subsidiaries in the USA, Japan, South Korea, China and Taiwan.

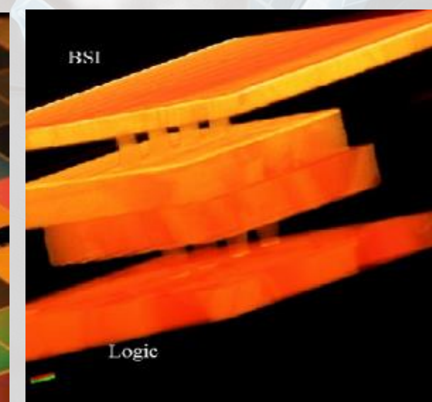


Nanoimprint & S&R Mastering

Wafer Level Optics & Photonics Packaging

Advanced Resist Processing

Heterogeneous Integration



3D Integration & Hybrid Bonding

EV Group | Lithography Tools

	Mask Aligner	Maskless Exposure	UV–NIL
			UV Curing
Pattering method	Proximity Mask Aligner Exposure	**MLE™ Maskless Exposure Technology**	Nanoimprint Lithography
Pattern field size	Full field	**Clustered Write Heads**	S&R and Full Field
Exposure wavelength	Broadband (g, h, i-line)	**Multiple - Wavelength Exposure Optics**	UV - LED
Resolution L/S	> 3 µm	**< 2 µm**	< 30nm

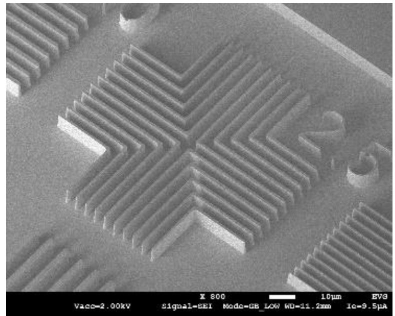
EV Group MLE™ | LITHOSCALE® Key Performance Indicators

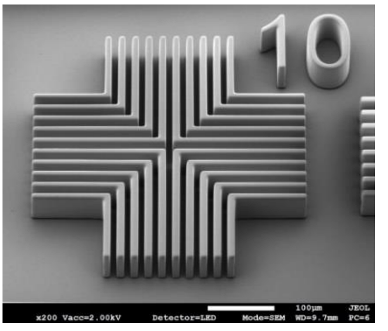
- SW: Real–time autofocus, active distortion & surface in-variations compensation.
- LAYOUT: independency from chip/reticle size for large size die, multi-die architectures, die-level patterning.
- HIGH RESOLUTION capability < 2 µm L/S at high dose and high throughput and high aspect ratio.
- Scalable substrates from wafers to panels and substrate materials.
- Scalable throughput with multiple write head configurations from R&D to HVM.

Parameter	Specification
Exposure Source	HP UV – Laser Diode (LD)
Exposure Spectrum [nm]	375, 405
CD L/S [µm]	< 2
Substrate Sizes [inch]	8“ – 12“
Wafer Layout [format]	GDS II (standard) etc.

ADVANCED PACKAGING

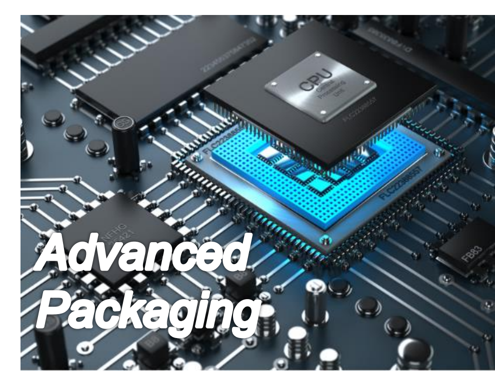
- L/S shrinkage enabling increased RDL line density, I/O pitch density without die size increase.

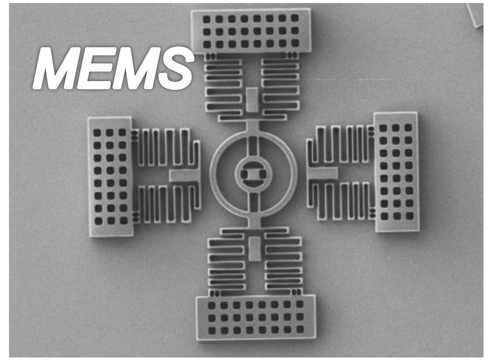


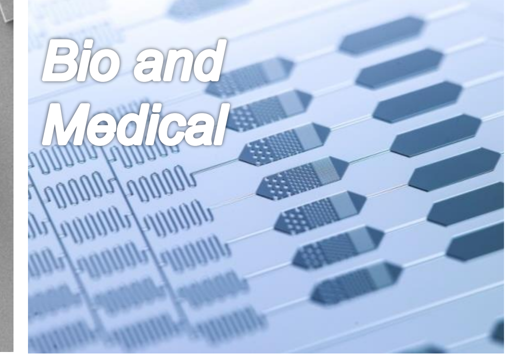


EV Group | Target Markets for Maskless Lithography

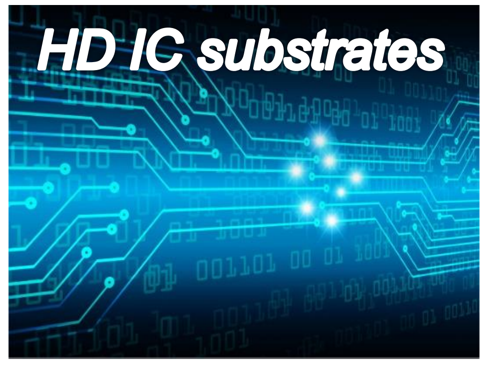
established



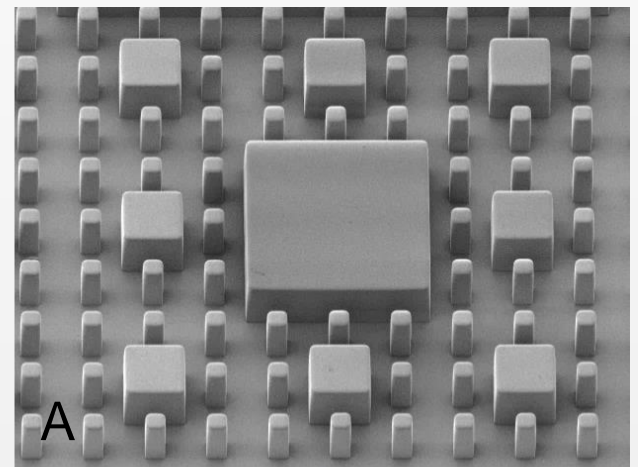


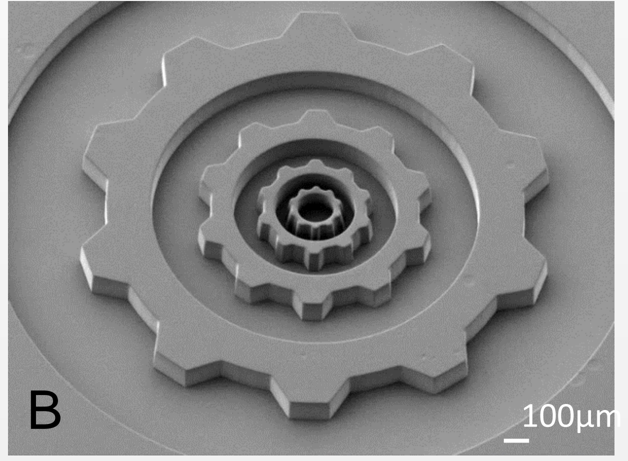


applications in development



EV Group MLE™ | LITHOSCALE® Applications & Process Results

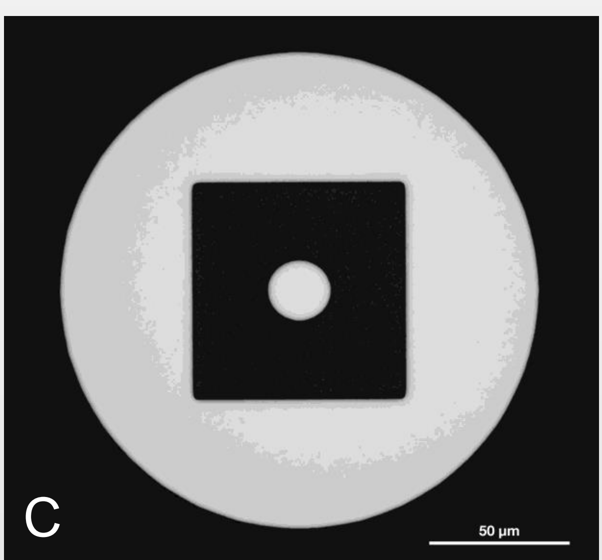


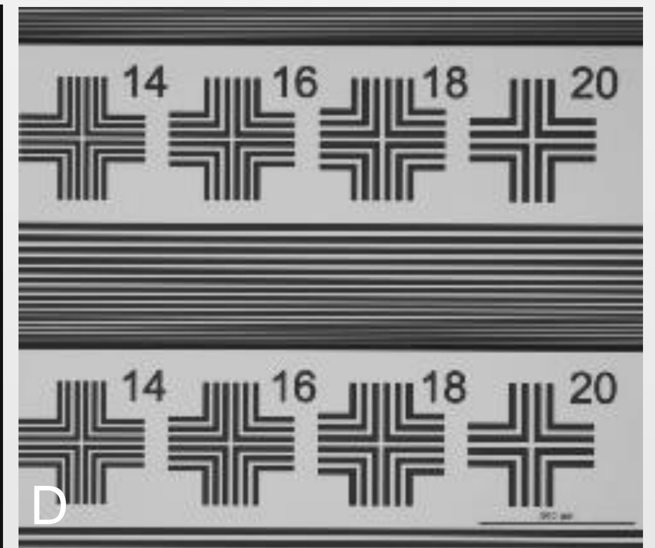


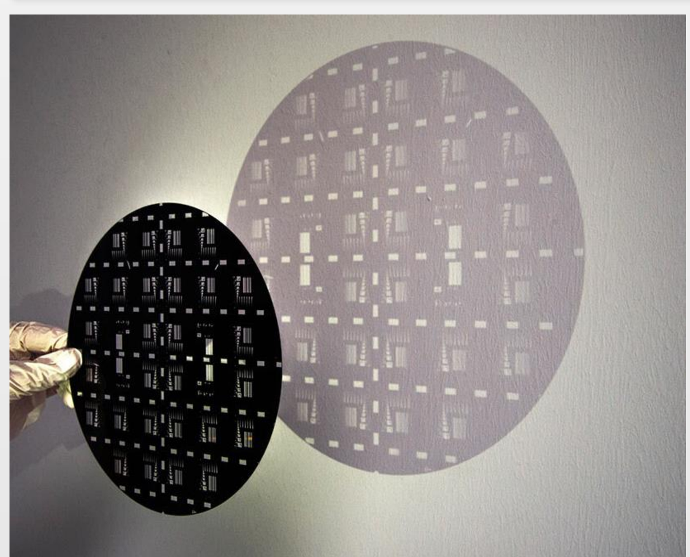
MEMS
→ High aspect ratio, extreme topographies
→ High depth–of–focus
→ Broad variety of designs

PHOTONIC PACKAGING

Neg. Thick Resist LT **100 – 600µm** (A, B)

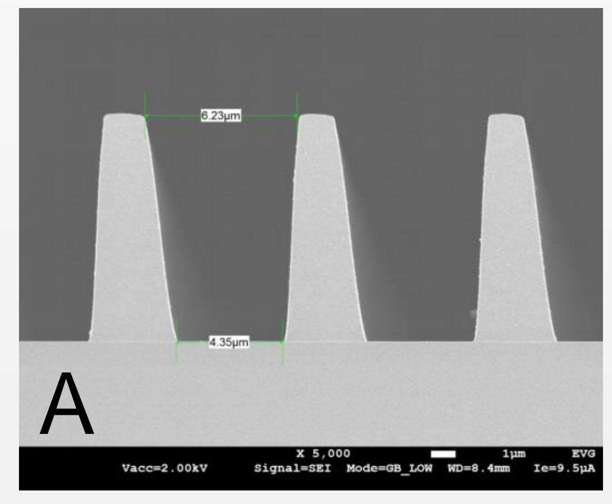


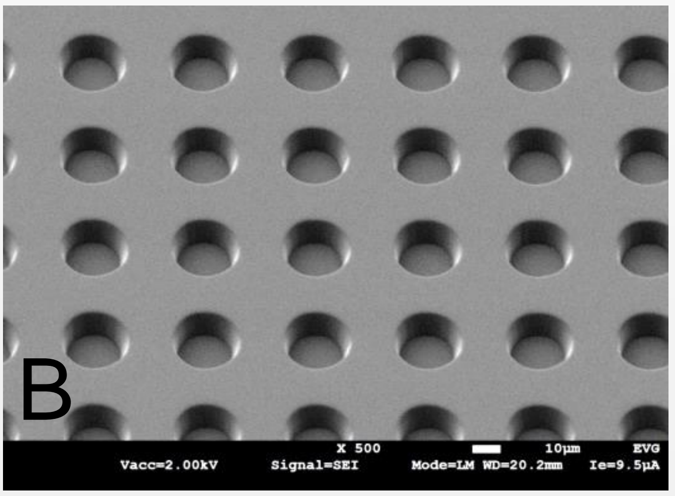




Neg. Black Resist LT **1 – 6µm** (C, D)

EV Group MLE™ | LITHOSCALE® Applications & Process Results

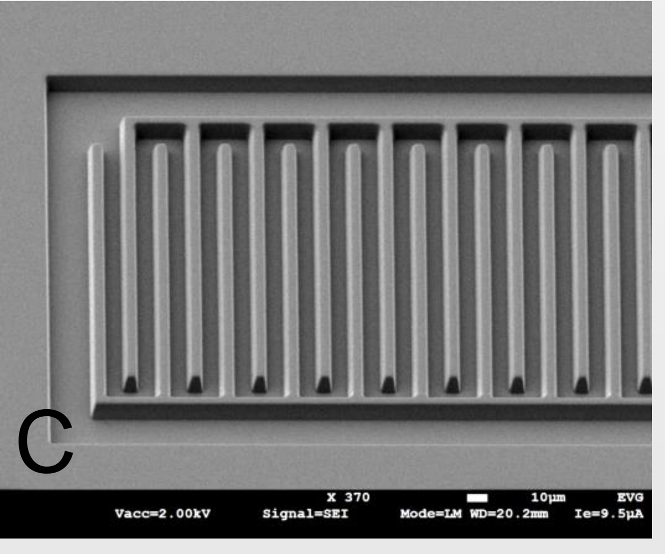


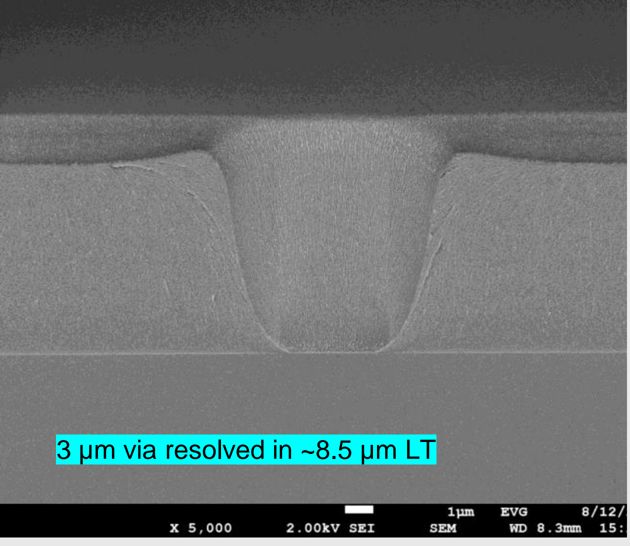


ADVANCED PACKAGING
Numerous layouts, distortion compensation

DIELECTRICS
→ Buffer layer for stress & thermal optimization

Pos. Resist
LT **7µm**, AR 2:1, sidewall angle: 82°
(A, B, C)





PI Layers evaluated for FO WLP
→ ultimate goal: scaling down VIA CD
→ Redistribution layer
LT: **7 – 8 µm** (after SB)

Thank you for your attention!

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