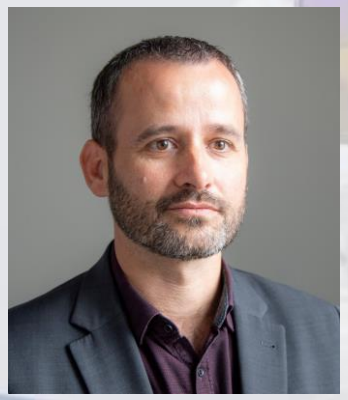

Jean-Luc Polleux
Cofounder & CTO
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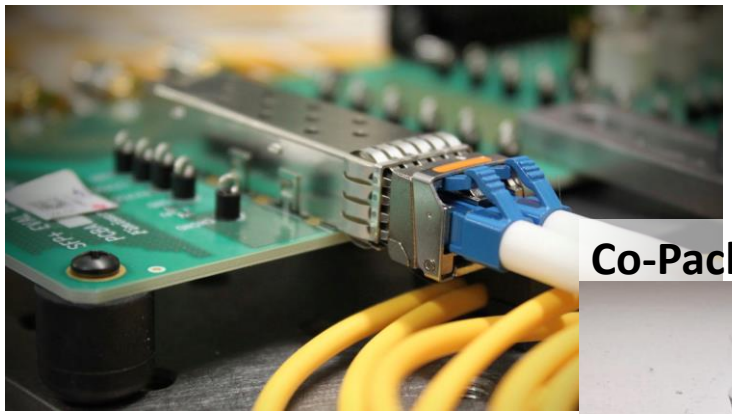
icon PHOTONICS

Integrated Photonics Packaging enabling the Next Generation Optical connectivity

EPIC European Photonics Industry Consortium Proud member since 2018

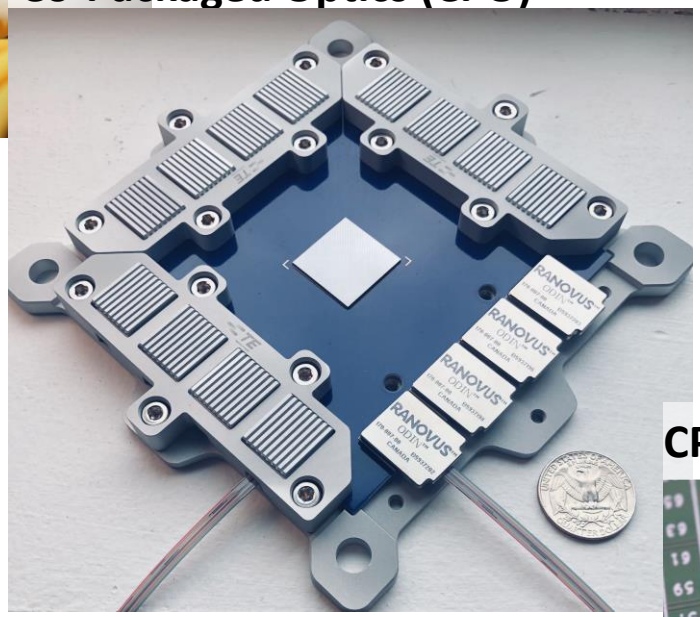
Run for the great shrunk

Pluggable Optics



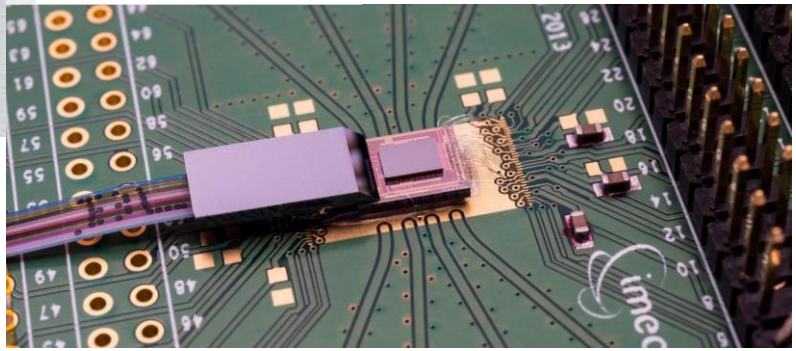
Size ↘ Speed ↗ / Density ↗

Co-Packaged Optics (CPO)



Ranovus 2021, nx100Gbps PAM4

CPO to 3D-chiplet



IMEC Si-PIC platform

80%

Cost/complexity in packaging

Today :
112/224Gbps

2023 :
400/800Gbps

2025 / 2027:
1.6Tbps/3.2Tbps

[Yole 2022]

Quantum supremacy

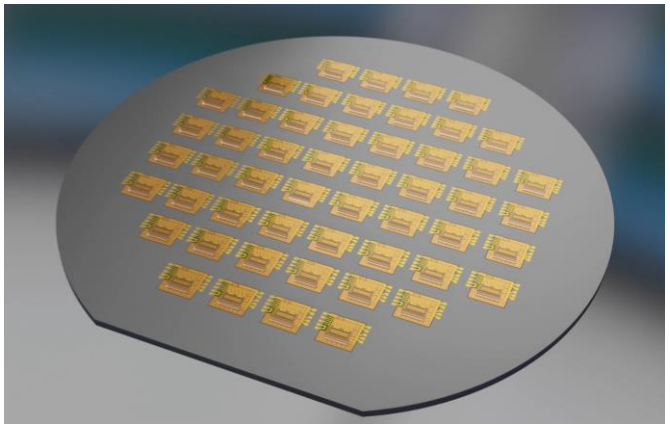
Today :
100/400 Qubits

Needs for >10k/100k qubits
Search for the breakthrough

Google's Sycamore quantum computer
Rocco Ceselin/Google

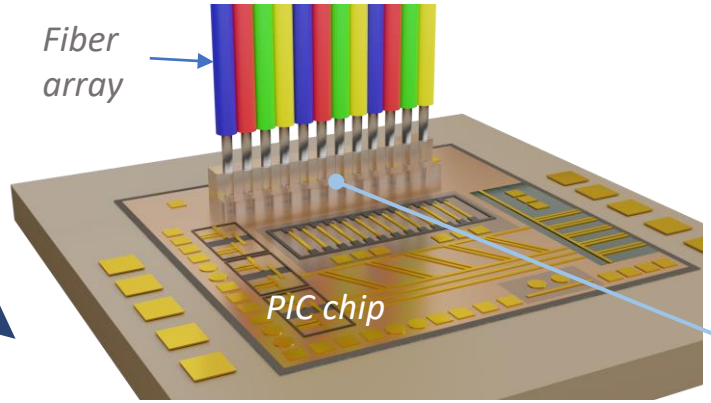
All-in-one-package: Photonics + Electronics + Mechanics integration

Wafer-Level Platform

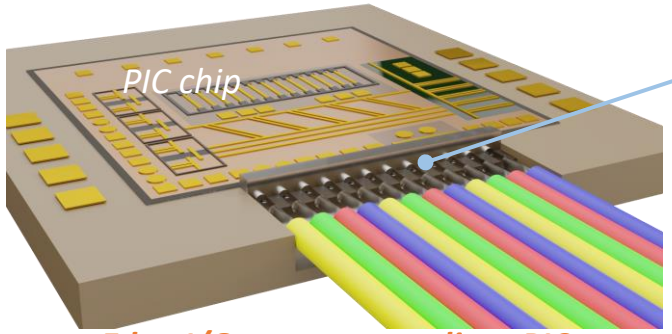


- *UV photolithography*
- *Etching*
- *Wafer bonding*
- *Sputtering*
- *etc*

Multiple Solutions

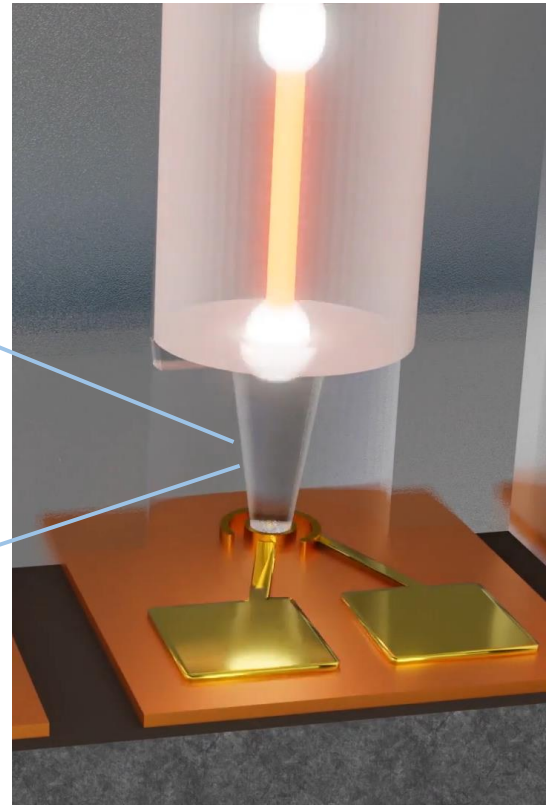


Surface I/O use case on client PIC



Edge I/O use case on client PIC

Low loss coupling

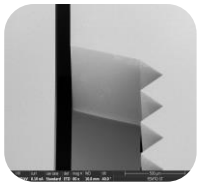
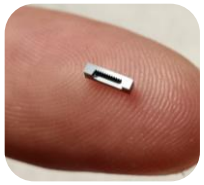
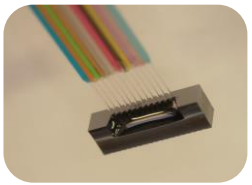


Polymer tapered microoptics

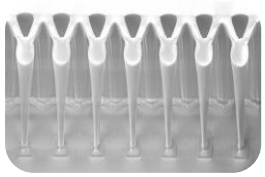
Surface to Edge I/O also available

Technology use-case

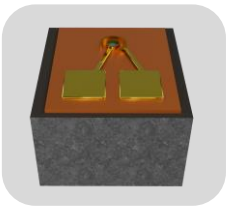
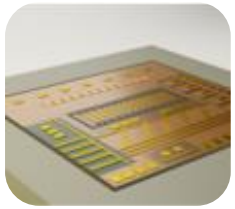
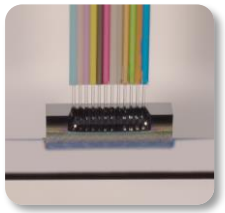
- Mechanical fixture for Fiber array <u>self-alignment and attachment</u>

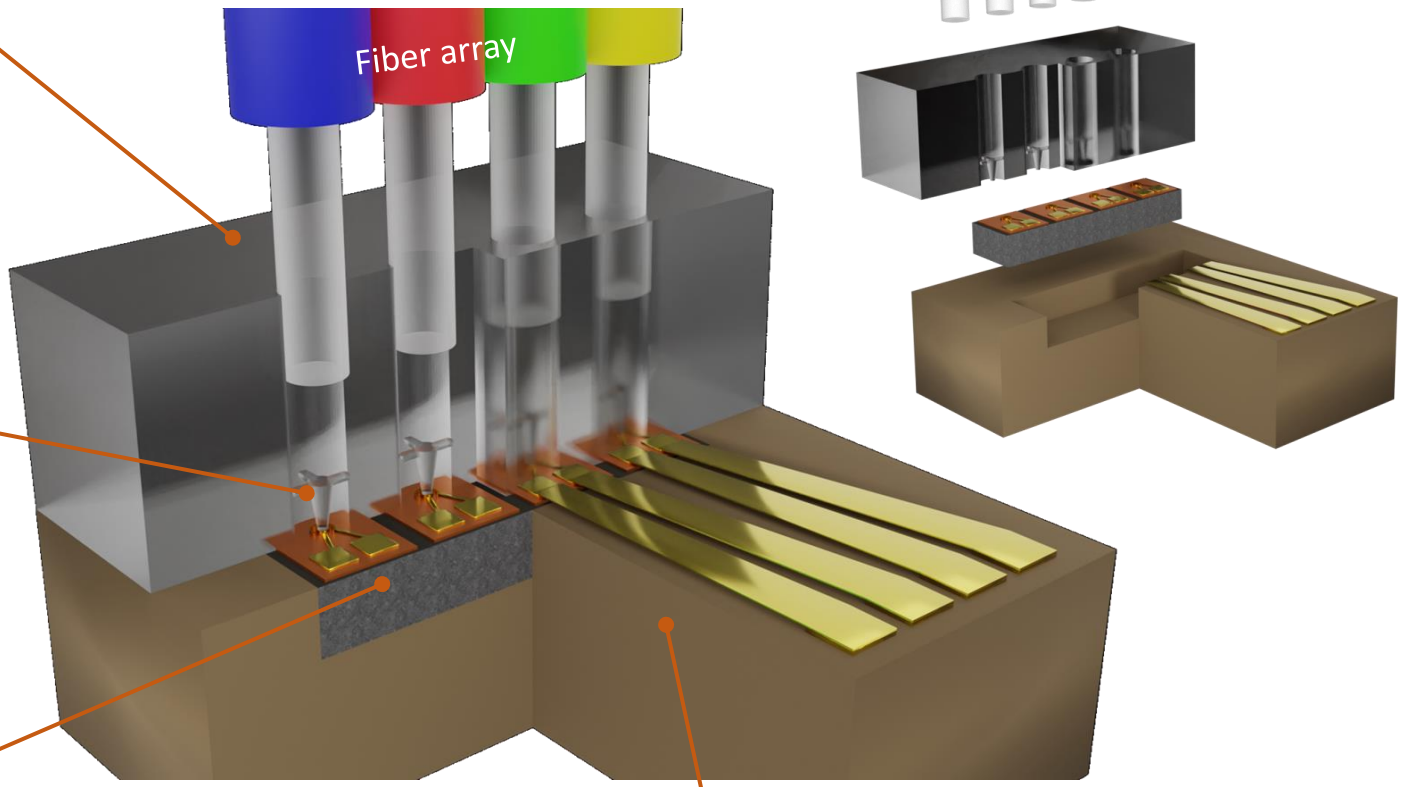




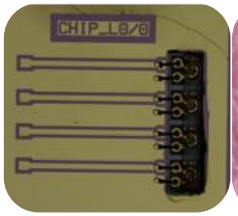
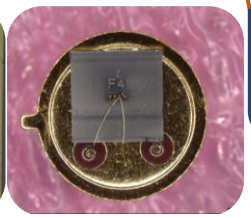
- Polymer Tapered microoptics for low-loss light coupling

- Active device embedding: PIC, Detector, SNSPDs , VCSEL, Laser

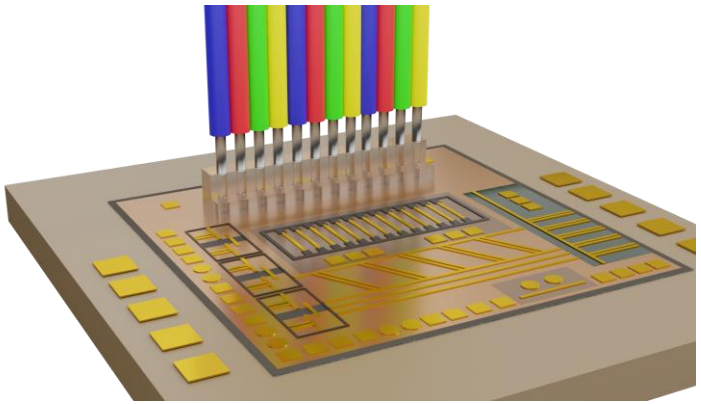


- Silicon Electrical interposer
- RF and mmW transmission lines

From °mK cryogenic to high-temp >350°C conditions

Our Solutions



Surface I/O array

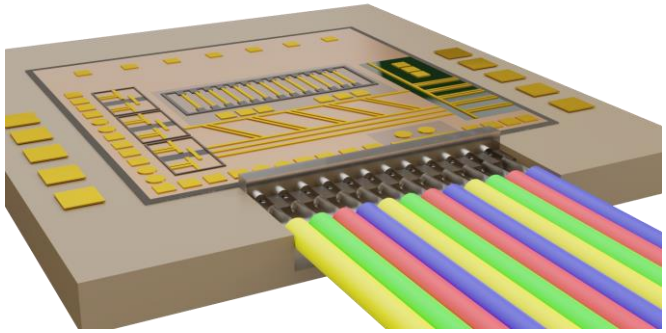
MMF, SMF, MCF
Top / back-side
PD, VCSEL, GC-PIC, SNSPD
Both silicon interposer and full-wafer possibilities

SMF and MMF coupling losses <0.1dB

70µm to 10µm (MMF)

50µm to ~1µm (SMF/MCF)

Fiber holder with passive alignment



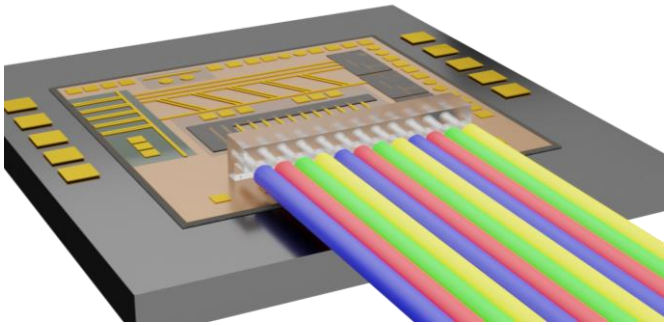
Edge I/O array

EEL, DFB, DBR, Edge-PIC
SSC, MMF, SMF
Both Silicon interposer and standalone possibilities

SMF coupling losses <0.5dB

Active alignment (standalone)

Passive alignment (clipping option)



Surface to Edge I/O array

Upcoming

Advantage of surface I/O array

@All :
- Zero-Air-Gap option or ARC
- Si interposer up to mmw

Collaboration Model

Package development

Contract manufacturing services

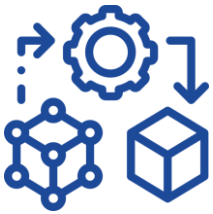
Design and Testing

1

› *Custom-made design to the customer technology and applications*

Fast Prototyping

2



› *Development of the proposed solution*
› *Small series Sampling*

Fabrication and production

3

› *Low to medium volume production*

HVM

4

› *High-volume manufacturing possibilities*

On-stop-shop from design to industrialization

The question

What can we do for you?

› Bring to packagers standalone options to ease their coupling
› Bring to OEM makers higher performances and yield from cryo, RT to HT
› Make it smaller, denser, better

What are we looking for?

› New challenges (>10k qubits, >100Gbps)
› Early-stage adopters
› Exploiting our mass volume capabilities

Feel free to contact us

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