Design For Assembly (DFA) for hybrid integration of prototype PIC’s

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Business Developer Photonic Packaging

PHOTONIC ASSEMBLY

PHIX Mission

PHIX is to become a world leading foundry in packaging and assembly of Photonic Integrated Circuits (PIC's) by supplying PIC based components and modules in scalable production volumes.

- Started operations in 2018 as spin-off from LioniX.
- Today a fully independent pure play packaging facility.
- Moving to a new facility end of the year to continue our scale-up.
- Specialized in hybrid PIC assembly and fiber array interfacing.

PHIX Introduction Video

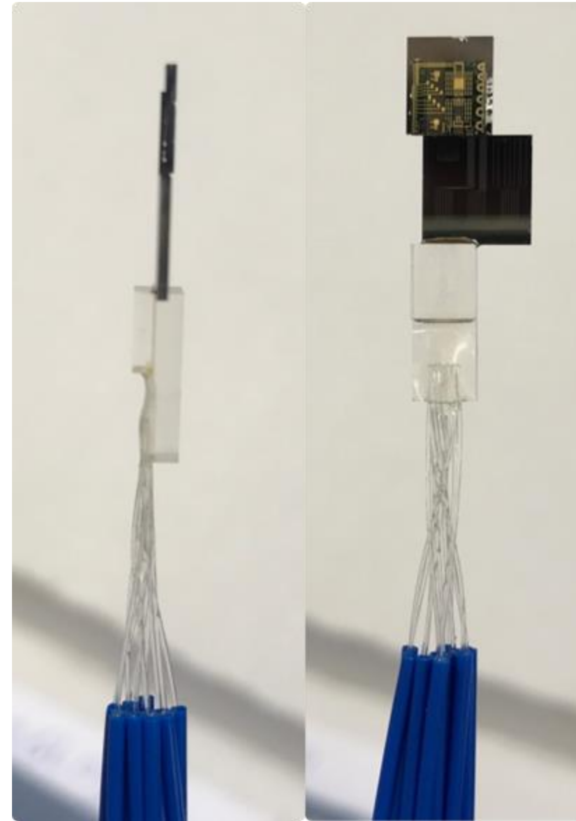
PhiX new 1800 square meters of floor space including 600 for production, including cleanrooms up to ISO-5 for various stages of photonics assembly.

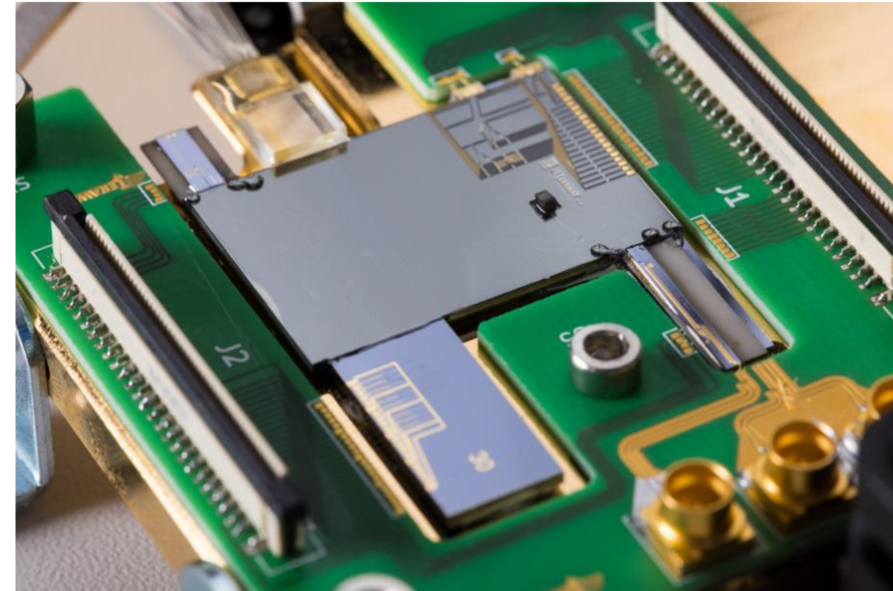
PHIX competences

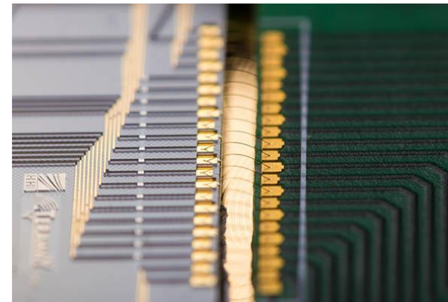
- Product design for assembly and manufacturing

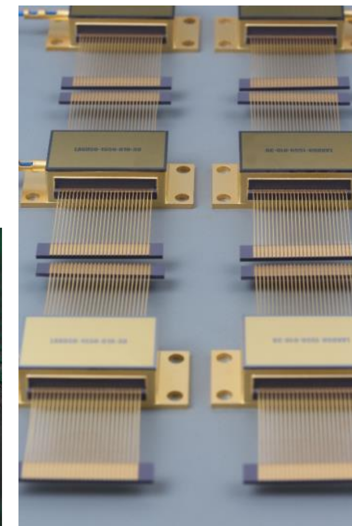
- Supported services:
    - Die preparation
    - Active alignment and bonding
    - Thermal Packaging
    - Electrical interfacing
    - Fiber I/O
    - High Power interfaces
    - Free Space packaging
    - Hybrid assembly
    - Hermetic sealing

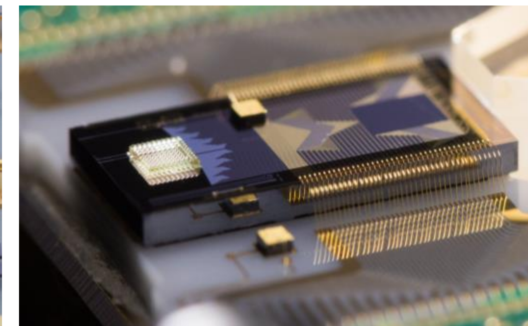
- Capital equipment sourcing and management











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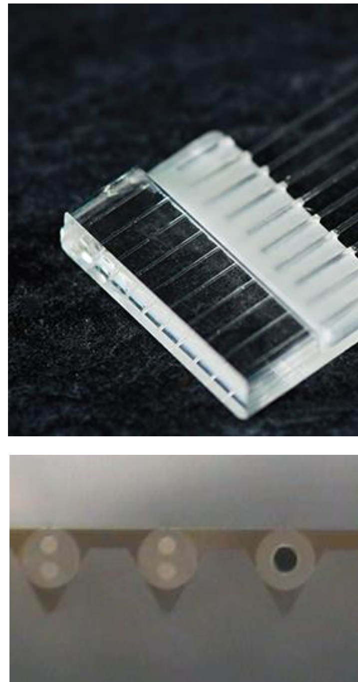
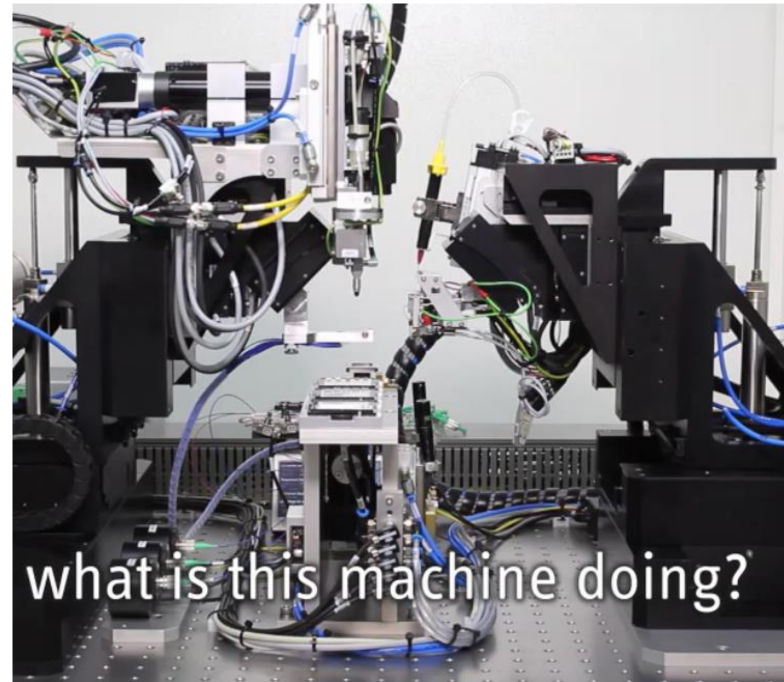
Automated fiber array assembly

Developed with Fraunhofer IPT & Aixemtec



Automated hybrid PIC assembly

Developed with Ficontec equipment



See PHIX YouTube channel

Automated flip-chip assembly

With Finetech equipment, Lapda & Femto2

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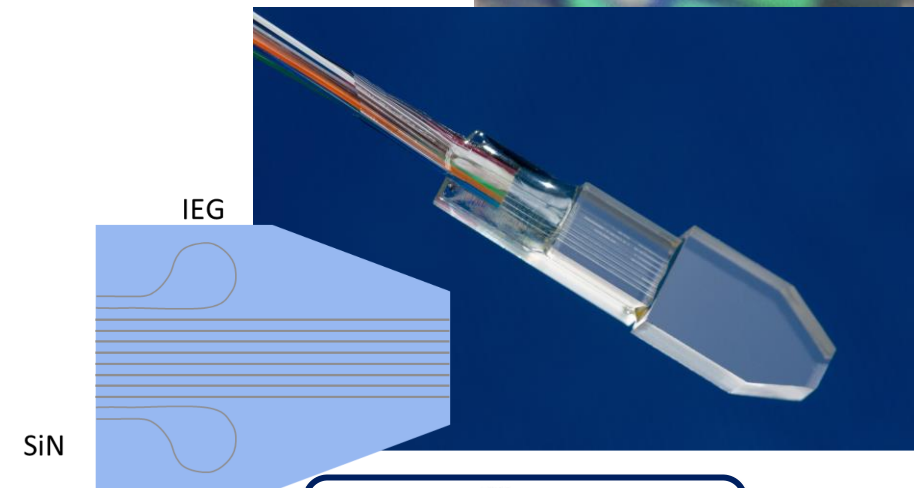
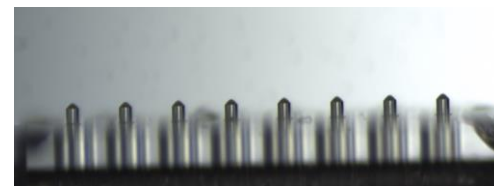
Wide variety of fiber array configurations

- 2, 4, 8, 16, 24, 32, 40 fiber
- Pitches, 127 & 250 microns are standard
- Single Mode, Multimode, Polarization Maintaining
- High NA, SMF 28 small core (visible)
- Flat, 8 degrees, or any custom angle
- Different connector interfaces FC, SC, LC, SMA, MPO
- Different lengths, 1 m default
- Spot Size Converter
- Lensed fiber



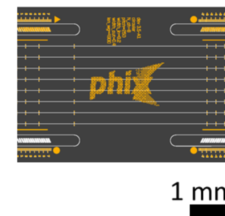


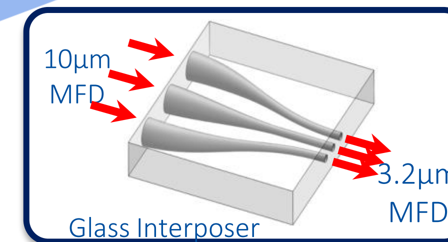
Nanoscribe capabilities

Printing on fibers

Printing on photonic chips

Printing on 3D topographies

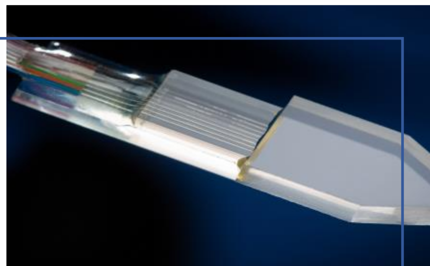


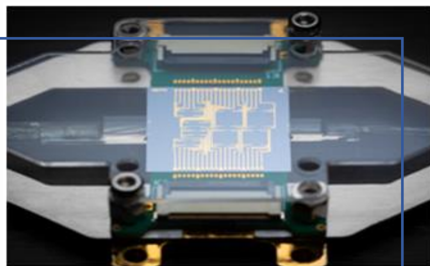


PHIX spot-size-converter-fiber-arrays

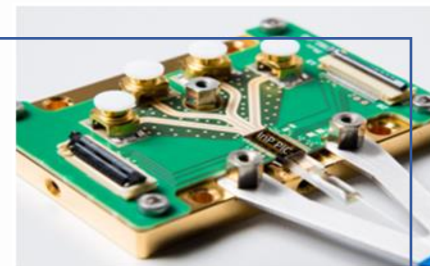
Technologies

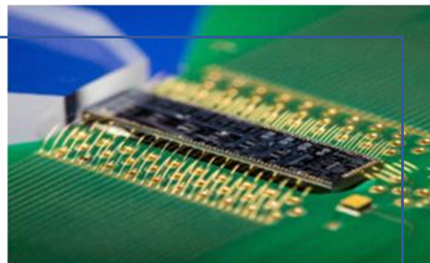
Assemblies


Fiber Array + SSC

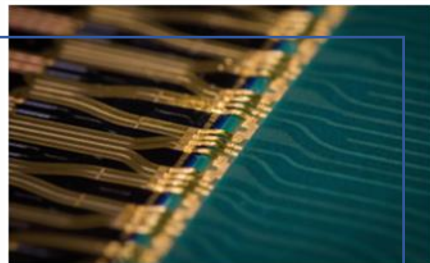

Characterisation Package

Hybrid-Integrated Transceiver

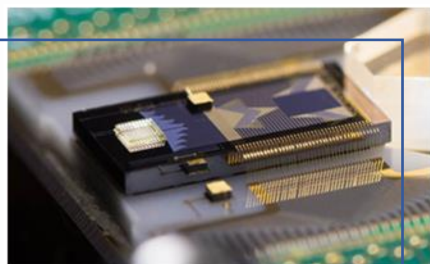

InP Tranceiver

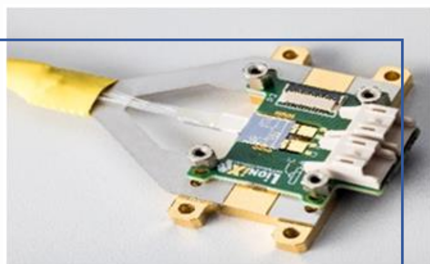

High Density Wire-bonding

RF Prototyping Board

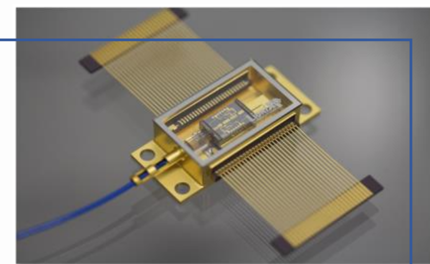

Ribbon Wire-bonding

Mobile 5G Receiver

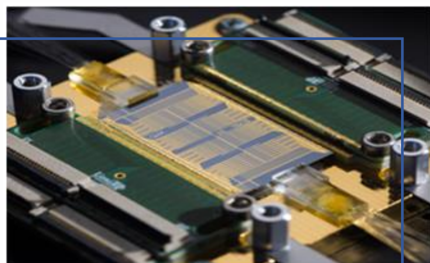

Printed Microlens Array

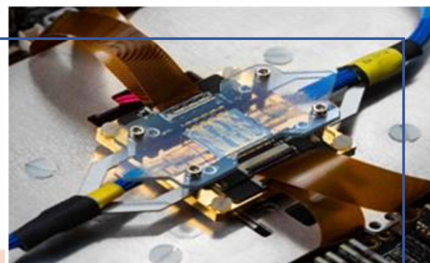

Dual Gain Tunable Laser

SiPh-Transciever


Tunable laser

Bio Sensors


Quantum Processor


Quantum Processor

Quantum Processor System

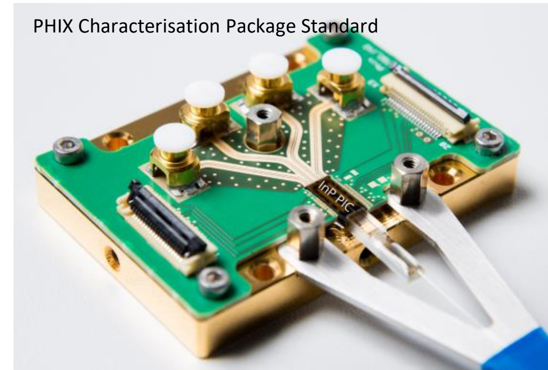
Package types for PICs

Characterisation & Prototype Packages

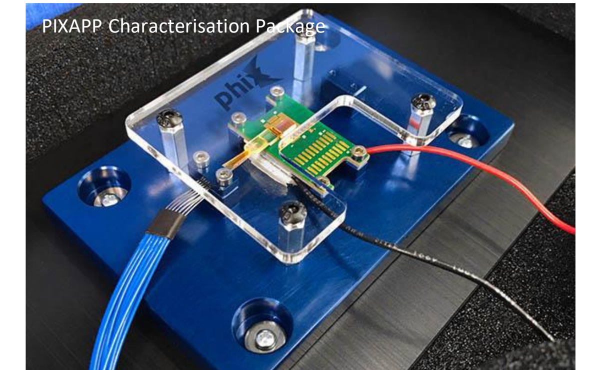
- For PIC characterisation with easy access.
- Design for Assembly (DFA) for quick turn around.
- Packaging guidelines support the standardisation of the process steps.

Low-volume/high-mix Packages

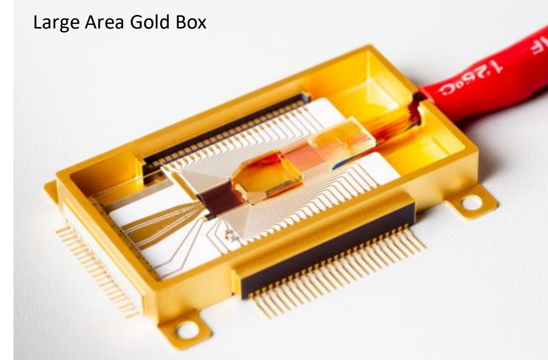
- Automate not for volume but for reliability.
- Use of space compliant materials and processes.
- Packaging guidelines support the standardisation of the process steps…for space.
- …Design for Manufacturing and Assembly (DFMA).

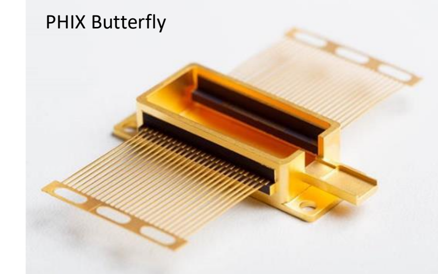


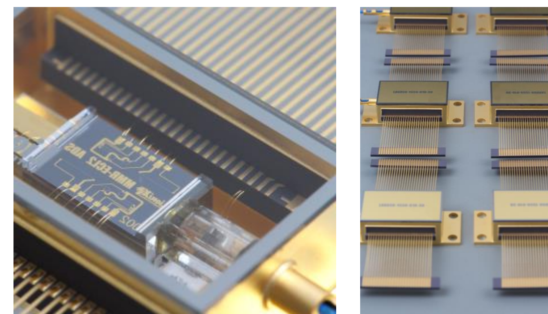
PHIX Characterisation Package Standard

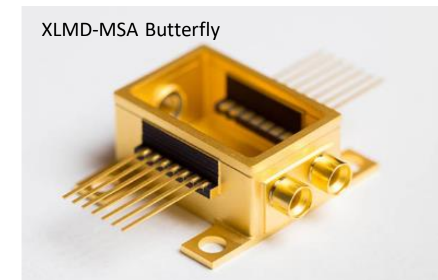


PIXAPP Characterisation Package


Large Area Gold Box

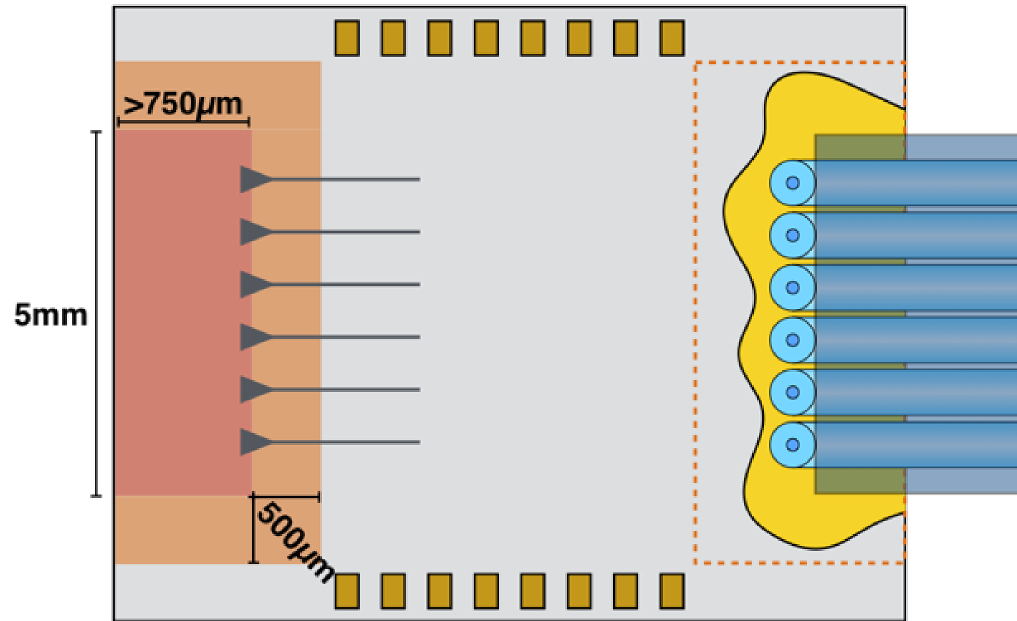

PHIX Butterfly

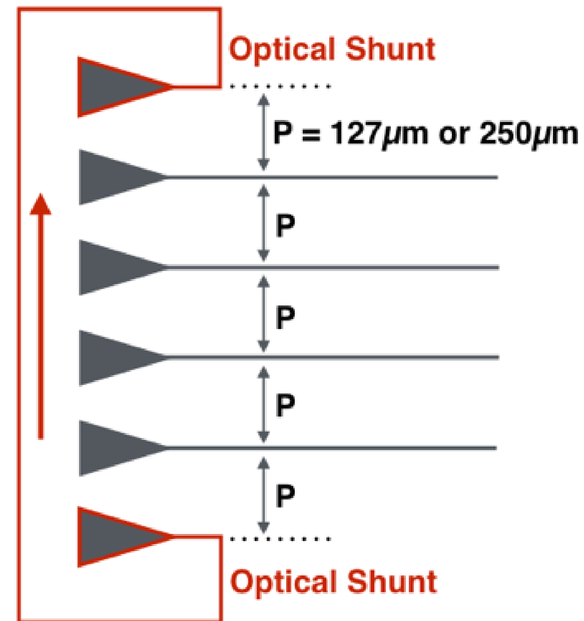


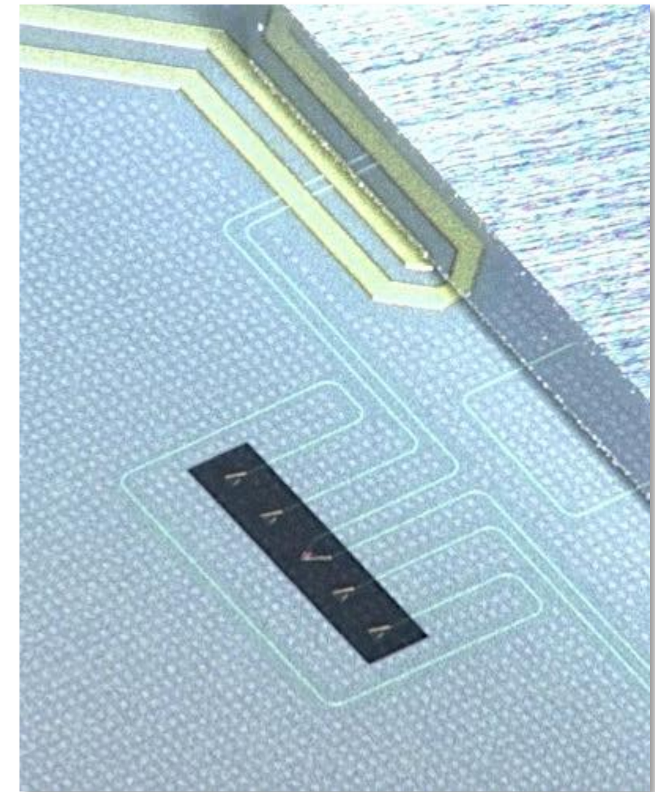

XLMD-MSA Butterfly

Design for assembly → design guidelines

PIXAPP Photonic Packaging Pilot Line







Our Design Guidelines

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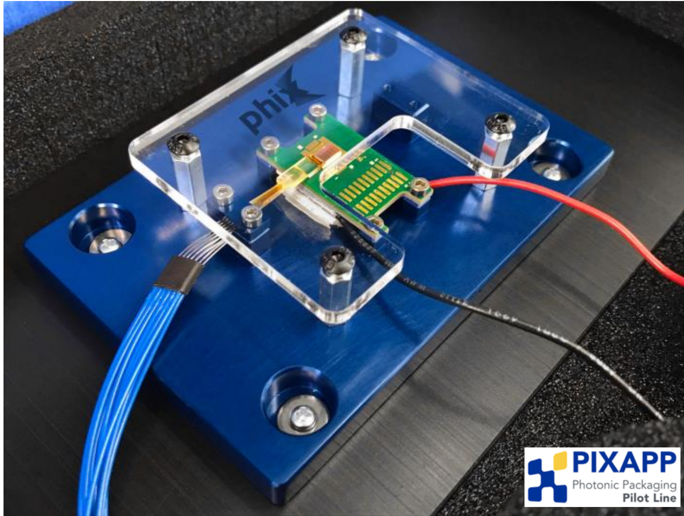
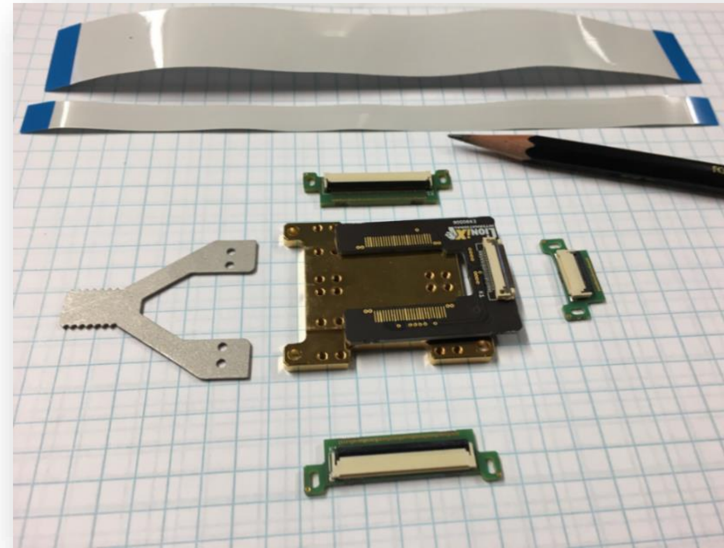
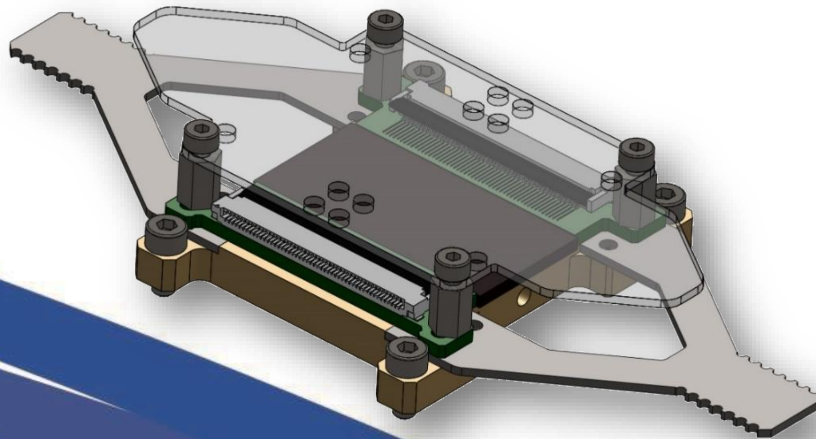
PHIX Characterization Packaging Service (CPS)







TERAWAY Consortium

12 Partners
6 EU countries

3 Large Companies
4 SMEs
2 Industry-oriented Research Institutes
3 Academic Organizations

Netherlands
LioniX International — SME
phix — SME

Germany
Fraunhofer Heinrich Hertz Institute
Leibniz Ferdinand Braun Institut — Industry Institutes

Finland
Aalto University — Academic Organization
Cumucore — SME

Italy
SM siae microelettronica — Industry

Greece
ICCS — Academic Organization
Optagon Photonics — SME
INTRACOM TELECOM — Industry

Spain
uc3m — Academic Organization
Telefónica Investigación y Desarrollo — Industry

Topic: 5G Long Term Evolution

Type: RIA

Call: H2020-ICT-2019-2

Contract No: 871668

Start date: 1 November 2019

Goal: Leveraging optical concepts and photonic integration techniques, for the **generation, emission and detection of wireless signals** for high-capacity data links

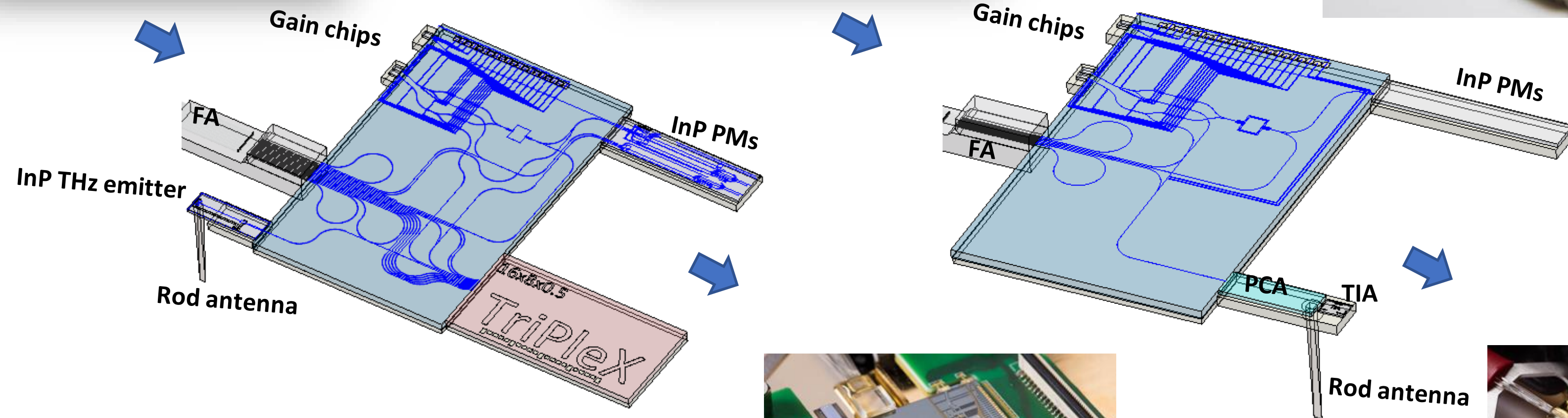
PHOTONICS21 5G PPP

T2.4: Integration methodologies and processes

Module -1: optical subassembly physical model and chip configurations

Functional schematic

Optical subassembly



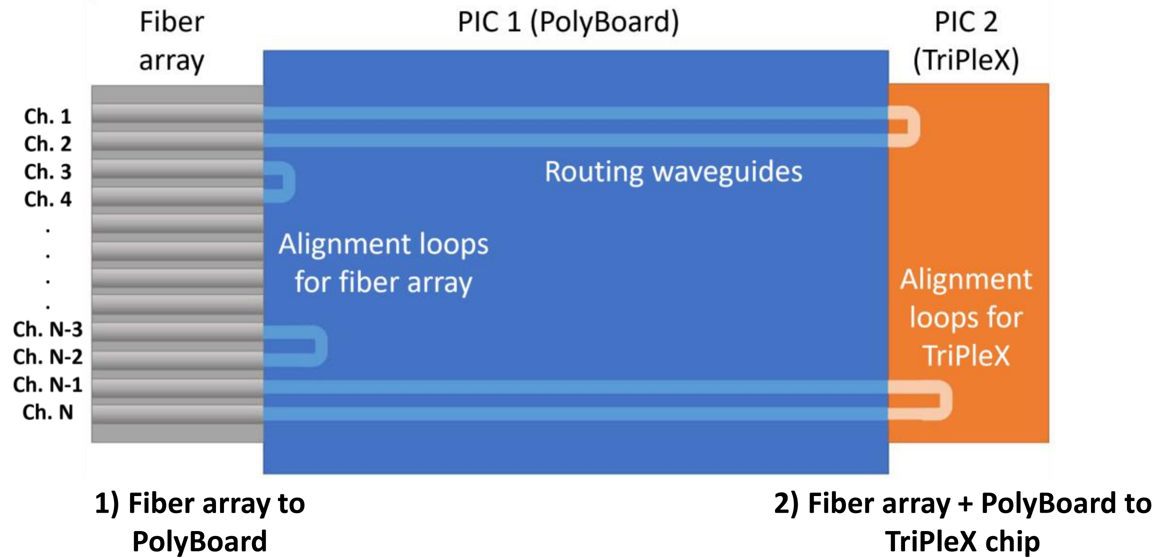
Final assembly

- **PolyBoard as a motherboard**
- **Fiber arrays to facilitate the ingeneration, port monitoring and testing**
- **PHIX design rules require the optical and electrical interfaces to be on different edges**
- **Multiple optical interfaces/components can coexist on a single edge if spacing requirements are respected**

T4.2: Development of the integration /packaging engine

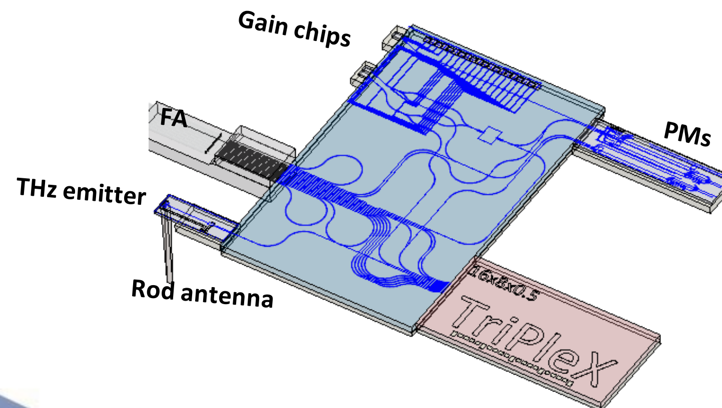
Module -1: Optical alignment and packaging methodologies

Loopback Active Alignment

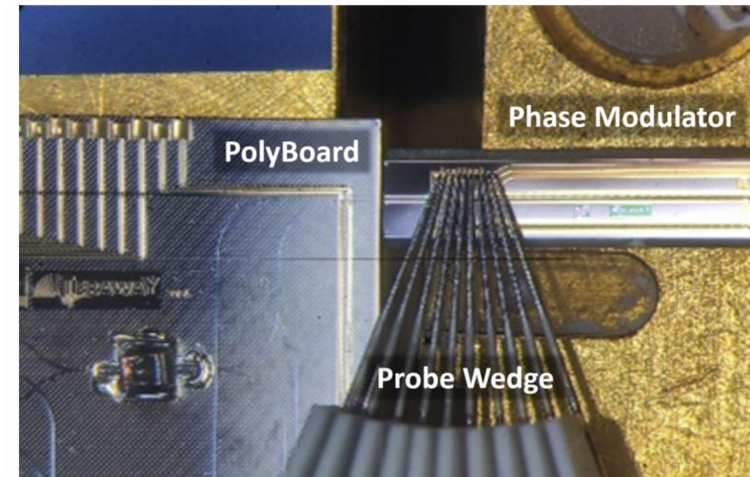


1) Fiber array to PolyBoard

2) Fiber array + PolyBoard to TriPleX chip



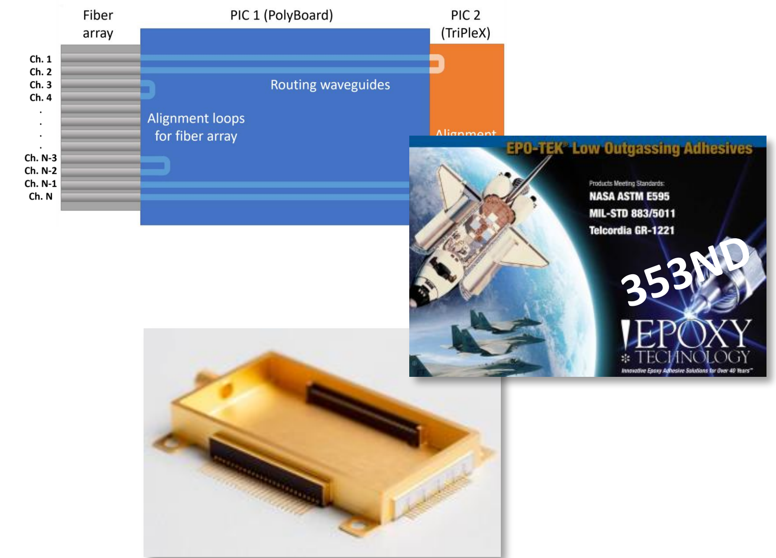
Electro-Optical Active Alignment



1) Gain section chips to the PolyBoard
2) PM chips to the PolyBoard
3) InP THz emitter and receiver chips to PolyBoard

What can we do to accelerate the movement of PICs from Earth to the NEWSPACE?

- Apply existing design guidelines to speedup PIC iterations and functional testing?
- Space qualified materials and processes for PIC's?
- Generic PIC housing as test vehicle for Space qualification?
- Create Design guidelines for Space qualified processes to facilitate qualification?
  - Photon Delta Flagship project "PIC's in Space"



PhotonDelta
Gateway to Integrated Photonics

The PhotonDelta Flagship project **"PIC's in Space"** connects the main Dutch industry players in the photonic integrated circuit supply chain to design PIC-based modules for space applications.

Project contact for more information: Paul van Dijk, LioniX

Conclusion

- Design guidelines are essential to keep the industry moving fast forward. Not only to have them but also to use them as much as possible.
- Hybrid integration strategies have been developed.
- Hybrid integrated photonic devices will become a part of the NEWSPACE

What can we do for you / What others can do for us

- Quick packaging turnaround of (hybrid) PICs, based on design guidelines.
- Cooperation on Space compliant Design guidelines by utilizing a standardized package.

Thank You