Monolithic Integration of Photonics and Electronics for High-Capacity Co-Packaged Optical Engines

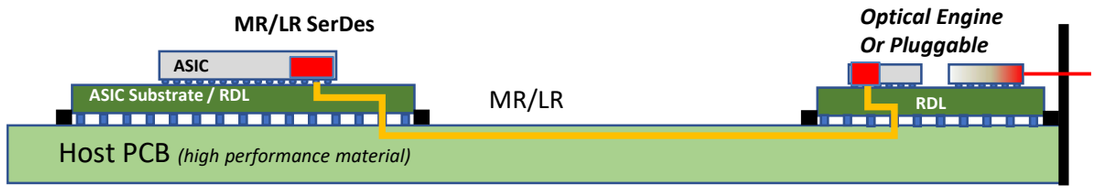
RANOVUS™

Georg Röll

Outline

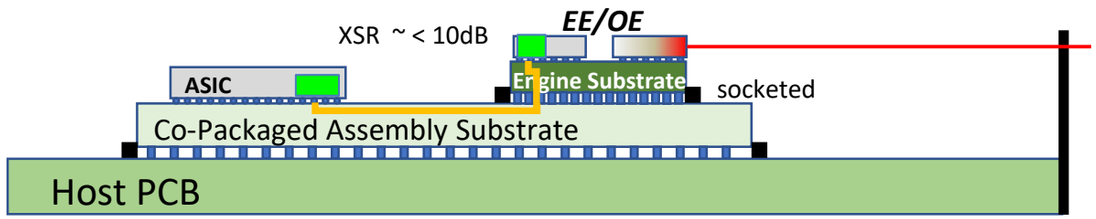
- What is Co-Packing?
  - What are some Co-Packaging Applications?
- Technology Platform for Monolithic EPIC SOC Integration
- End-to-End Transmission Model
  - IBIS-AMI Optical Re-Driver Model
- What did we build?
  - Odin™8P EPIC, ILS Version – Key Functional Blocks
  - Ring Resonator Modulator (RRM)
  - 100G Tx Macro (DRV+RRM)
  - 100G Rx Macro (PD+TIA)
  - ODIN™ EPIC Fiber Attach & Packaging
  - O-Band Lasers for EPIC Integration
- What did we demonstrate at OFC?
  - Test results

What is Co-Packaging?



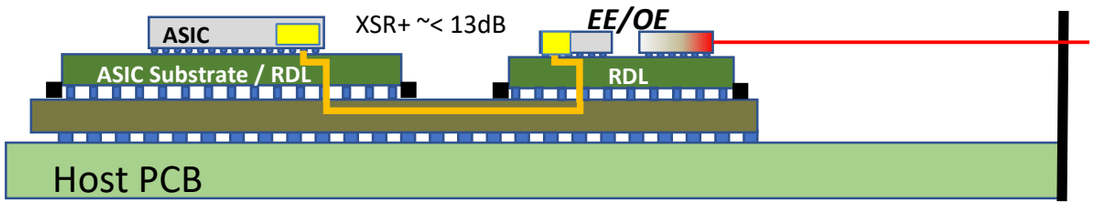
Pluggable or On-Board Architectures

- Pluggable module at the front panel or on-board module
- SerDes I/F can support pluggable or on-board optics



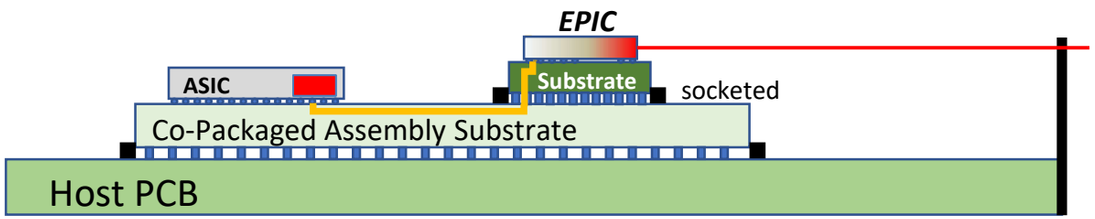
Co-Packaging Architectures

- The Co-Packaging Assembly (CPA) is a Multi-Chip Module (MCM) with either socketed or soldered
- XSR SerDes I/F supports ~50mm reach across substrate and saves SerDes electrical interface power which translates up to ~40% reduction in Ethernet switch card power



Near Packaging Architectures

- ASIC may be packaged and mounted on a high-quality platform (HDI)



Co-Packaging with Analog Drive Architectures

- A MR/LR SerDes can directly drive a non-retimed co-packaged optical engine
- This allows early co-packaging with ASICs which have only LR or MR type SerDes

What are some Co-Packaging Applications?

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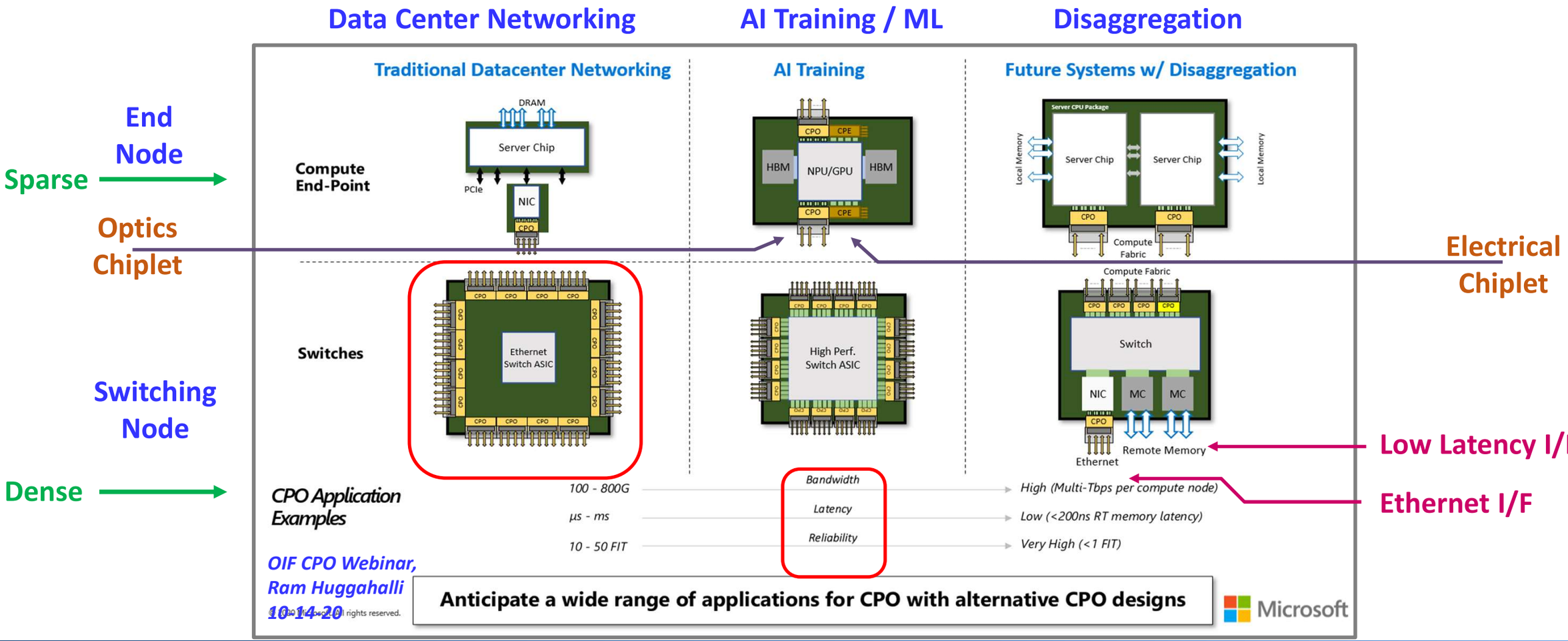
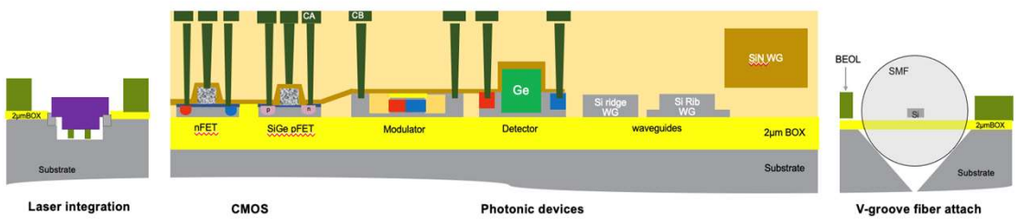


Applications requiring dense optical technologies will drive co-packaging

Technology Platform for Monolithic EPIC SOC Integration

GF 45SPCLO SiPh Foundry Offering
Technology Overview

- High performance photonic passive and actives device library
- Monolithic integration of high performance 45nm RF SOI CMOS
- Dual SOI thickness: 160nm photonics, 88nm CMOS; 2µm BOX, SOI and SiN waveguides
- State-of art 300mm Fab8 Malta Fab, leveraging advanced immersion lithography
- Freeform design enabled with curve-linear GDS with advanced OPC
- Passive v-groove fiber array / attach, 250µm, 127µm pitch
- State-of-Art PDK enablement with EO co-design environment, standard cell digital library
- Automated electrical / optical wafer level test



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Global Foundries material courtesy of Vikas Gupta

Beside using foundry PDK, Ranovus owns or co-develops critical IP:

- Ring resonator modulator (RRM)
- Lasers & laser attach design / process
- Fiber assembly process
- All electronic designs, including RF building blocks and control IP

Benefits:

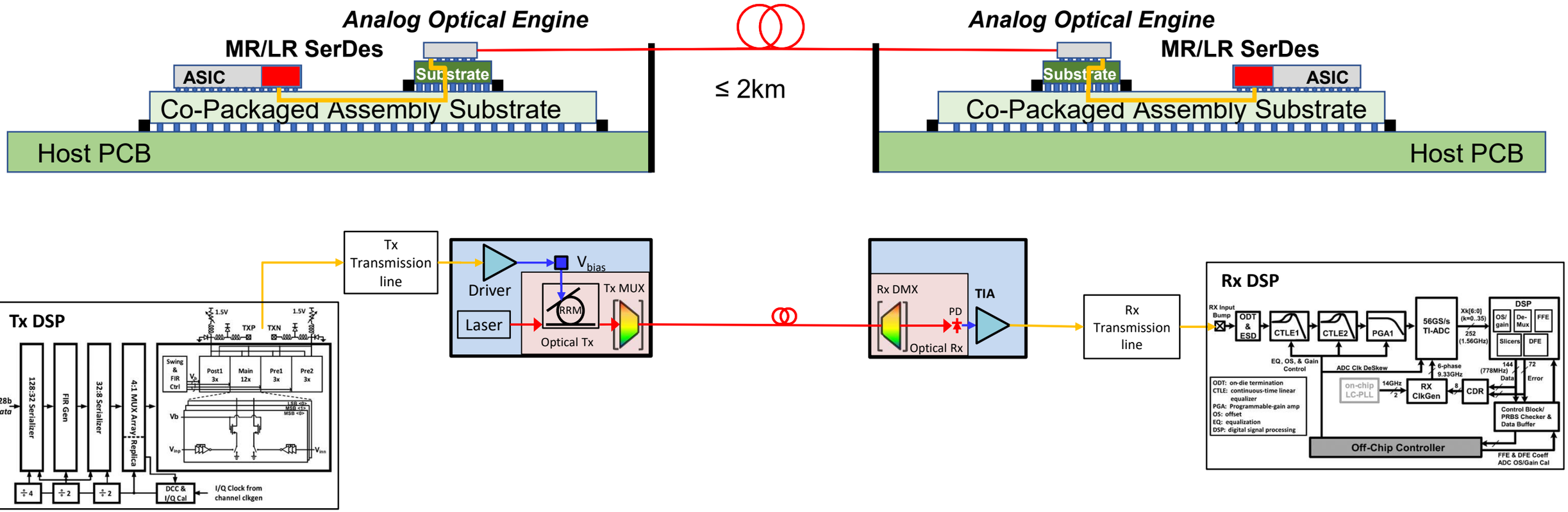
- **Enables a true opto-electronic system-on-chip**
  - Smallest possible size of a solution, as all functional blocks are on single die
  - Simplified packaging (no complex 3D packaging etc.)
- **Super low-parasitic interconnect between photonic and electronic (modulator driver – modulator, Photodetector – transimpedance amplifier)**
  - No impedance matching required
  - Enables best-in-class power dissipation
  - Enables superior TIA noise performance and bandwidth
- **SOI prevents substrate coupling and X-talk**

Challenges:

- **BOX related thermal limitations need to be taken into account in circuit design**
- **No metal allowed in close vicinity of optical waveguides**
  - Routing constrained, as only upper metal layers can be used to cross WG
- **Narrow Si WG have non-negligible insertion loss, should be kept as short as possible**
  - Placement & routing constrained

Ranovus chose Global Foundries' 45nm Process 45SPCLO as the optimum EPIC integration platform

End-to-End Transmission Model



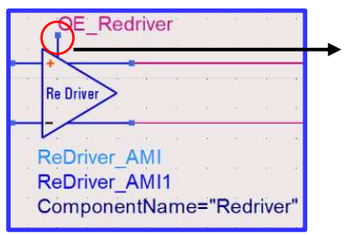
Courtesy: AMD/Xilinx
Reference: DesignCon 2021, Track02 (Best Paper Award)
"End-to-end IBIS-AMI Modeling and Simulations of Electrical/Optical Links"

Transmission Model for End-to-End Link Simulation

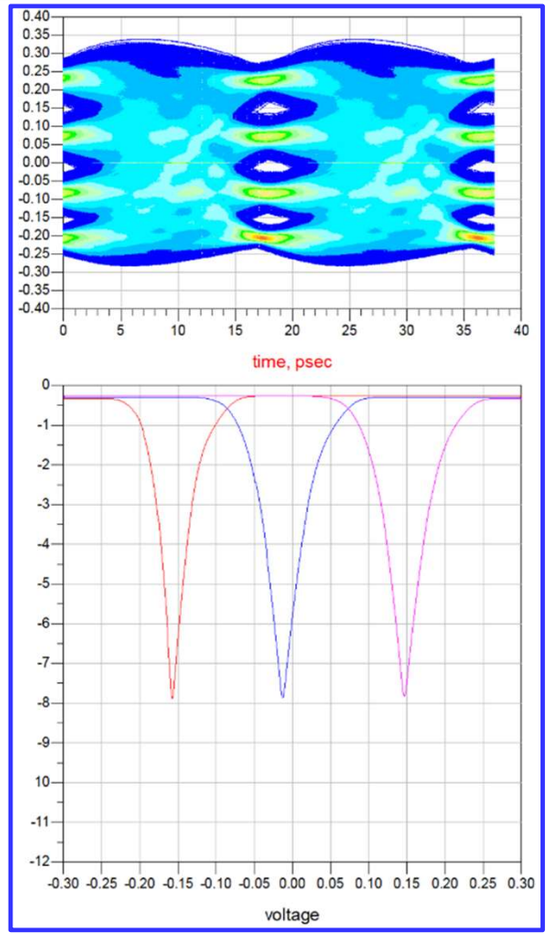
IBIS-AMI Optical Re-Driver Model

Compiled version of Matlab model

- Purpose: Co-simulation of complete electrical-optical-electrical (EOE) chain with packaged Serdes model and s-parameters
- EOE re-driver model variables
  - RRM Detuning Frequency (Hz)
  - Channel Loss (dB)
  - LaserPower
  - Gain (dB)
  - Configuration
  - Modulation
  - ModType
  - DesignType
  - DRVType
  - bePlot
  - Debug



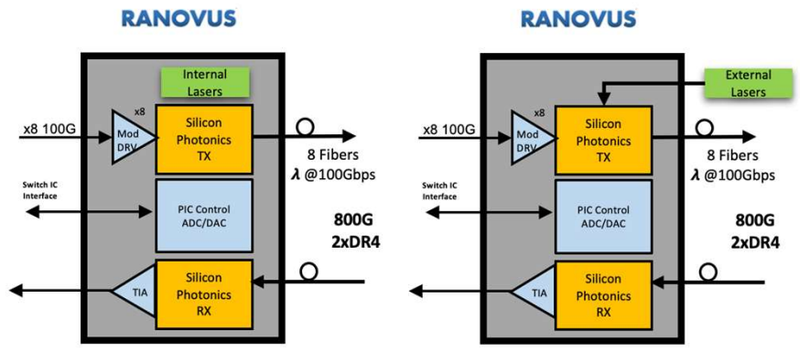
Re-Driver symbol for ADS simulator



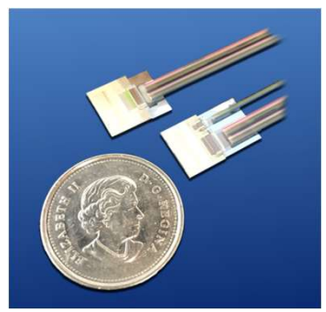
Example: output waveform from IBIS-AMI simulation with Re-Driver model

What did we build?

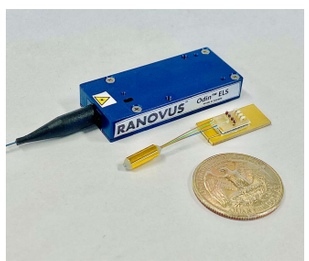
- **Analog Optical Engine (AOE)**
  - Analog drive at 8x 100Gbps PAM4
  - Protocol agnostic (Ethernet, PCIe, …)
  - Low latency ~400psec latency
  - Low power consumption ~5pJ/bit



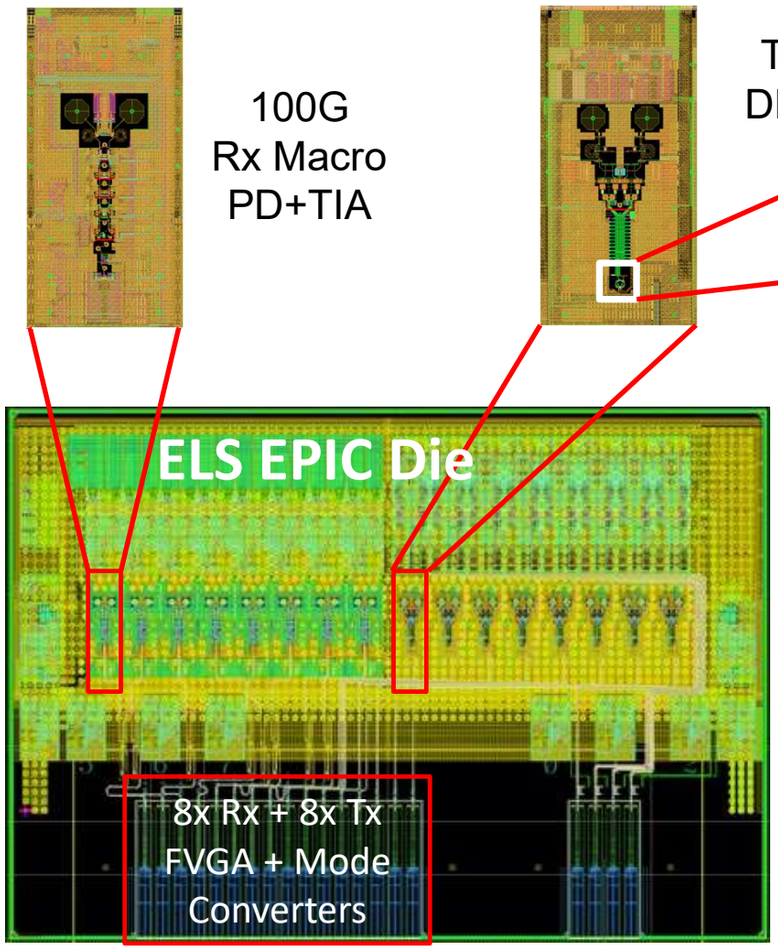
- **Architecture**
  - Optical & electronic monolithic integration
  - Ring Resonator modulators at 100Gbps PAM4
  - Supports On-Die Laser and External Laser Source



- **Fostered an industry eco-system for co-packaging of silicon PICs**
  - OE fiber attachment with optical connectors
  - OE electrical socket
  - OE assembly and test



Odin™8P EPIC, ILS Version – Key Functional Blocks



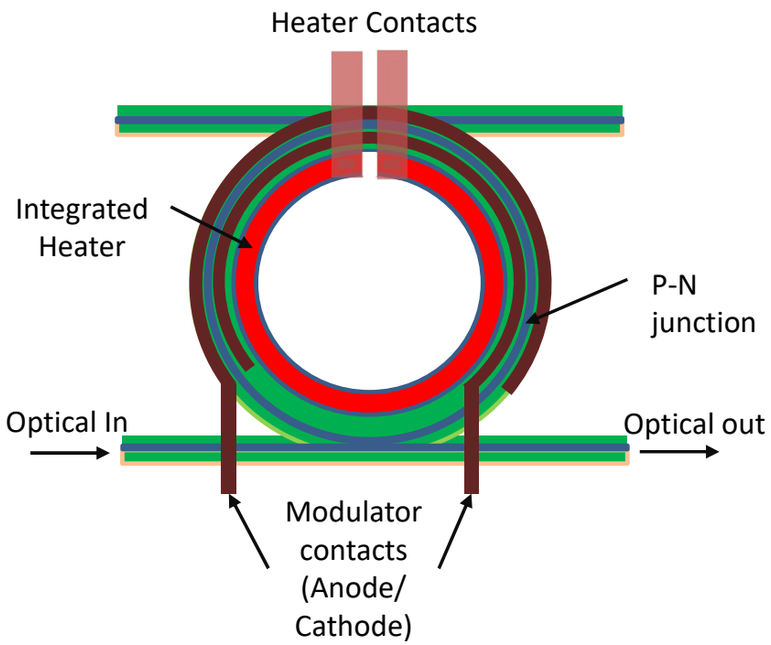
Die size strongly determined by photonics:

- FVGA + mode converters
  - V-groove pitch: 250µm
  - VG + mode converter length: ~2mm
- Laser cavities (in case of ILS)
- Assembly rules related to fiber attach, for things like:
  - Fiber mounting glass block
  - Keep-out zones for underfill or epoxy outflow etc.
- Overall: photonics determine beachfront width

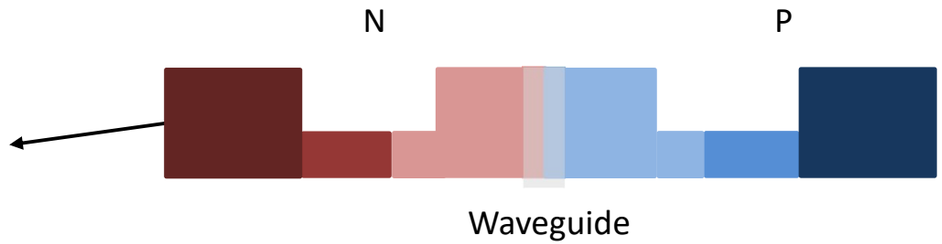
Ring Resonator Modulator (RRM) Design

Parameters to optimize:

- FSR
- Optical bandwidth
- Insertion loss
- Extinction ratio

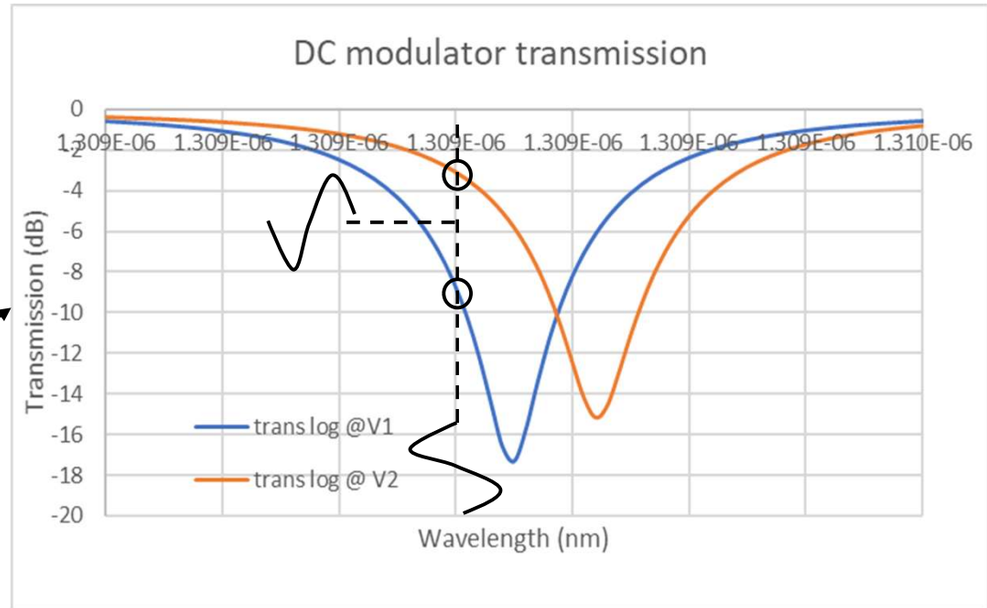


Modulate charge carrier concentration in reverse-biased pn junction



Modulate resonance wavelength

Modulate transmitted amplitude of single-λ input



System Simulation input: Proprietary Dynamic Nonlinear RRM Time Domain Model

100G Tx Macro (DRV+RRM)

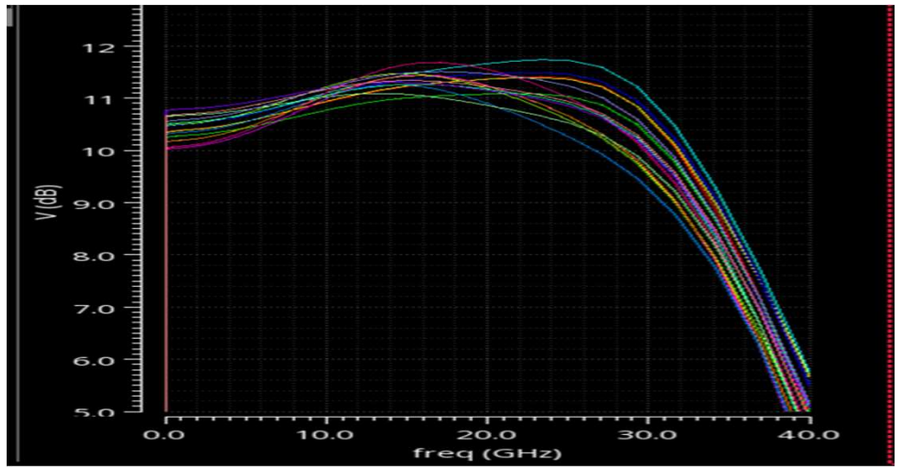
Design Requirements & Extracted Simulation, Samples

Single-stage fixed gain linear RRM driver:

- **Differential Drive Stacked Cascodes**
- **On-chip AC coupling**
- **3dB BW: >40GHz**
- **RF gain: >10dB**
- **Low freq. corner: <50kHz**
- **Min. linear output voltage: >2V$_{diff,pk-pk}$**
- **Single supply: 3.3V**
- **Power dissipation: <100mW**

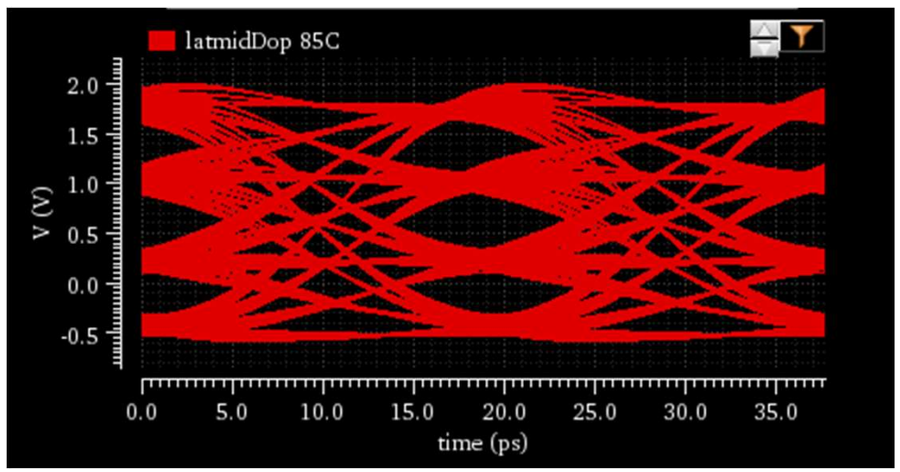
Driver AC response:

- **Voltage gain vs. frequency**
- **Input Port → RRM junction**
- **Corner simulations**



Driver Transient Response:

- **Drive voltage @RRM junction**
- **Ideal input PRQS waveform**
- **Typical corner, high T**



System simulation input: time domain waveforms or frequency responses

100G Rx Macro (PD+TIA)

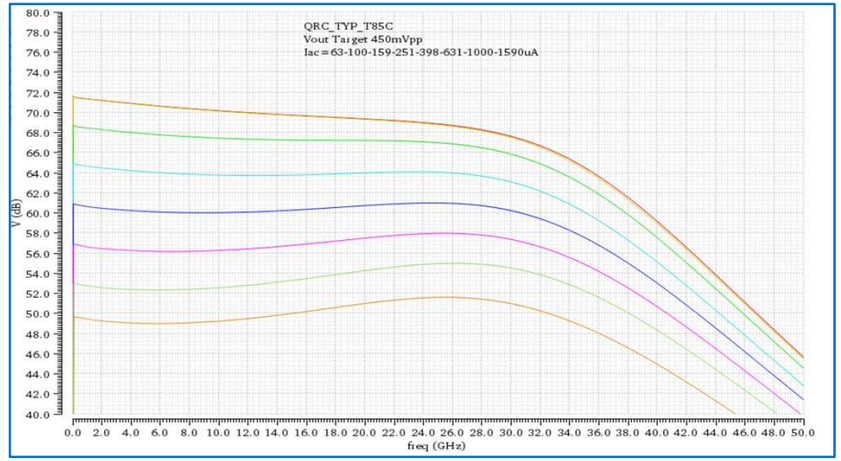
Design Requirements & Extracted Simulation, Samples

Multistage O/E Converter Amplifier :

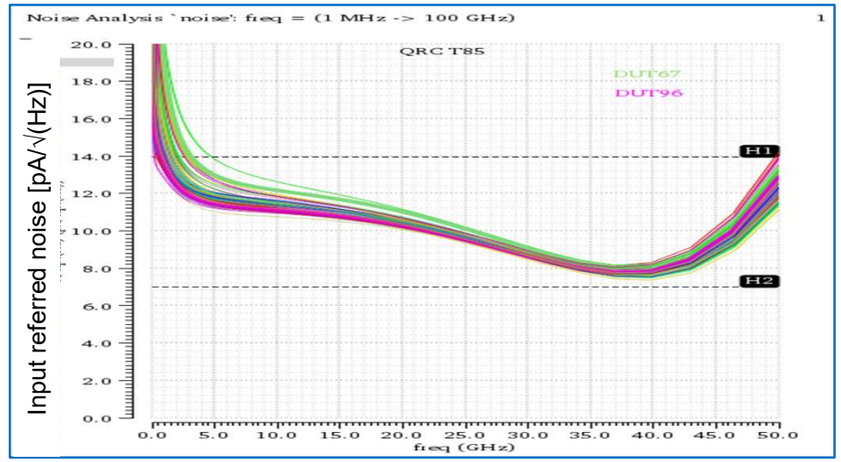
- **TIA + SE/Diff + 3xVGA + Buffer**
- **3dB BW:** **>30GHz**
- **TIA max gain:** **>72dBΩ (4kΩ)**
- **Output Swing Target:** **450mV$_{diff,pk-pk}$**
- **Input referred noise:** **<14pA/√(Hz)**
- **Performance PVT-stabilized**

- **Single supply:** **1.8V**
- **Power dissipation:** **<120mW**

Typical AC Magnitude Response over Gain Setting @ 85 °C



Input Referred Noise Spectrum, Monte Carlo Simulation @ 85 °C / max gain

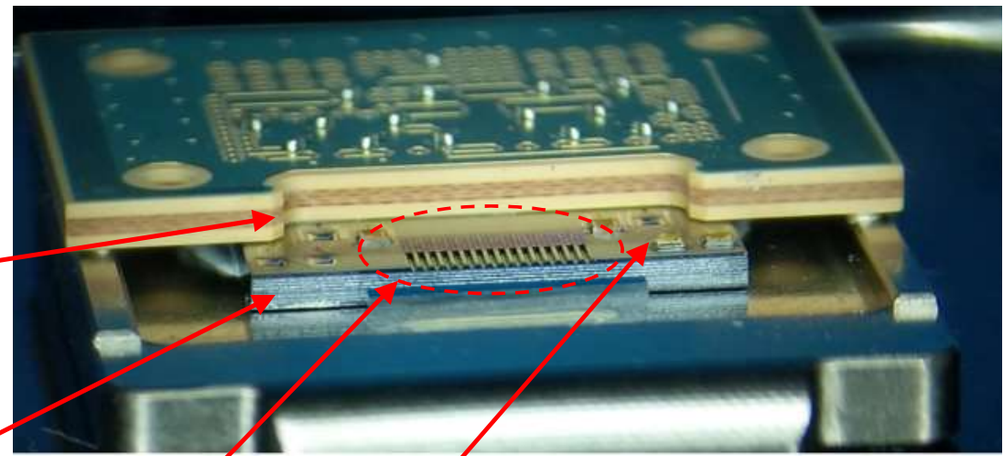


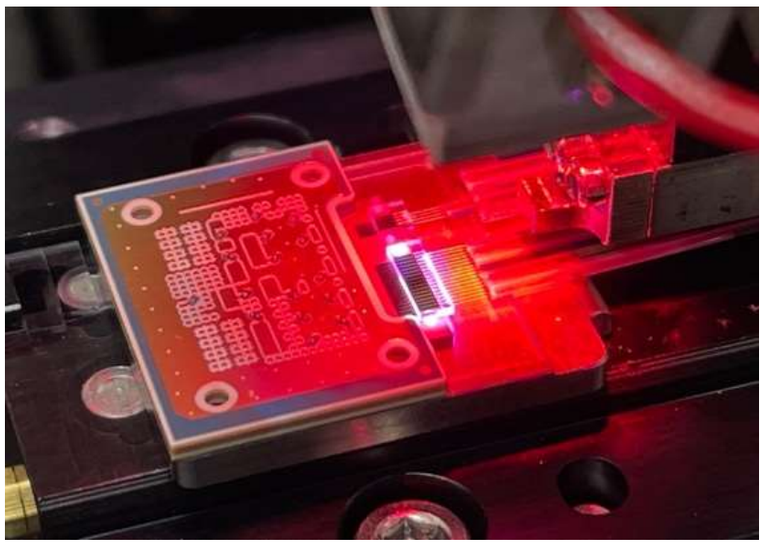
System simulation input: time domain waveforms or frequency responses (e.g. magnitude, phase + noise spectral density)

ODIN™ EPIC Fiber Attach & Packaging

16 Fiber passive V-Groove attach system

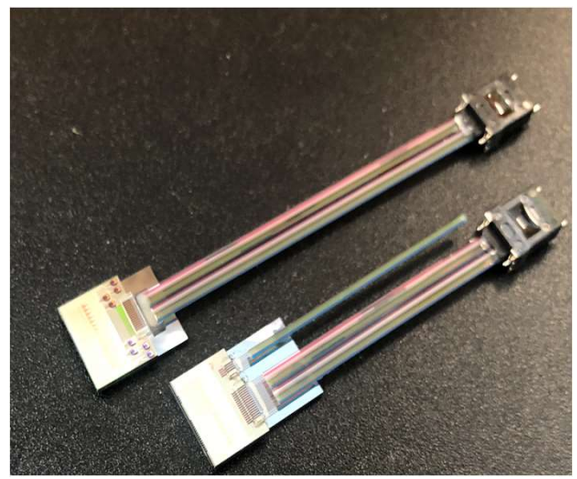
- Flip-chip technology used for SiP with V-Groove
- Passive attach of 16 fiber array
- Performance Targets:
  Insertion Loss <2dB per facet/connection - across complete 16 channel fiber array
- Reliability:
  Telcordia Damp Heat, High-Temperature Storage & Temperature Cycling





EPIC on fiber assembly station

EPIC variants with fiber array attached to FVGA

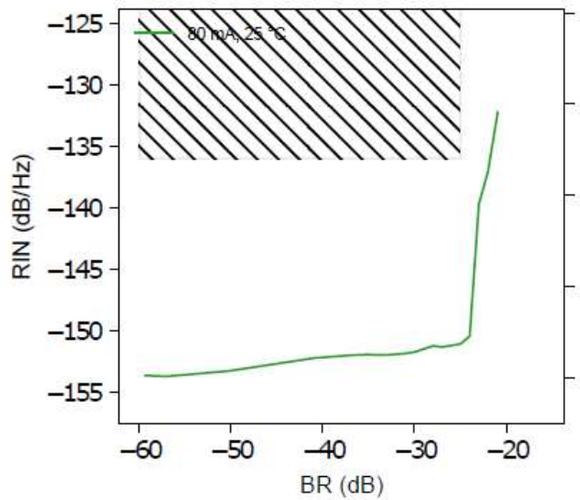


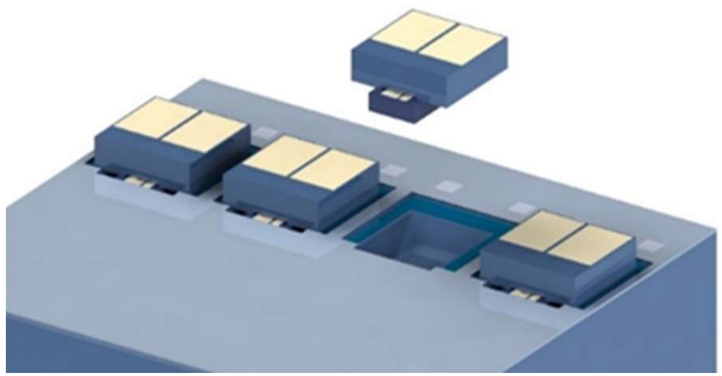
O-Band Lasers for EPIC Integration

ILS concept

- **Odin™ DFB O-Band Laser**
  - **Co-Designed to support SiP Optical/Physical Interface**
  - **Optical**
    - Designed for backreflection (BR) resilience
      - Isolator free interface
    - RIN (Relative Intensity Noise) performance under BR
    - Power/Size Efficiency
  - **Physical**
    - Size minimized for EPIC mounting
    - Customized for precise passive mounting
- **Innovative laser mounting mechanism, supporting**
  - **Mounted/soldered laser and test before attach**
    - Relaxed tolerances for submount attach
  - **Burn in capability before attach**
  - **Features and facility to perform machine vision/optical alignment**

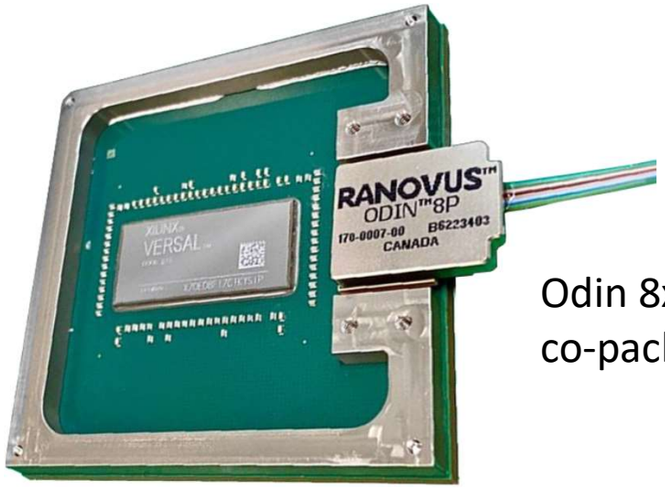
ILS Backreflection Resilience – RIN vs. BR



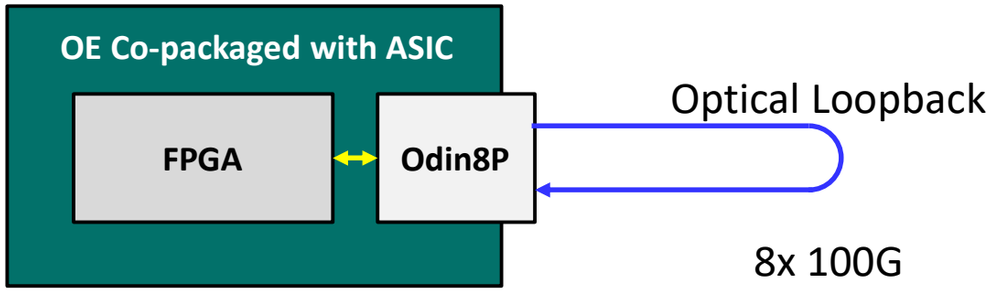


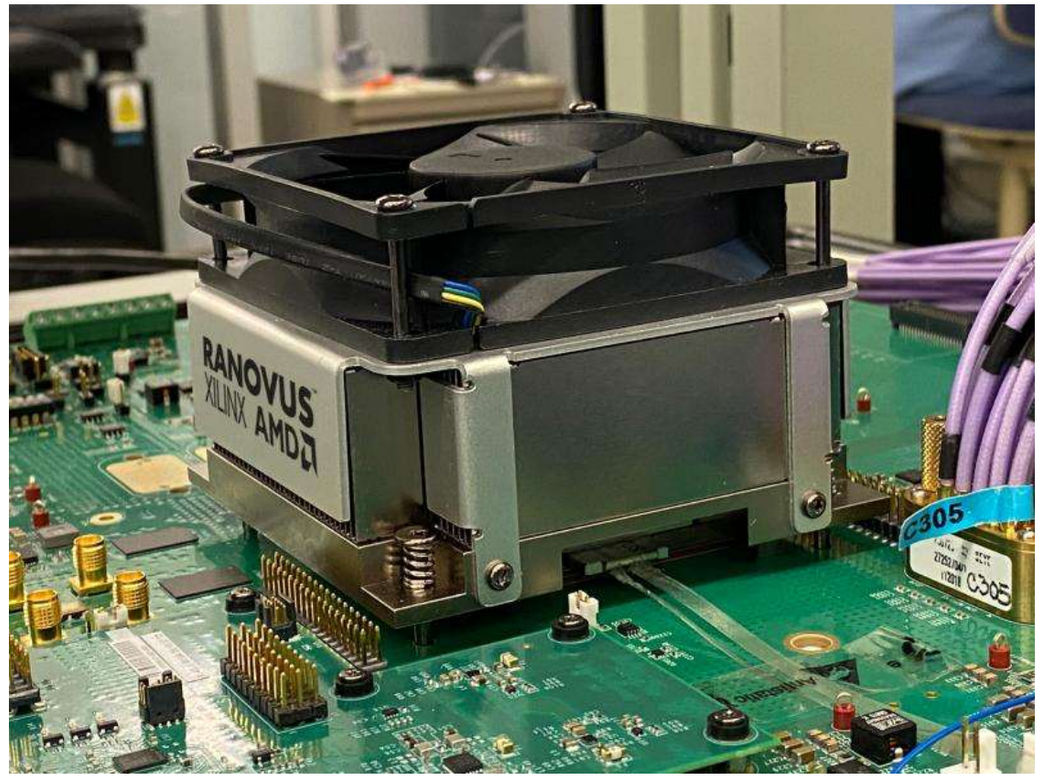
Patent application US020210364694A120211125 (storage.googleapis.com)

What did we demonstrate at OFC?



Odin 8x 100G analog optical engine co-packaged with an AMD FGPA

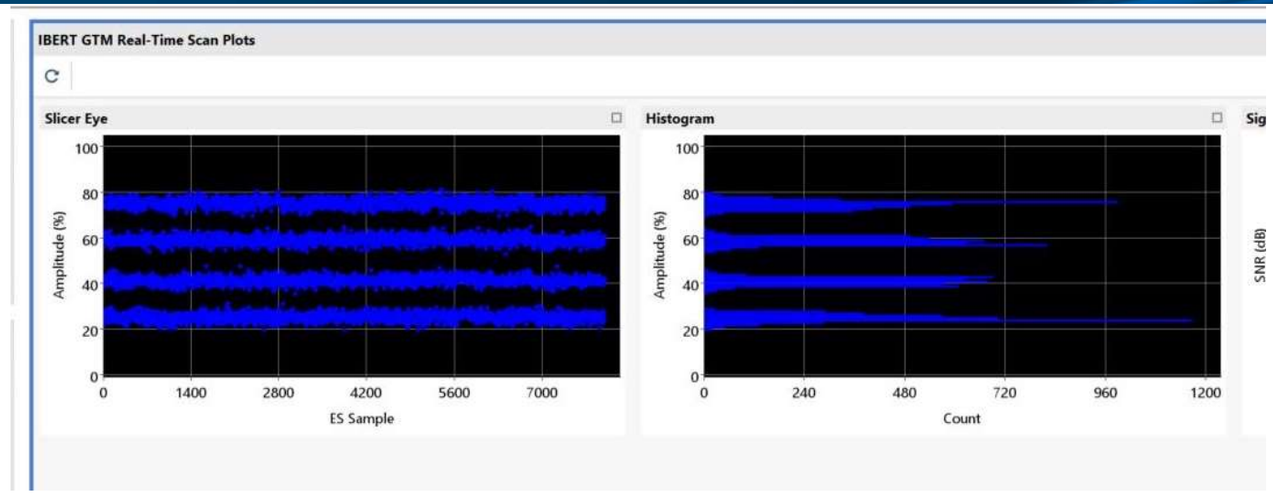




2022 Analog Drive CPO 2.0

Demonstrated error free Ethernet links for 100G/λ

106.25Gbps PAM4 Fiber Loopback BER



100G PAM4 - Slicer Eye & Histogram Sample

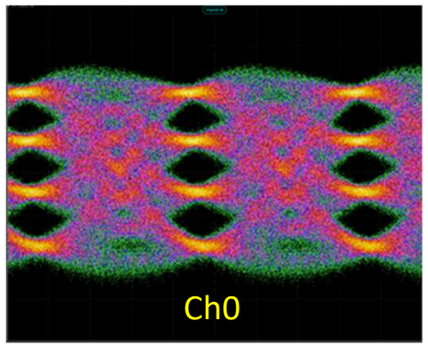
Link Group 0 (8)			Reset	Reset	Reset				BER	PRBS 31	PRBS 31
Link 0	IBERT_0.Quad_206.CH_2.TX	IBERT_0.Quad_206.CH_2.RX	Reset	Reset	Reset	106.219 Gbps	4.359E12	5.773E5	1.275E-7	PRBS 31	PRBS 31
Link 1	IBERT_0.Quad_206.CH_0.TX	IBERT_0.Quad_206.CH_0.RX	Reset	Reset	Reset	106.219 Gbps	4.301E12	5.68E4	1.283E-8	PRBS 31	PRBS 31
Link 2	IBERT_0.Quad_205.CH_2.TX	IBERT_0.Quad_205.CH_2.RX	Reset	Reset	Reset	106.242 Gbps	4.273E12	2.497E5	5.753E-8	PRBS 31	PRBS 31
Link 3	IBERT_0.Quad_205.CH_0.TX	IBERT_0.Quad_205.CH_0.RX	Reset	Reset	Reset	106.219 Gbps	4.125E12	1.272E4	3.004E-9	PRBS 31	PRBS 31
Link 4	IBERT_0.Quad_204.CH_2.TX	IBERT_0.Quad_204.CH_2.RX	Reset	Reset	Reset	106.219 Gbps	4.02E12	2.301E5	5.731E-8	PRBS 31	PRBS 31
Link 5	IBERT_0.Quad_204.CH_0.TX	IBERT_0.Quad_204.CH_0.RX	Reset	Reset	Reset	106.219 Gbps	3.922E12	2.73E4	6.847E-9	PRBS 31	PRBS 31
Link 6	IBERT_0.Quad_203.CH_2.TX	IBERT_0.Quad_203.CH_2.RX	Reset	Reset	Reset	106.219 Gbps	3.686E12	1.153E5	3.073E-8	PRBS 31	PRBS 31
Link 7	IBERT_0.Quad_203.CH_0.TX	IBERT_0.Quad_203.CH_0.RX	Reset	Reset	Reset	106.242 Gbps	3.688E12	6.131E4	1.669E-8	PRBS 31	PRBS 31

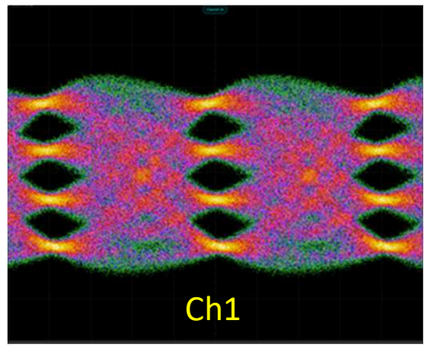
100G PAM4
8 channels BER results

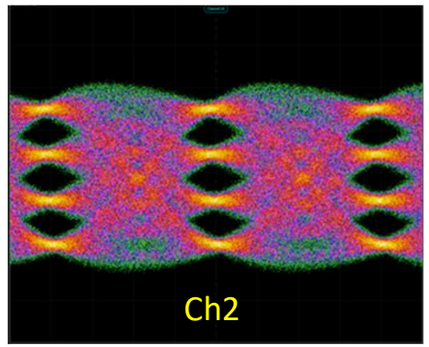
BER in the range of 3E-9 to 1E-7 (>3 decades of margin vs. IEEE spec)

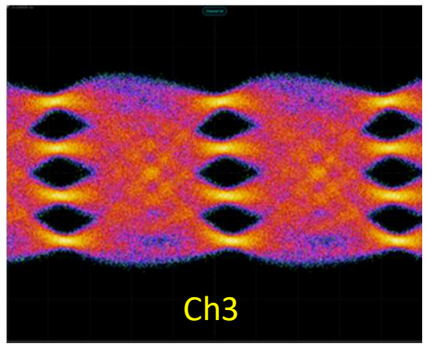
106.25Gbps PAM4 TX Quality

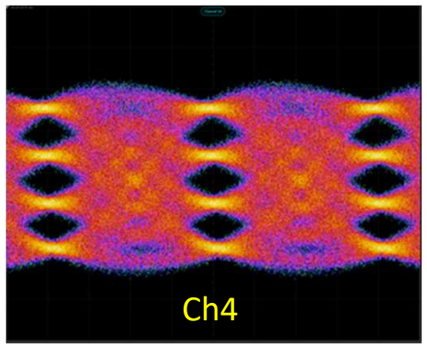
Averaged Optical Tx from ODIN™8P

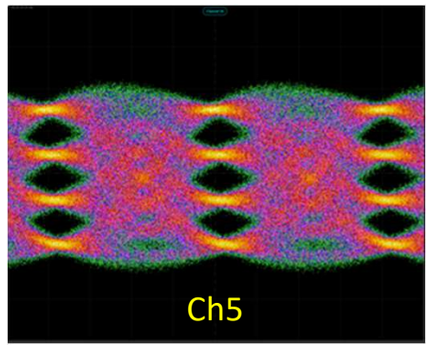


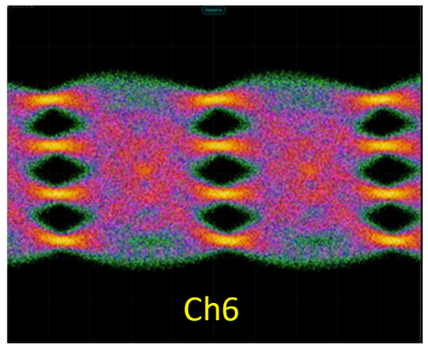


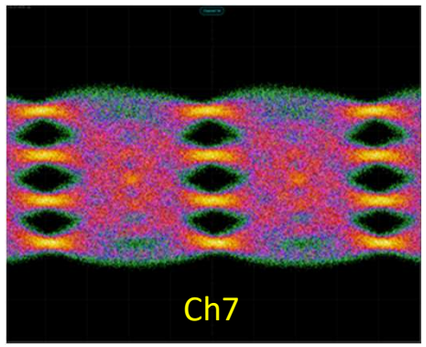








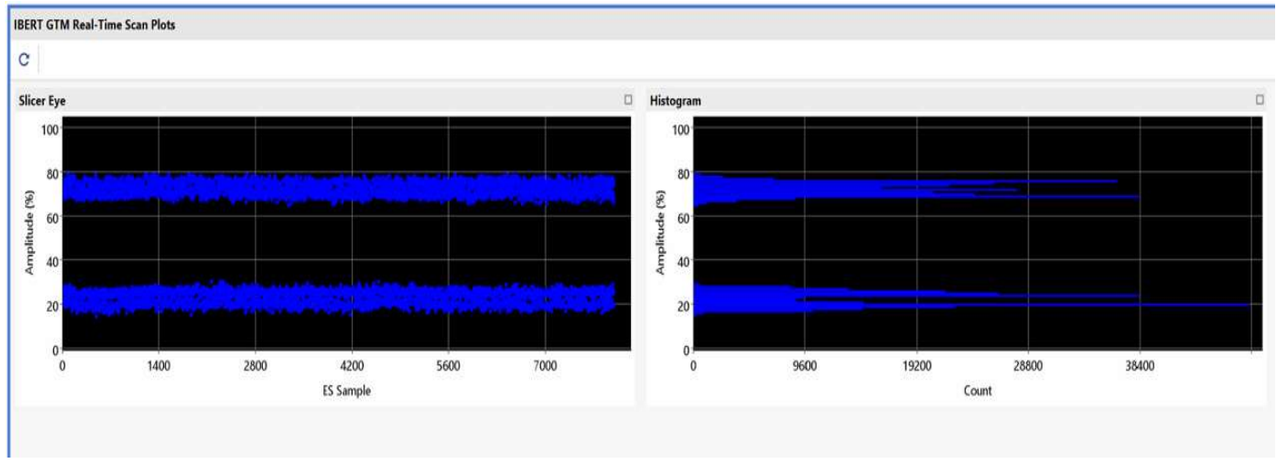




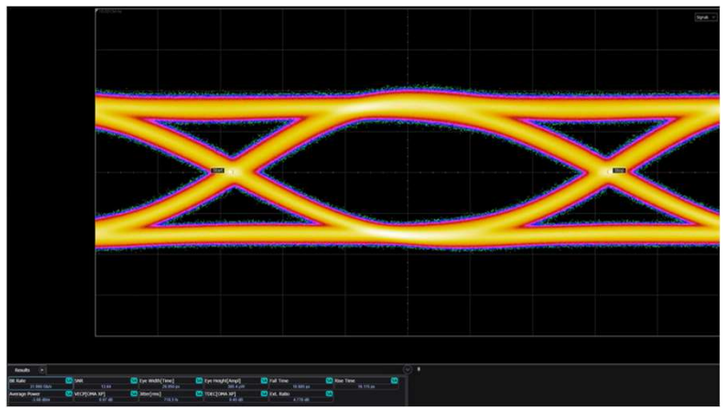
Channel		Ch0	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7
TDECQ (dB)	After IEEE 802.3bs TDECQ EQ	1.29	1.19	1.00	1.09	1.30	1.57	1.39	1.56

Optical Tx passing IEEE 802.3bs TDECQ spec (< 3.5dB) with good margin

32Gbps NRZ Fiber Loopback BER



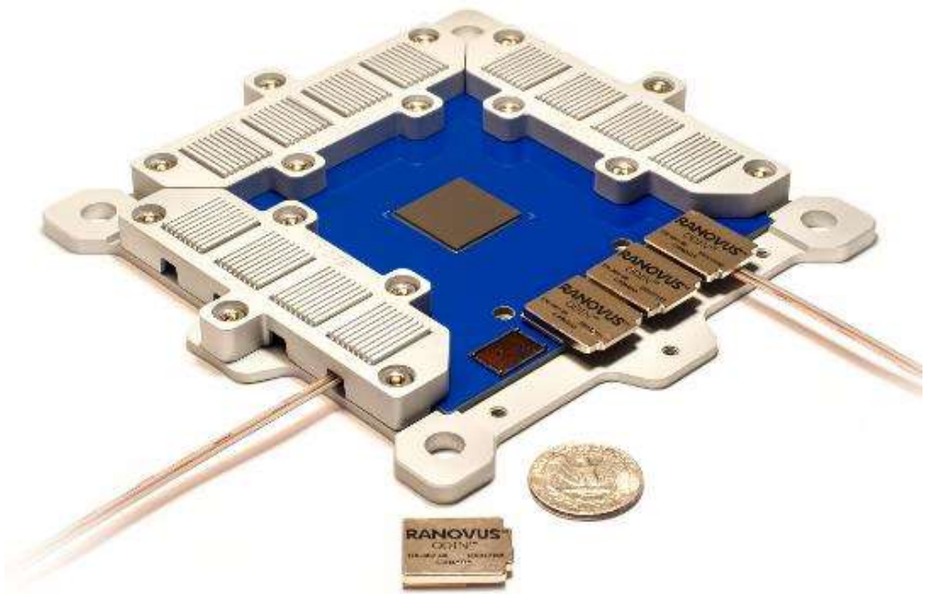
32G NRZ – Slicer Eye & Histogram Sample



32G NRZ
Eye Diagram Sample
@Rx Output

ODIN™ is protocol & data rate agnostic – ready to support PCIe Gen5 application

Thank You!



RANOVUS Odin™

Multi Terabit platform for optical interconnect