HOLISTIC TRANSFORMATION IN HIGH VOLUME MANUFACTURING OF DATA CENTER TRANSCEIVERS

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Acknowledgement

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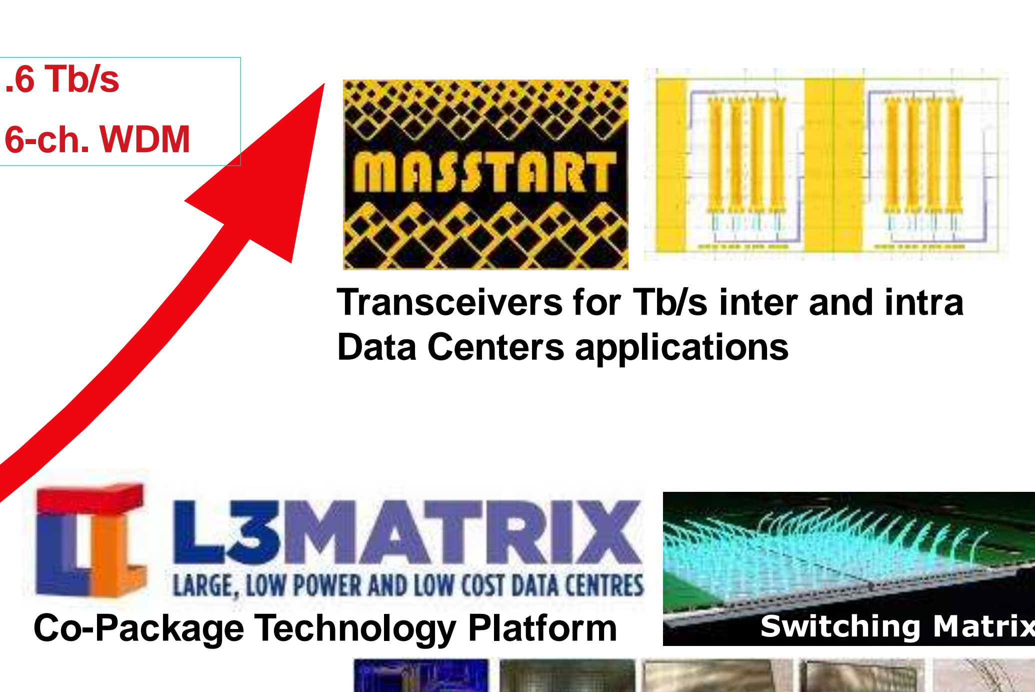
*MASSTART project is an initiative of the **Photonics Public Private Partnership**. www.photonics21.org*

Empowering Photonic Interconnects for Data Center and Next Generation Computing

Fraunhofer IZM:

- System concept and design
- Photonic and RF component design
- Signal integrity and board design
- Silicon photonics interposer
- Through silicon via (TSV)
- 3D integration
- Flip chip assembly
- Co-packaging
- System evaluation
- Benchmarking



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Empowering Photonic Interconnects for Data Center, Next Generation Computing, Next Generation Networks

1 **PROMETHEUS**

Programmable photonics enabling ultra-fast spiking and quantum neural networks

2 **OCTAPUS**

Optical circuit switched time sensitive network architecture for high-speed passive optical networks and next generation ultra-dynamic and reconfigurable central office environments

3 **ADOPTION**

Advance co-packaged optics enabling high-efficiency cloud computing

4 **ALLEGRO**

Agile ultra low energy secure networks

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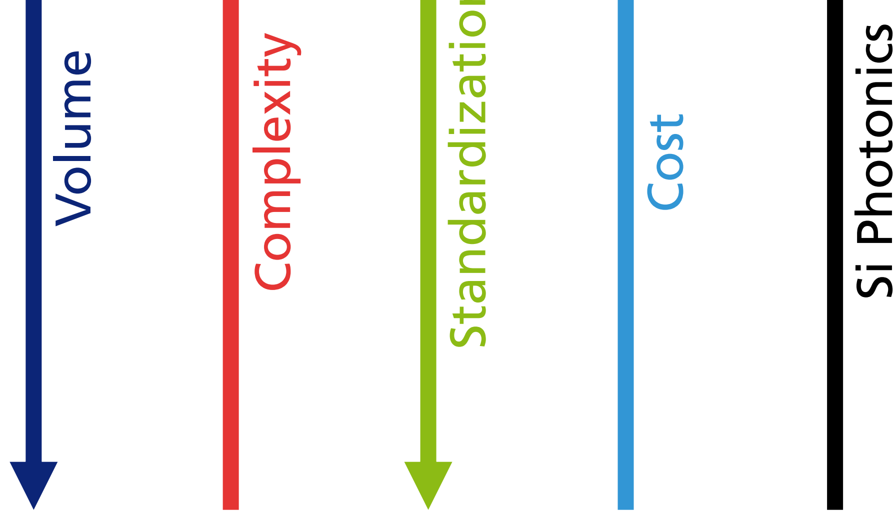
Data Center Architecture Metrics



Tier 0 switches service a rack

Tier 1 switches service a „row“ (of racks)

Tier 2 switches service a „Co-location“

Tier 3 switches service a data-center

- Interface to long-haul network
- Also interface to metro network

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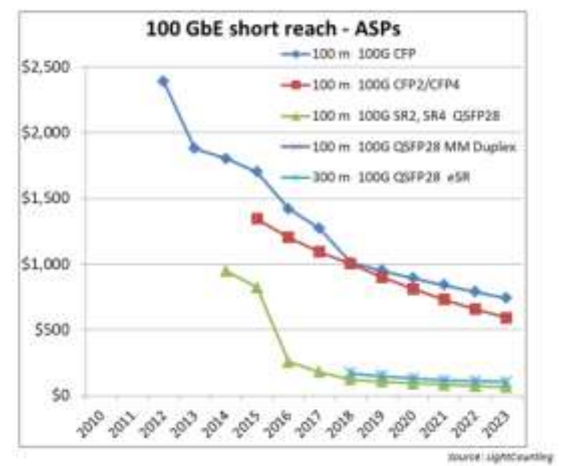
Data Center Transceiver Metrics

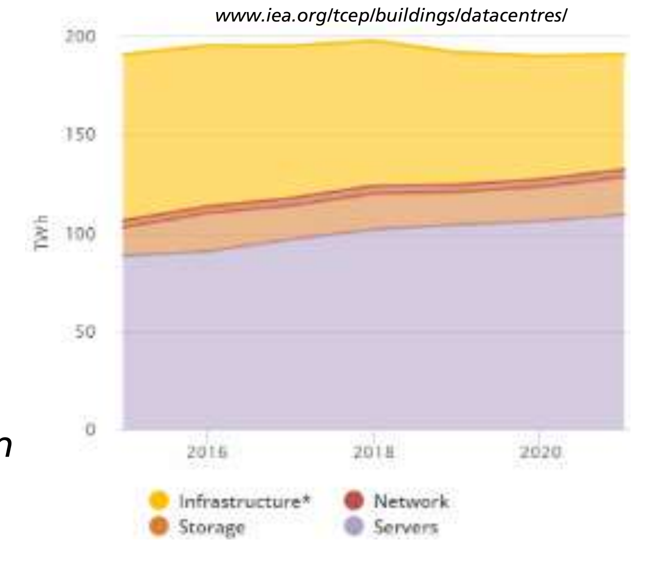
Lower Cost

Sub $1/G is an industry-wide goal



Lower Power

Optical interconnects power consumption amounts to ~2% of the total DC power; however, within a rack they are critical.



Higher Reliability

Transceiver failures in the DC requires constant maintenance

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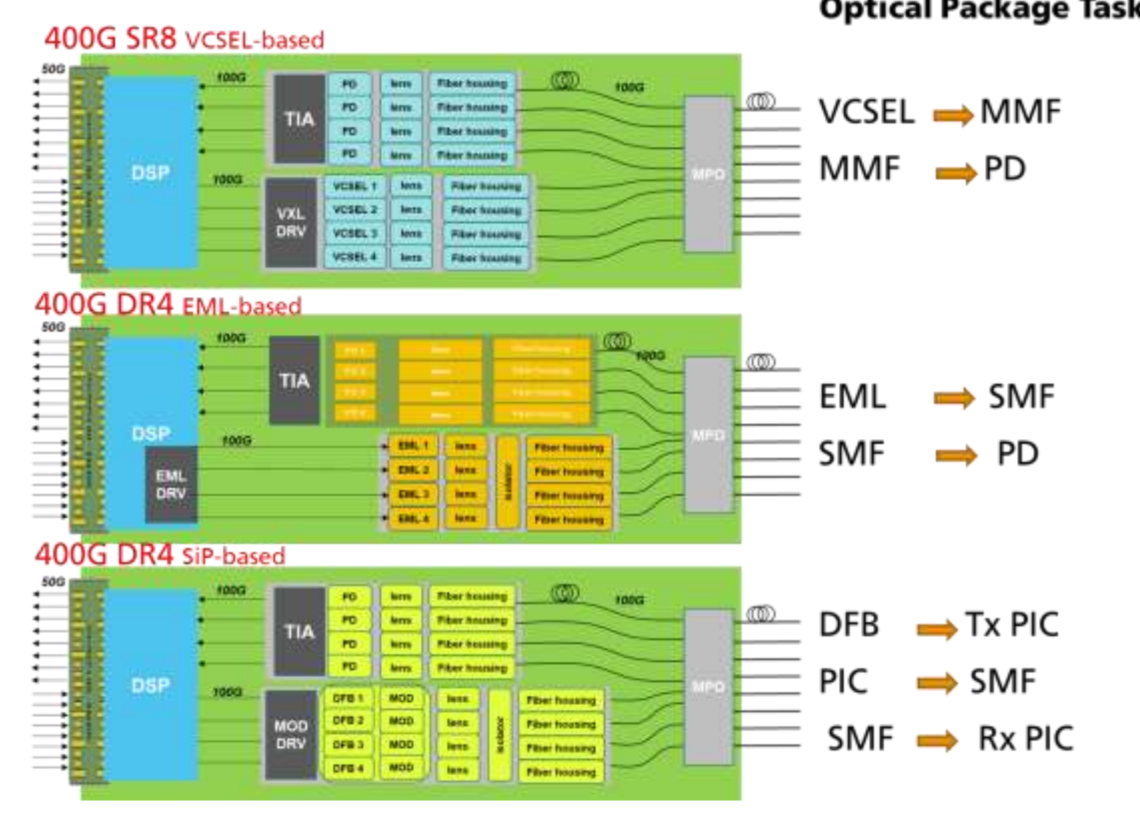
Cost, Power and Reliability Optimization Requirements

- Design for high volume manufacturing: passive or fully-automated
- Design for reduced BOM
- Eliminate labor-intensive alignment steps (COGS)
- Support extended reach, high temperature with single design
- Support all data rates with a single optical design

Innovation in Optical Packaging



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MASSTART

teem
PHOTONICS

- System providers
- Photonic Assembly & Testing
- Design House & Technology consultancy
- Technology providers

www.masstart.eu

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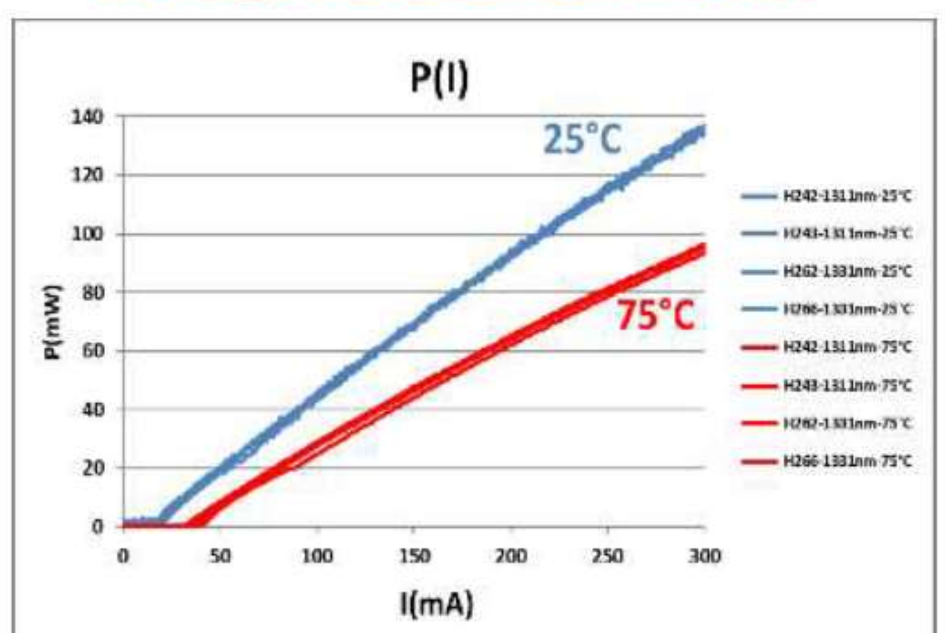
High-Power DFB Lasers based on Al-free MQW

- Uncooled DFB with low Ith and high Pout
- Compatible with SiBH technology

New generation of HPDFB



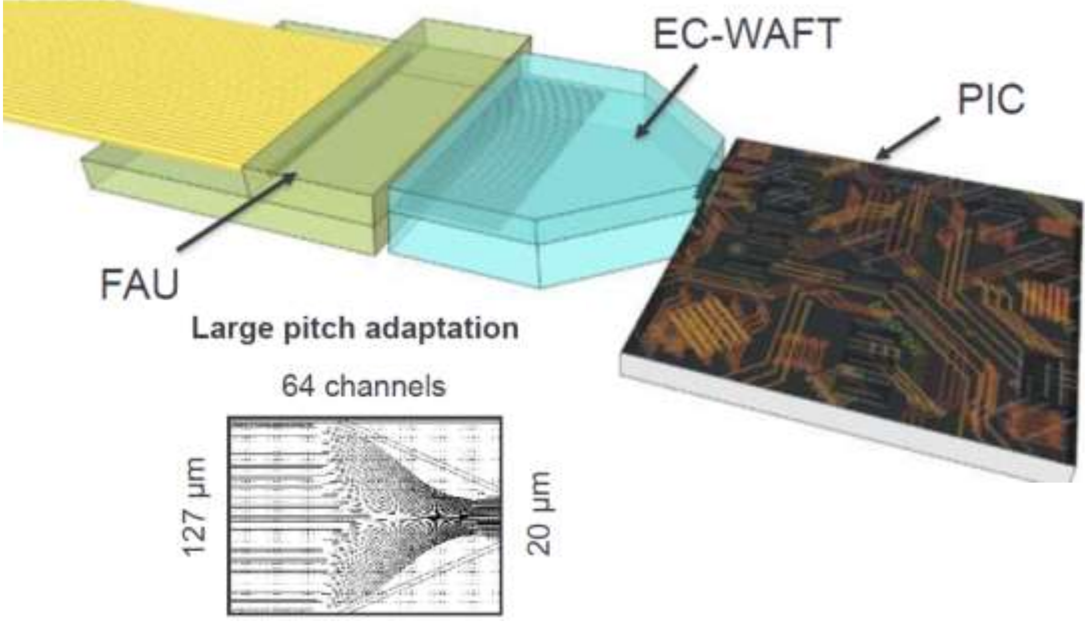
The output power is improved by 25% at high temperature operation

WAFT : Pitch and Mode Adaptation

teem PHOTONICS

- Insertion loss (incl. fiber) <0.7dB
- MFD 4x3µm (1/e2), pitch >20µm
- SM and PM compatible

MFD matching to PIC edge couplers



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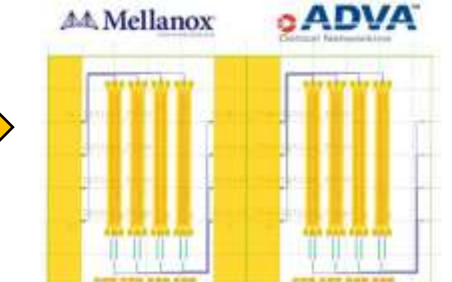
BRIGHT Integrated PHOTONICS

ARISTOTLE UNIVERSITY OF THESSALONIKI

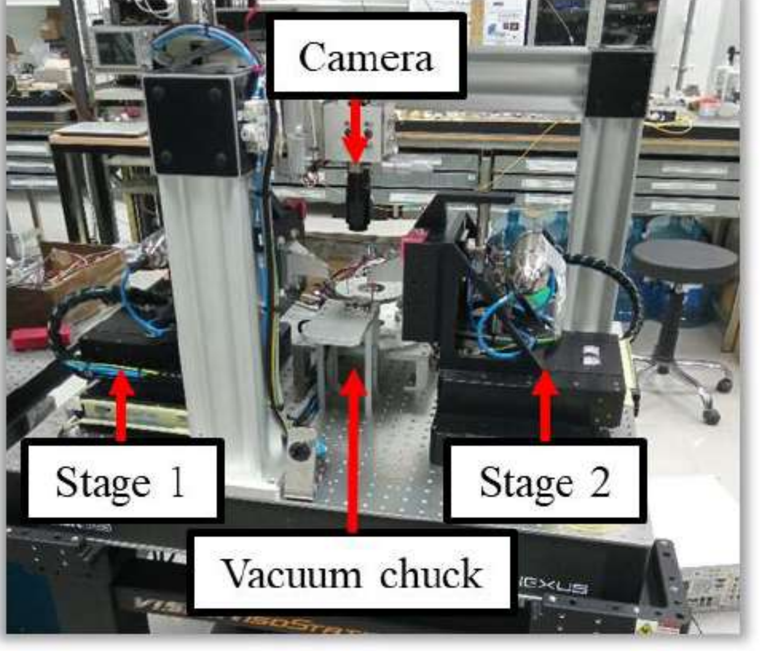
Inter- and Intra- Data Center Design Challenges up to 1.6 Tb/s

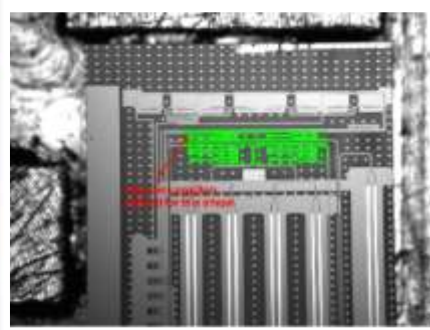
- Multiple technologies: Si-Photonics, III-V, Glass
- PDK for separate technology mapped layers
- Multiple IP Building Blocks
- Complex routing and design rules
- New generation of assembly, coupling and packaging approach
- Create packaging rules, packaging templates, import fiducial markers

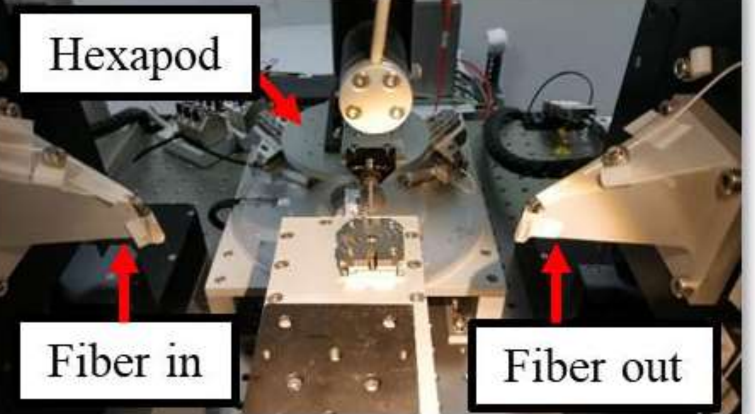
```
# import PDK
# import IP BBs
# import Fiducials

import nazca
import leti
import teem
import izm
import apt
import bright
import ficontec
import dust
```



Automated Die Tester Platform







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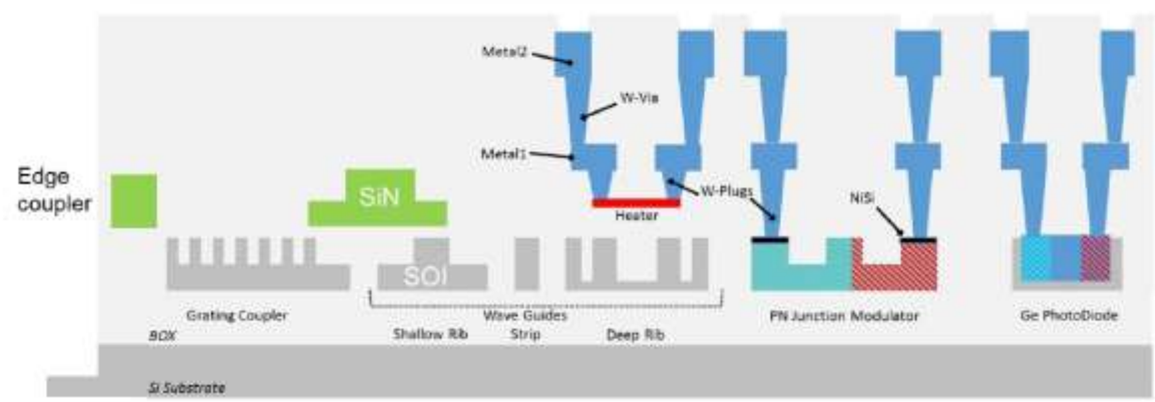
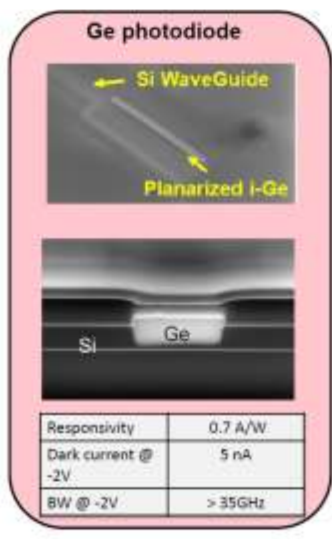
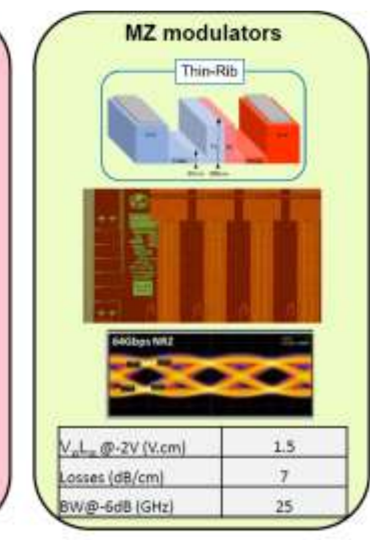
Silicon Photonics Technology KPIs and Device Libraries





Responsivity	0.7 A/W
Dark current @ -2V	5 nA
BW @ -2V	> 35GHz



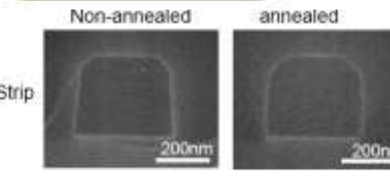
$V_\pi L_\pi$ @-2V (V.cm)	1.5
Losses (dB/cm)	7
BW@-6dB (GHz)	25

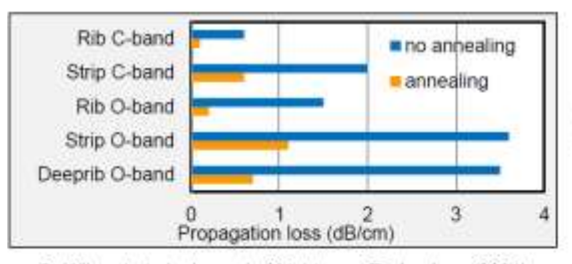
- **Advanced 300mm Si platform**
- Substrates : SOI 310nm and 220nm
- Si patterning with immersion lithography
- 60nm smallest feature size
- > 200 steps ; 24 litho levels
- 40 metro/control steps
- Low optical losses: 0.6-2 dB/cm
- **Versatility**: combine building blocks

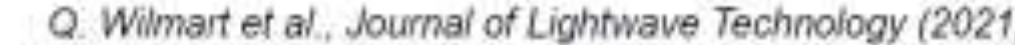
Low-loss Si waveguides:

- Roughness reduction with smoothing annealing (H2 850°C)
- Record low propagation losses in Si <1dB/cm
- No shape modification: no impact on other devices
- No impact on modulator efficiency

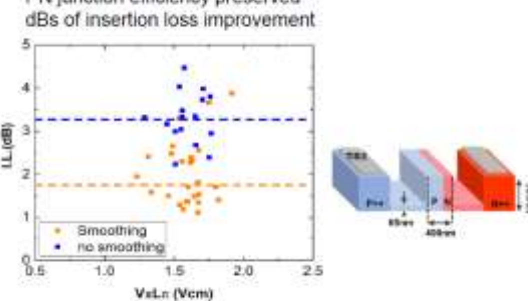
Strip WG @1310nm	1.1dB/cm
Strip WG @1550nm	0.7dB/cm






Q. Wilmart et al., Journal of Lightwave Technology (2021)

PN junction efficiency preserved
dBs of insertion loss improvement



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Front and Back Side Processes for TSV, RDL and IO formation

1. Original wafer condition o Original IO pads opened o keep out zones in FEOL and BEOL (red circle)	
2. TSV process (Litho mask required-->layer 10 in current TRX8 layout) o original IOs pads are covered with passivation layer after TSV process	
3. Passivation opening over original IO pads (Litho mask required-->layer 8 in current TRX8 layout)	
4. Front side RDL formation (1µm Al) (Litho mask required-->layer 11 in current TRX8 layout) **5. RDL passivation (1µm CVD Oxide / Nitride)** (Litho mask required-->not foreseen in TRX8 layout)	
6. Front side pad metallization (Litho mask required-->not foreseen in TRX8 layout) o original IOs can be covered with pad metallization o pad metallization to be located at all positions were passivation is opened o pad formation on top of TSVs not allowed	

7. Temporary carrier bonding	
8. Back grinding / TSV reveal **9. Back side passivation (1µm CVD Oxide / Nitride)** (Litho mask required-->layer 9 in TRX8 layout)	
10. Back side RDL (1µm Al) (Litho mask required-->layer 21 in TRX8 layout) **11. RDL passivation (1µm CVD Oxide / Nitride)** (Litho mask required-->not foreseen in TRX8 layout)	
12. Back side pad metallization deposited (Litho mask required-->not foreseen in TRX8 layout)	
13. Temporary carrier de-bonding	

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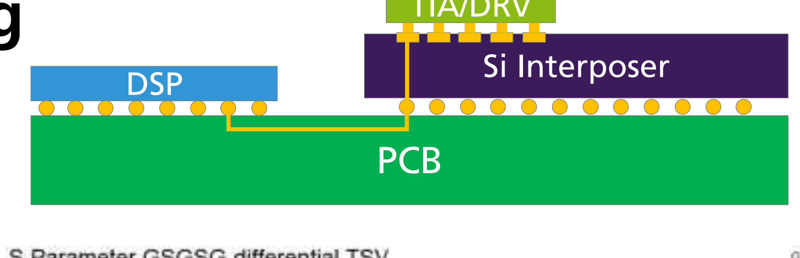
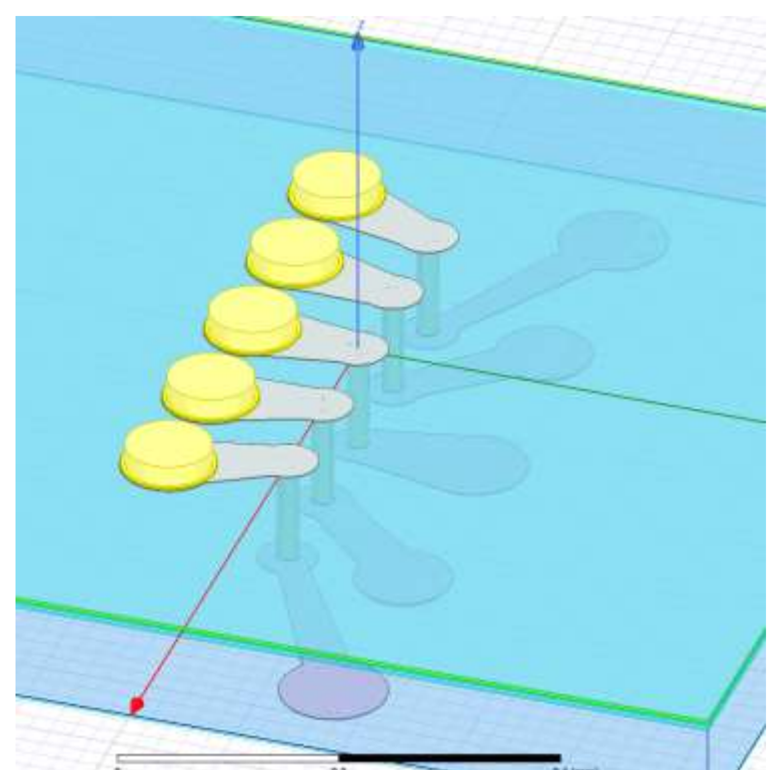
GSGSG TSV Application Scenario / Co-Packaging



Required to connect:

- Driver/TIA chips assembled on top of the Interposer
- DSP chip assembled on the PCB



S Parameter GSGSG differential TSV

Magnitude (dB): 0.00, -10.00, -20.00, -30.00, -40.00, -50.00, -60.00

Freq [GHz]: 0.00, 10.00, 20.00, 30.00, 40.00, 50.00, 60.00

Curve Info
dB(St(Diff1,Diff1)) Setup1 : Sweep wtop='40um'
dB(St(Diff2,Diff1)) Setup1 : Sweep wtop='40um'
dB(St(Diff1,Diff2)) Setup1 : Sweep wtop='40um'
dB(St(Diff2,Diff2)) Setup1 : Sweep wtop='40um'

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Module Coupling

400G

DFB

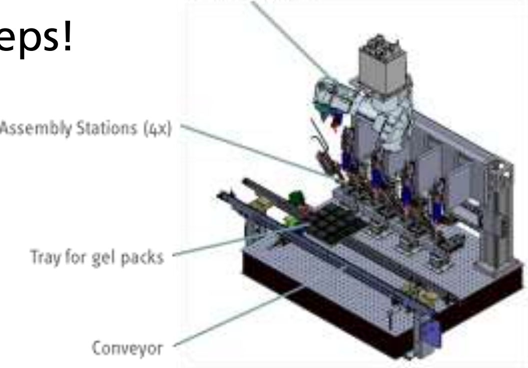
PIC

800G

Mass manufacturing line for DC interconnects (possible layout)

ficonTEC photonics assembly & testing

- Final cost defined by
- Machine costs
- Footprint / Clean room area
- Throughput of all assembly steps!



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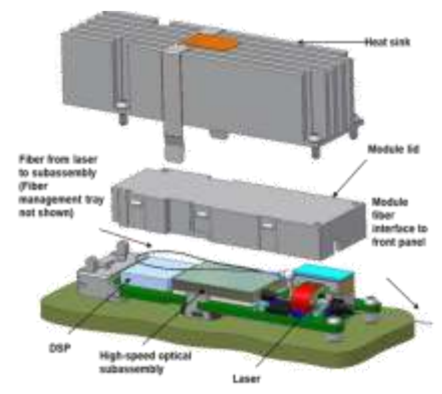
NVIDIA NETWORKING

Coherent transceiver with 600Gb/s capacity (DP-64QAM)

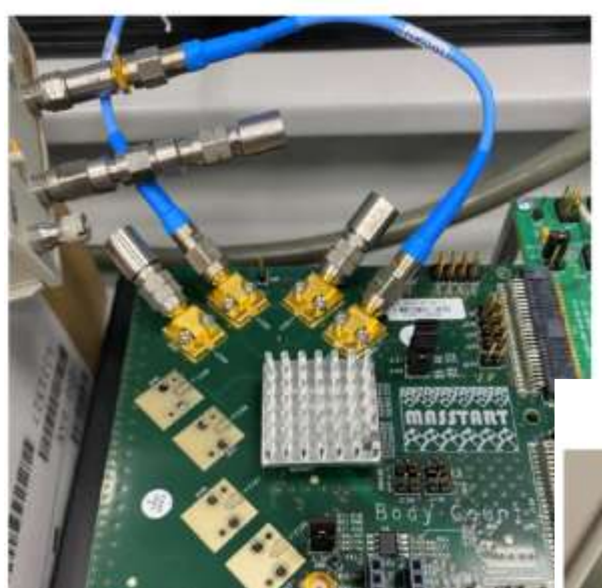
- A tunable single-wavelength
- Following the DP-64QAM modulation format on 64Gbaud/s line rate
- Engine for pluggables and line-cards
- Modulator, receiver, driver, TIA and control IC
- Solder reflow compatible
- BGA contacts for highest RF-performance
- OIF standard, 15 x 22.5 x 3.6mm footprint



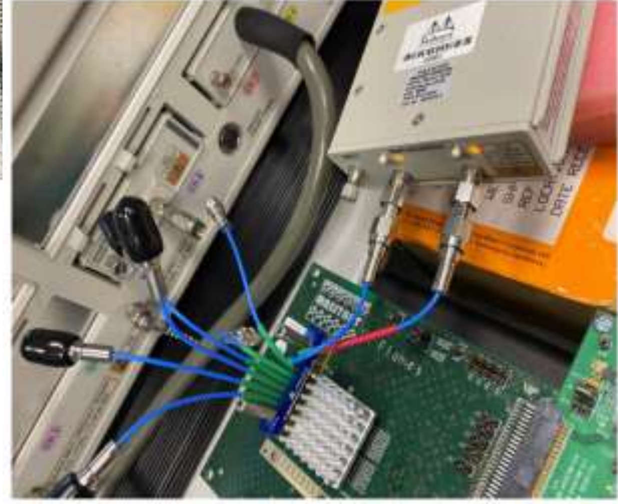
Source: ADVA

4-Channel PSM4 Module in QSFP-DD Format with 400G Aggregate Bit Rate

Rosenberger Based Prototype



Ardent Based Prototype



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How to enable mass-manufacturing of datacom photonics products?

- Automated manufacturing
- Optical transceivers transfer rates > 1Tb/s
- Competitive costs according to the interconnection distance

- Proven designs
- Chip manufacturing (photonic/electronic)
- Integration & Packaging
- Testing
- Demonstration in a real environment
- Standardization

- PIC-based optical transceivers with transfer rates above 1Tb/s enabling massive deployment in datacenter environments
(<1€/Gbps between racks and <0.1€/Gbps inside racks)

→ **Ecosystem and improved cross fertilization between photonics and other technology areas**

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8th International Symposium for Optical Interconnect in Data Centres

Wed., 21. September 2022,

ECOC 2022, Basel, Switzerland

MASSTART Project

19.-21. September 2022,

Berlin-Brandenburg Pavilion (booth #411)

ECOC Exhibition 2022, Basel, Switzerland

Applause ECSEL Project

Heterogenous Integration Summer School

29.-30. September 2022,

ESREF 2022, Berlin, Germany

We are constantly looking for new talents!

Optical - wireless networks

Photonic neural networks

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Transmit and Receive Module Coupling

400G

400G

DFB

PIC

800G

PIC

Fiber array

800G

Total Irradiance surface 4 SMF
5/25/2020
Beam wavelength is 1.31000 µm in the media with index 1.44680 at 0.0000 (deg)
Display X Width = 2.6140E-02, Y Height = 9.5957E-03 Millimeters
Peak Irradiance = 1.3288E+04 Watts/Millimeters^2, Total Power = 3.9262E-01 Watts
Fiber Efficiency: System 1.000000, Receiver 0.943865, Coupling 0.943865
Beam Width X = 4.54796E-03, Y = 3.96272E-03 Millimeters

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