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Photonic Integration and Pathfinding with Intel FPGAs

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Intel

Date: 7th September 2022

Agenda (20mins + 10min)

- Some DARPA Program Examples
- Figures of Merit
- DARPA CHIPS and the Era of Chiplets
- DARPA PIPES – Heralding Fiber from Compute Package
- DARPA Space-BACN and Coherent Free-Space-Optics for LEO Satellite Constellations
- Future Research Initiatives
- Conclusion
- Q & A

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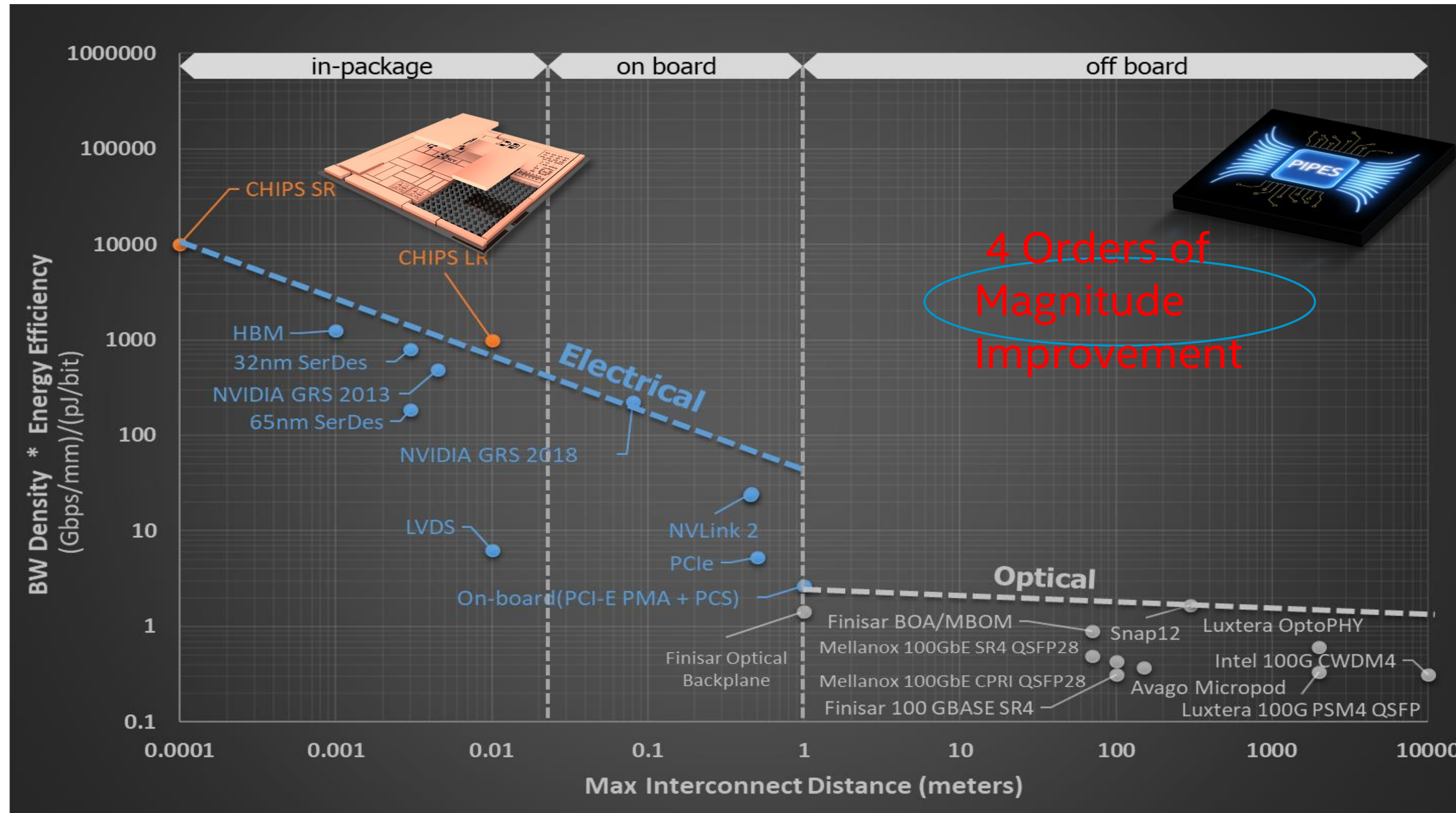
Intel’s participation on some of DARPA Photonic Integration Programs

- CHIPS - Common Heterogeneous Integration and IP Reuse Strategies
  - Standardized Interfaces for Interoperable Chiplets for ‘System in Package’
  - Integration demonstration of Highspeed Data-converters and Photonic Transceivers
  - FoM sets following metrics <<1pJ/bit and > 220Gbs/mm Shoreline
  - ‘System in Package’ Development Cost and Schedule reduced compared to Monolithic Designs
- PIPES - Photonics In the Package for Extreme Scalability
  - Aim of 100Tbs @ <1pJ/b >1km per Package (Phase 3)
  - Phase 1, 2.5pJ/b 1Tbs/mm 10Tbs/Package
- Space-BACN - Space-Based Adaptive Communications Node
  - Coherent Multi-waveform/FEC/Protocol Modem
  - 100^3 - $100K, 100W, 100Gbs
  - 3 Technical Areas, Optical Head (TA1), Optical modem (TA2) and Constellation Control (TA3)

FEC: Forward Error Correction

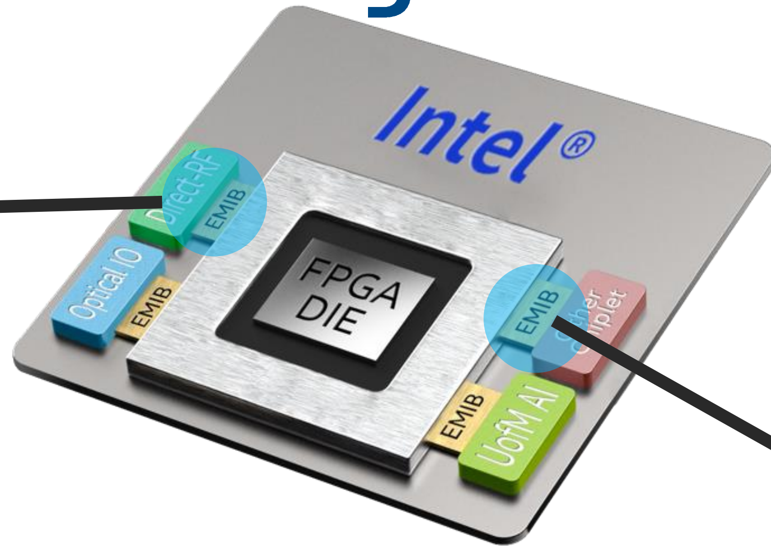
Two Interconnect Bottlenecks

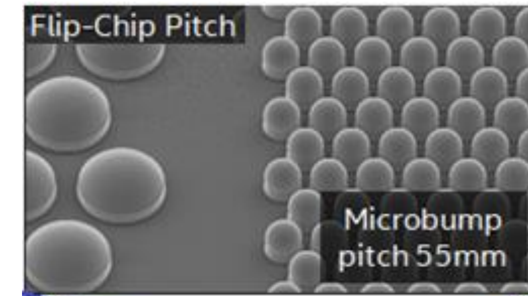


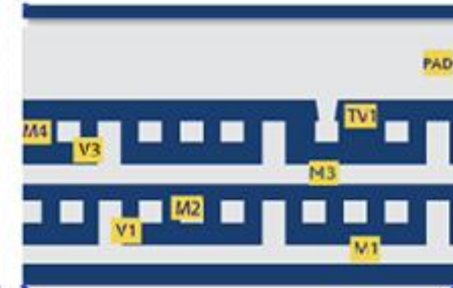
Dr. G. Keeler, ERI Summit 2019

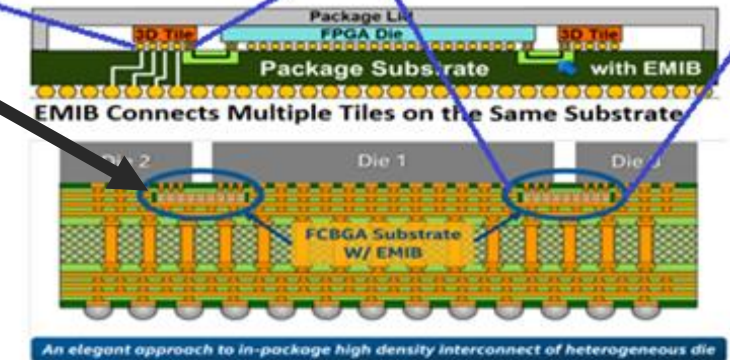
1. Solve Chiplet Integration Bottleneck (CHIPS) – intra-package
2. Solve Optical Bandwidth Power and Density through Optical Integration (PIPES)

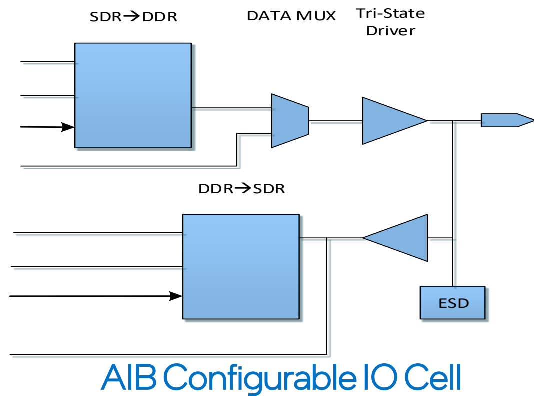
Intel EMIB for Heterogeneous Chiplet Integration











AIB Configurable IO Cell

Parallel in-package (AIB 1.0: 2Gbps/IO)
At ~3ns latency
AIB 1.0 (~1Tbps) → AIB 2.0 (~4Tbps)

AIB 1.0 EMIB (500 IOs/mm)
At 0.85pJ/bit (for 55μm μbump)

Standardization through CHIPS Alliance and UCIe
AIB 1.0 and AIB2.0 Open-Source Specifications

https://github.com/intel/aib-phy-hardware
https://github.com/chipsalliance/AIB-specification/blob/master/AIB_Specification%202_0.pdf

AIB: Advanced Interface Bus
UCIe: Universal Chiplet Interconnect Express
IO: Input/Output
DDR: Double Data-Rate
SDR Single Data-Rate

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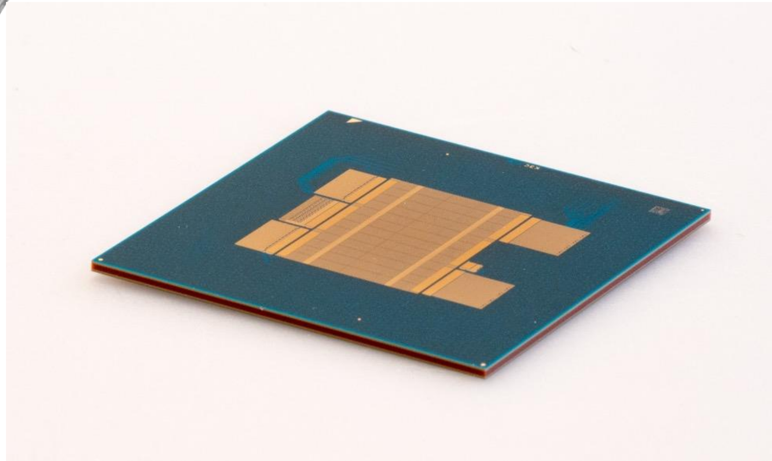
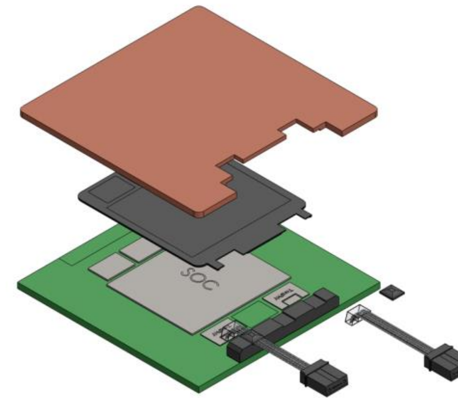
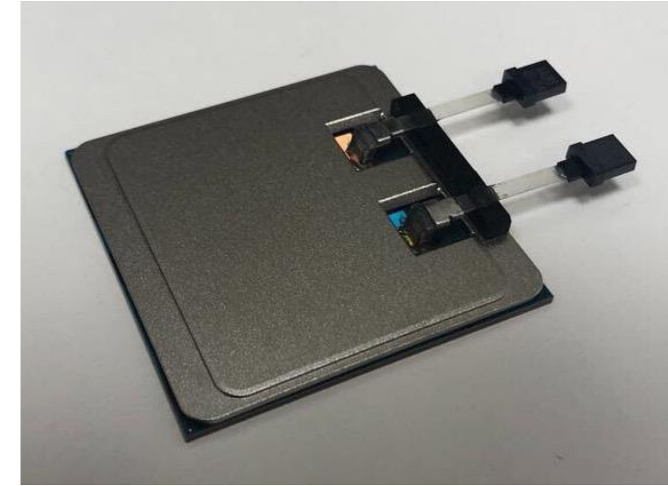
DARPA CHIPS

Gordon E. Moore
(1965)

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."







Wade et al. "TeraPHY: A Chiplet Technology for Low-Power, High-Bandwidth In-Package Optical I/O", Hotchips 2019

Mahajan, R., et al, "Embedded Multi-Die Interconnect Bridge (EMIB) – A High Density, High Bandwidth Packaging Interconnect," presentation at IEEE 66th Electronic Components and Technology Conference, May 2016.

Phase 1 Package design included Chiplets

- 2 X Quad ADC/DAC 64 GSps -Jariet Technologies (GF11)
- 2 X TeraPHY 2.56 Tbs WDM Chiplet – Ayar Labs (GF45)
- 1 X SERDES Chiplet Intel (TSMC 16)
- 1 X A.I. Accelerator Chiplet, University of Michigan (Intel 16)
- 1 x Intel Stratix 10 FPGA (Intel 14)
- 6 x EMIB (Intel)

Several other MCP developments in the program expanding the Ecosystem of interoperable Chiplets

FPGA: Field Programmable Gate Array
WDM: Wavelength Division Multiplexing
SERDES: SERializer-DESerializer
I/O: Input/Output
AI: Artificial Intelligence

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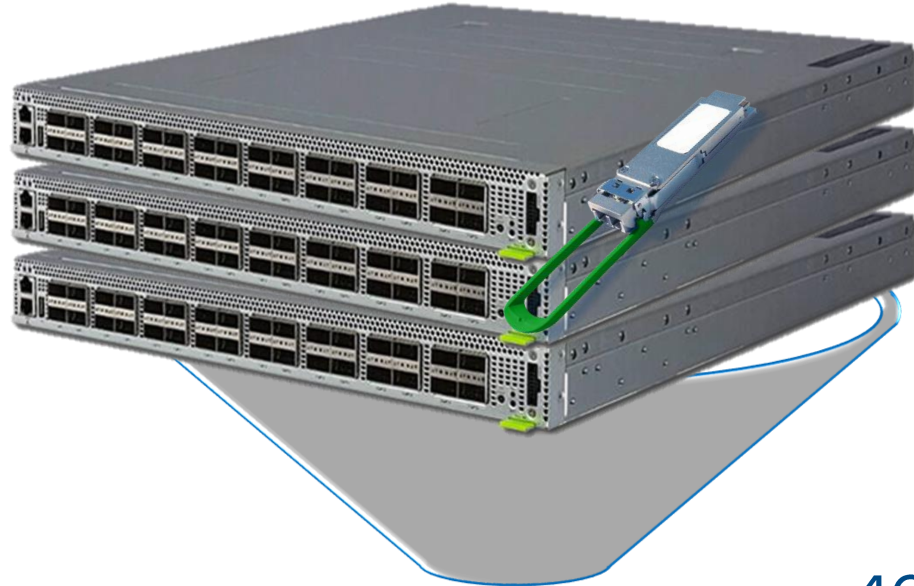
PIPES Optical Module

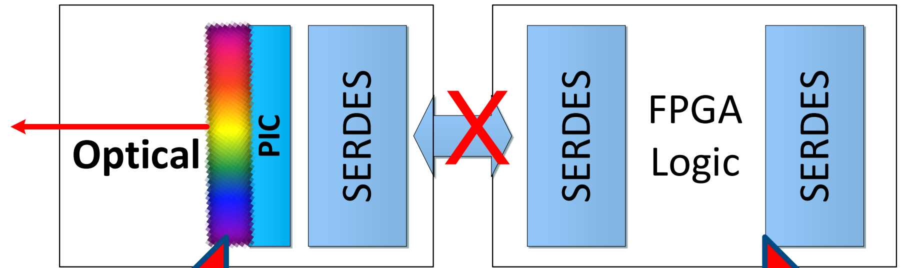


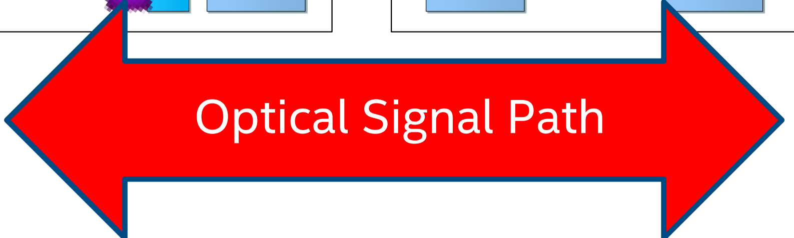
10Tbps Optical BW:

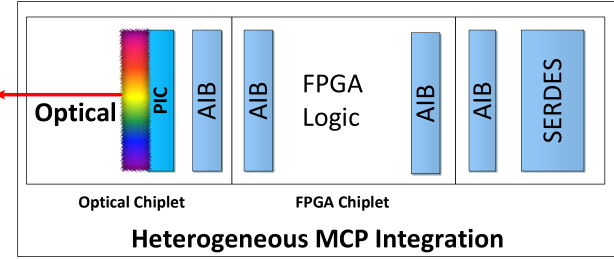
32x100G ports per card

3 RUs in 19” rack

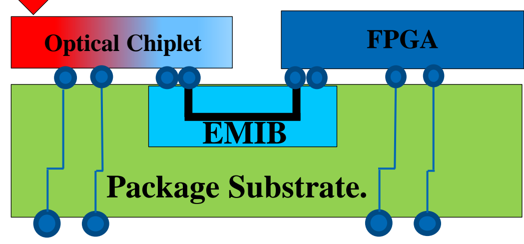
40x250G ports in 2” MCP

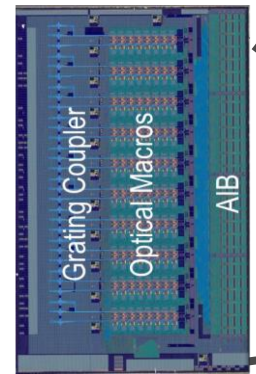


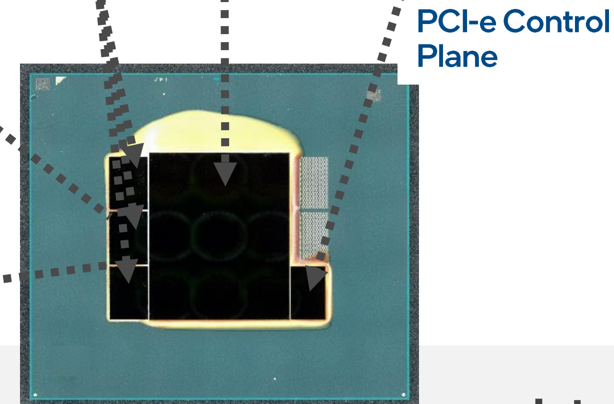




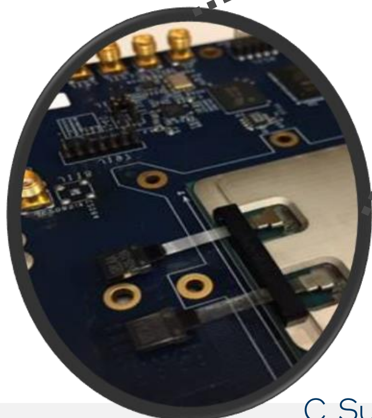
Optical Coupling







PCI-e Control Plane



C. Sun *et al.*, "TeraPHY: An O-Band WDM Electro-Optic Platform for Low Power, Terabit/s Optical I/O," *2020 IEEE Symposium on VLSI Technology*, 2020

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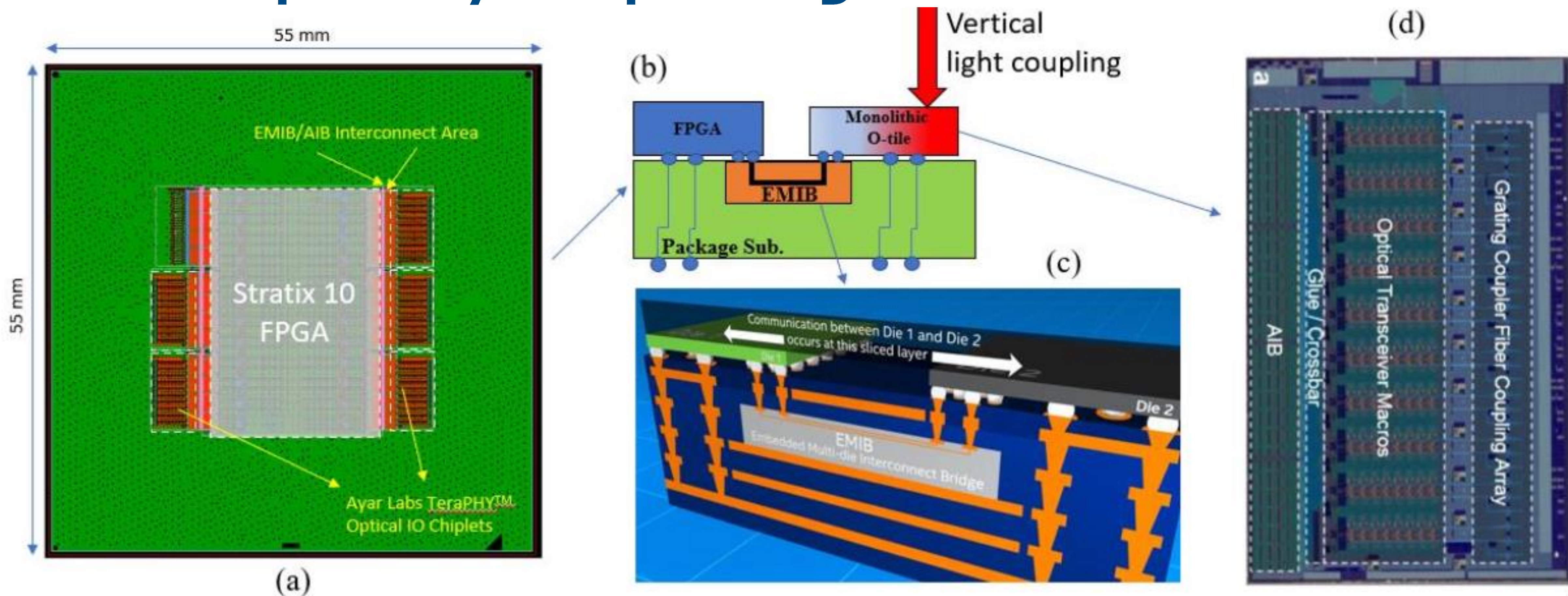
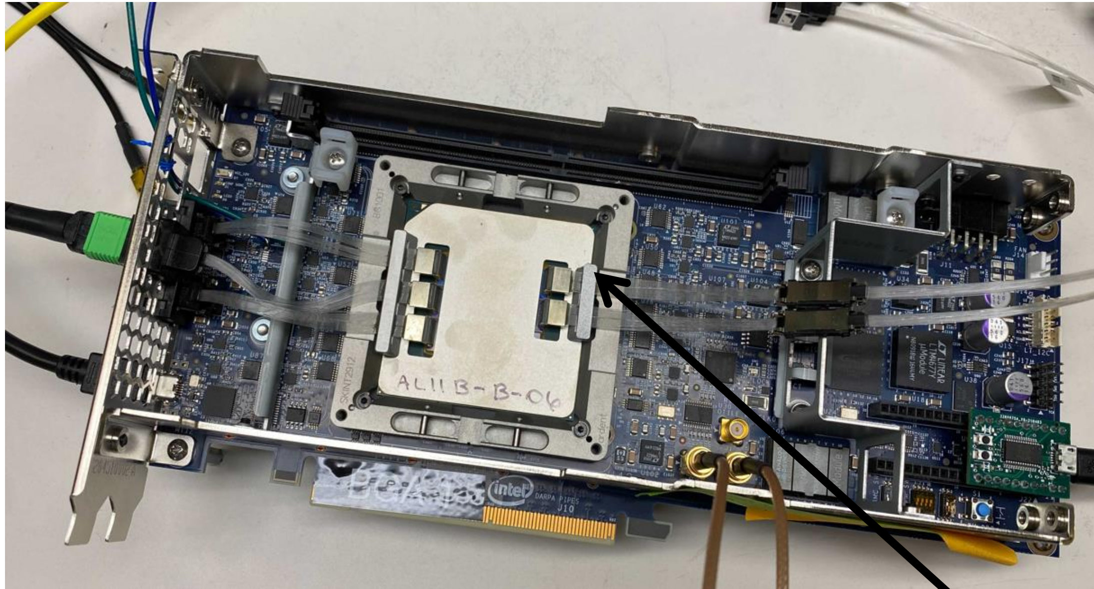
8Tbs Optically Co-packaged FPGA



K. Hosseini, E. Kok, S. Y. Shumarayev, C. Chiu, A. Sarkar, A. Toda, Y. Ke, A. Chan, D. Jeong, M. Zhang, S. Raman, T. Tran, K. A. Singh, P. Bhargava, C. Zhang, H. Lu, R. Mahajan, X. Li, N. Deshpande, C. O'Keeffe, U. Krishnamoorthy, C. Sun, R. Meade, V. Stojanovic, and M. Wade, "8 Tbps Co-Packaged FPGA and Silicon Photonics Optical IO," in Optical Fiber Communication Conference (OFC) 2021,

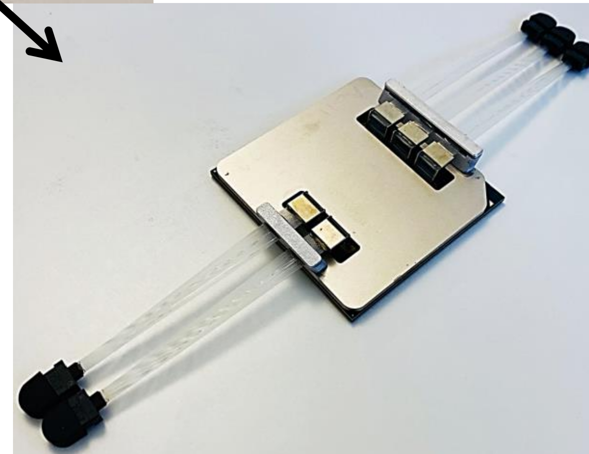
MCP on Datacenter Type Platform



Intel® FPGA Optical Programmable Accelerator Card (O-PAC) Prototype

- PCI-E Form Factor

K. Hosseini *et al.*, "5.12 Tbps Co-Packaged FPGA and Silicon Photonics Interconnect I/O," *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, 2022, pp. 260-261



MCP: Multi-Chip Package

PCI-E: Peripheral Component Interconnect Express

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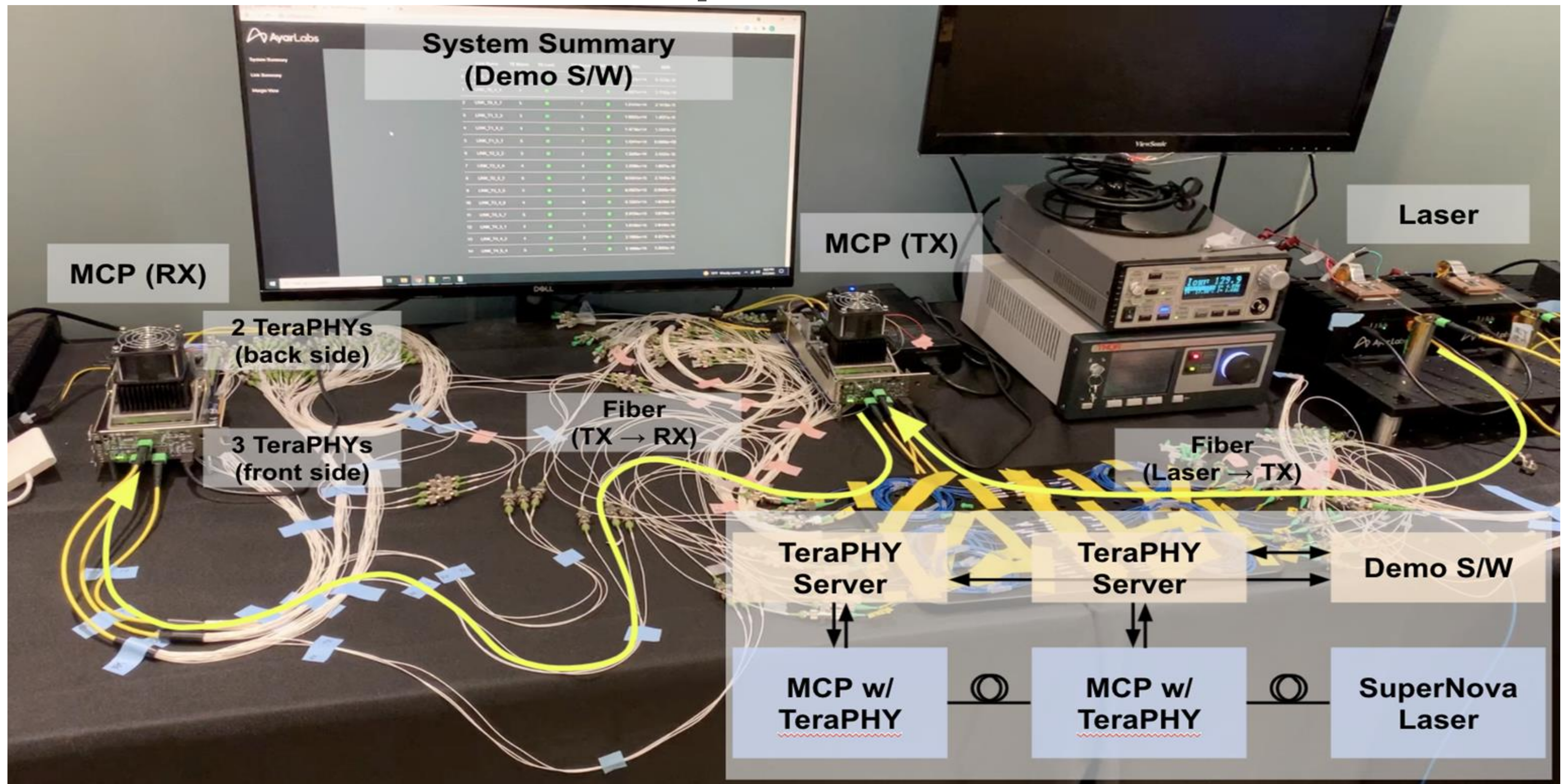
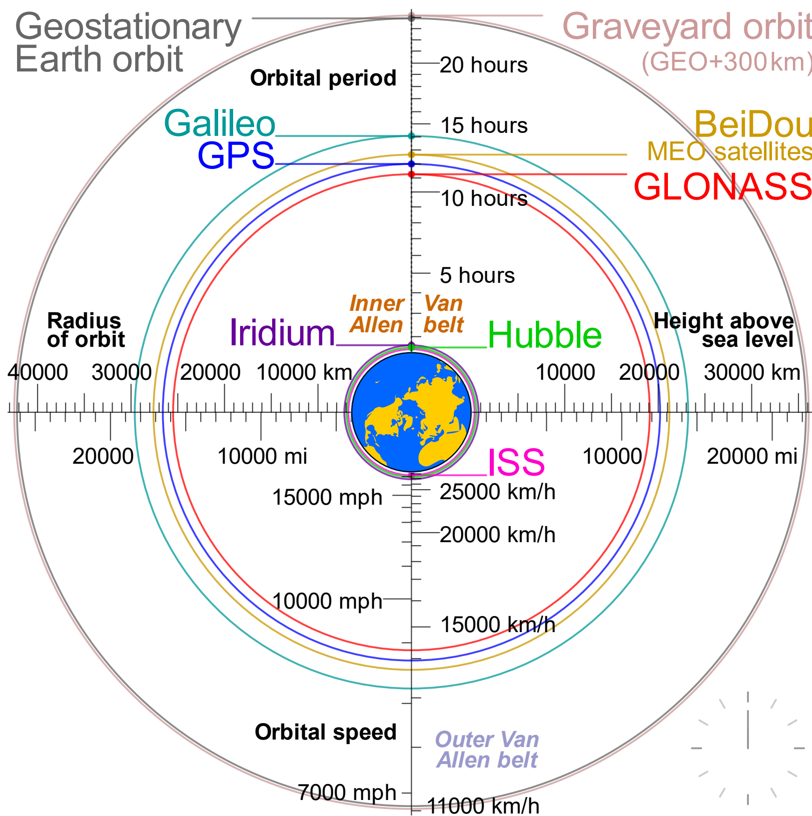
Measurement Set-Up



LEO Satellite Constellation Compatibility



https://en.wikipedia.org/wiki/Low_Earth_orbit

- LEO is between 600 km and 2000 km
- Current Operational Satellites: 5465 of which ~4700 are LEO*
- Worldwide Launches between 2022 and 2030 is >40,000
- OISL Mesh Network Proliferation
  - Limited Inter Constellation Compatibility on Protocols, Waveforms, Data rates, Channel Coding

Example LEO constellations

* https://www.ucsusa.org/resources/satellite-database

LEO: Low Earth Orbit
GPS: Global Positioning System
OISL: Optical Intersatellite Links
ISS: International Space Station

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Space-BACN High Level Objectives*

- Reconfigurable, multi-protocol intersatellite optical communications terminal – a “Swiss Army Knife” optical terminal
- Low SWaP-C
- Easy to integrate
- Connect heterogeneous constellations
- 100^3 goals:
  - 100 Gbps
  - 100 W
  - $100 k

*https://www.darpa.mil/work-with-us/space-based-adaptive-communications-node

Image: https://niklas-nienass.eu/megakonstellation

SWaP-C: Size, Weight and Power- Cost

How will it be done?

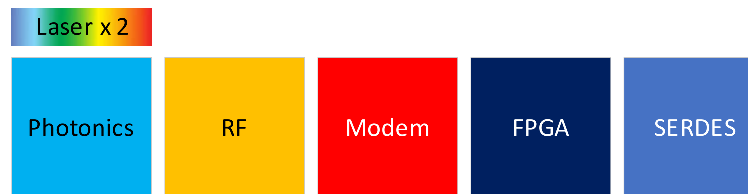
3 Technical Areas

TA1 Low-cost Coherent Aperture

- Telescope and Gimbal
- Fiber connection to TA2
- EDFA
- Beacon Tracking

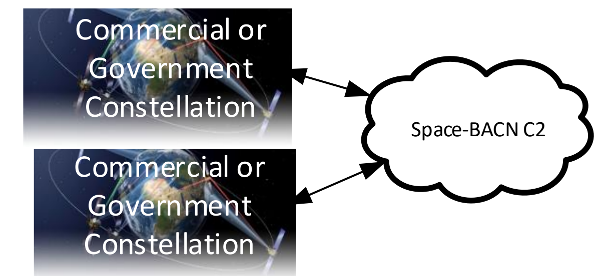
TA2 Reconfigurable Optical Modem

- Multi-waveform Support
- Multi-FEC Support
- Multi-protocol Support
- Up to 100Gbs



TA3 Cross-Constellation C2

- C2 to manage interaction between Commercial and Government Constellations
- QoS Simulations



Modular Interoperability between different Technical Areas

C2: Command and Control
FEC: Forward Error Correction
EDFA: Erbium-Doped Fiber Amplifier
QoS: Quality of Service

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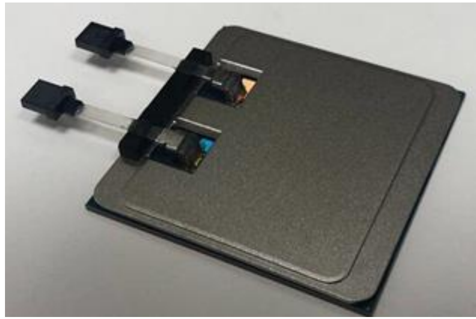
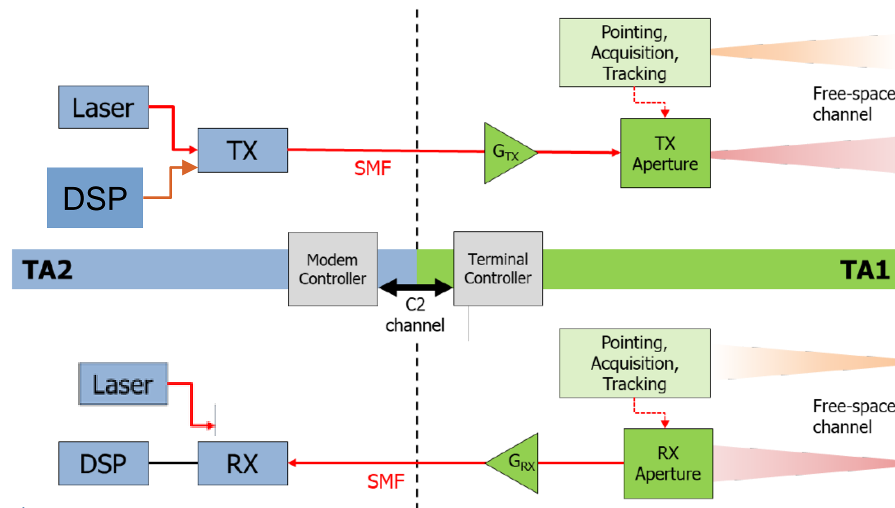
System Requirements

Program Level Goal Optical Terminal	Reconfigurable Modem Technical Area 2 (TA2)	Optical Aperture Technical Area 1 (TA1)
Link ranges	100 Gbps at 2,500 km, 25 Gbps at 5,000 km, 1 Gbps at 45,000 km	
Wavelength range	Fully tunable/selectable C band laser 1530-1565 nm	
Programmable waveforms	Reconfigurable modulation supporting various single wavelength OOK, PPM, DPSK, DP-QPSK formats	Optical aperture, optical amplifier gain, and noise performance supporting the link range and data rates
Power =< 100 W	=< 40W	=< 60W
Weight <= 10 kg	=< 2 kg	=< 8 kg
Cost in production =< $100k	=< $30k	=< $70k
5-Year lifetime in LEO	Radiation tolerant and cyber-hardened	Cross-plane support, radiation tolerant, and cyber-hardened
Modularity/Interoperability	SMF & C2 channel	
Pointing, Acquisition and Tracking (PAT)		"Beaconless," in-band-beacon, out of-band beacon *
Support major industry standards and communication protocols	Reconfigurable encoding, FEC, framing, open standards	





Space-BACN Program Solicitation
https://sam.gov/opp/e704657b448649a4a5ff7debeb39540a/view

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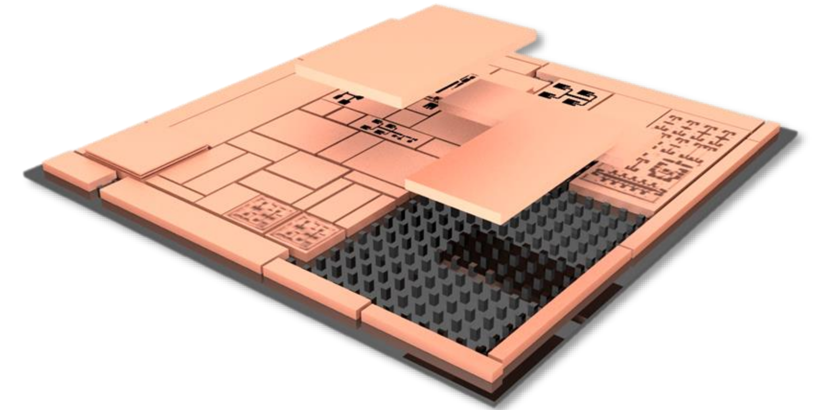
Leveraging DARPA PIPES and CHIPS for Space-BACN



- Chiplet integration of Photonics, high speed Data-converter/RF technology, DSP and FPGAs
- Phase 1 kicked off July 2022 following a Phase 0 Architecture Phase

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Further Research Topics

- Packaging Challenges
  - Allowing Compatibility with standard electronic Production Methods – Reflow , Pick and Place etc.
  - At scale low defect Fiber attach Methods,
  - Optical Chip Testing - at Probe and Final Test
- Efficient FECs
- Distributed Compute systems leveraging high Bandwidth Low-Latency Interconnect
- Communication Networks with high bandwidth processing Nodes

Conclusions

- Chiplets allow for optical co-packaging with High Performance Compute
- High Bandwidth low power Standardized Interconnect enables scaling of Platforms leveraging optical Chiplets as a reusable IP
- More Photonic Integration across Datacenter, Communications, RADAR
- Coherent Free-Space Optics for OISL

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