

07 September 2022

# Productizing a PIC: from Design IP to Scalable Testing



**VLC**  
**PHOTONICS**  
A Hitachi Group Company

# About us

- ❑ VLC Photonics offers Photonic Integrated Circuit (PIC) development services, focused on design and testing.
- ❑ Company founded in 2011.
- ❑ Offices and clean-room labs in Valencia Technological Campus (Spain).
- ❑ 21 members of extensive academic and industrial experience, and keep growing.
- ❑ 13+ years in the field of integrated optics and Photonics.
- ❑ Part of Hitachi High-Tech group since 2020.



## Hitachi High-Tech Corporation

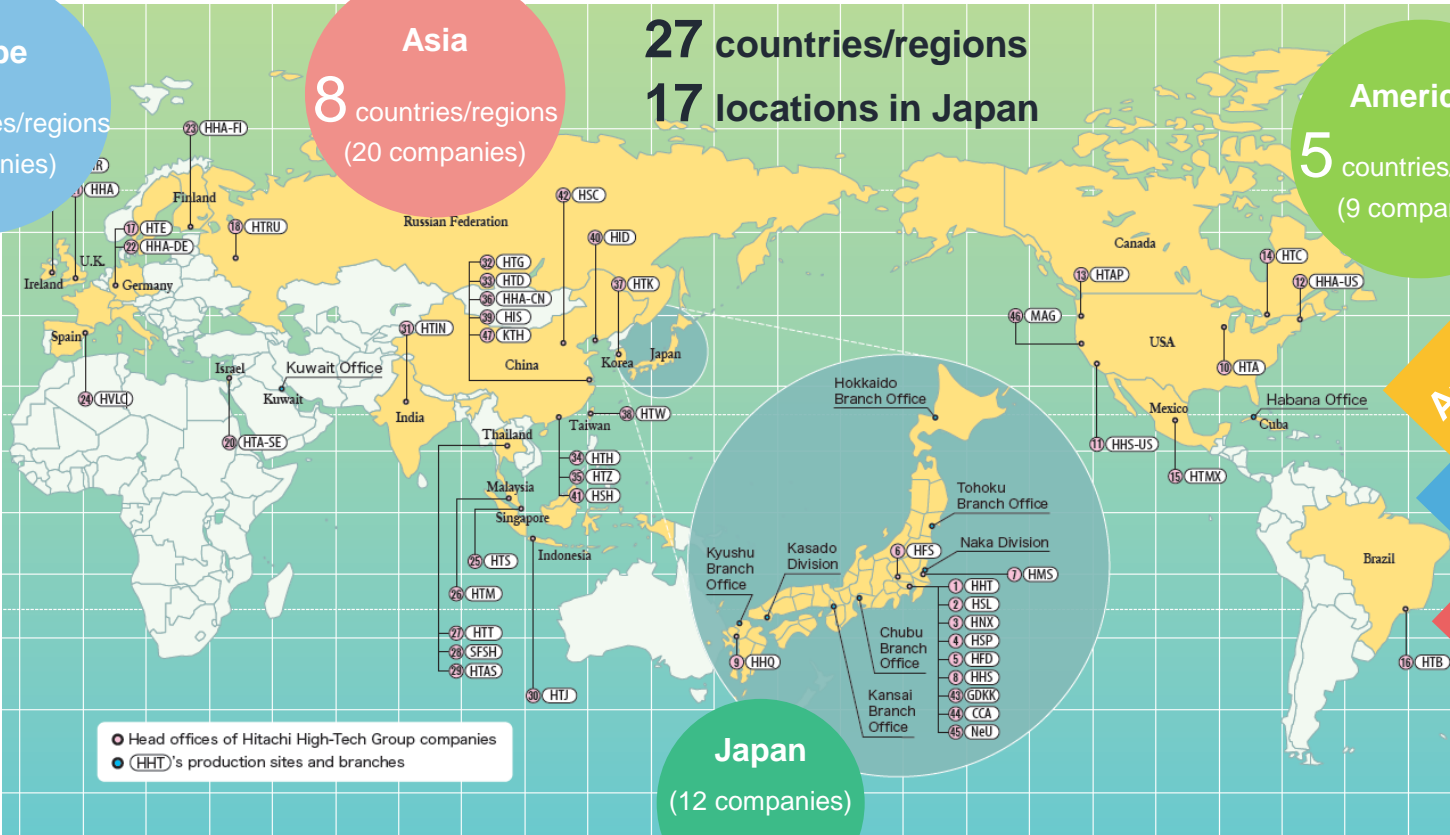
**Europe**  
11 countries/regions  
(7 companies)

**Asia**  
8 countries/regions  
(20 companies)

**27 countries/regions**  
**17 locations in Japan**

**Americas**  
5 countries/regions  
(9 companies)

Analytical & Medical Solutions  
Nano-Technology Solutions  
Industrial Solutions



● Head offices of Hitachi High-Tech Group companies  
● (HHT)'s production sites and branches

**Japan**  
(12 companies)

PIC provider  
Industrial Solutions  
complementing the  
solutions and  
services of HHT



# HHT optical components supply

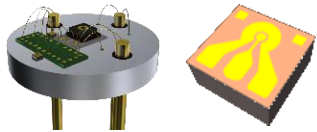
Optical Lens



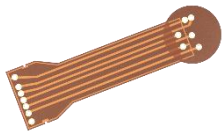
Thermistor



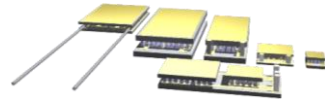
Photo Diode



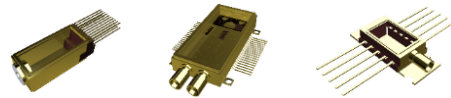
Flexible Print Circuit



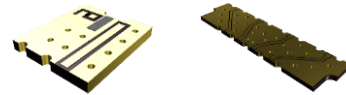
Thermo Electric Cooler



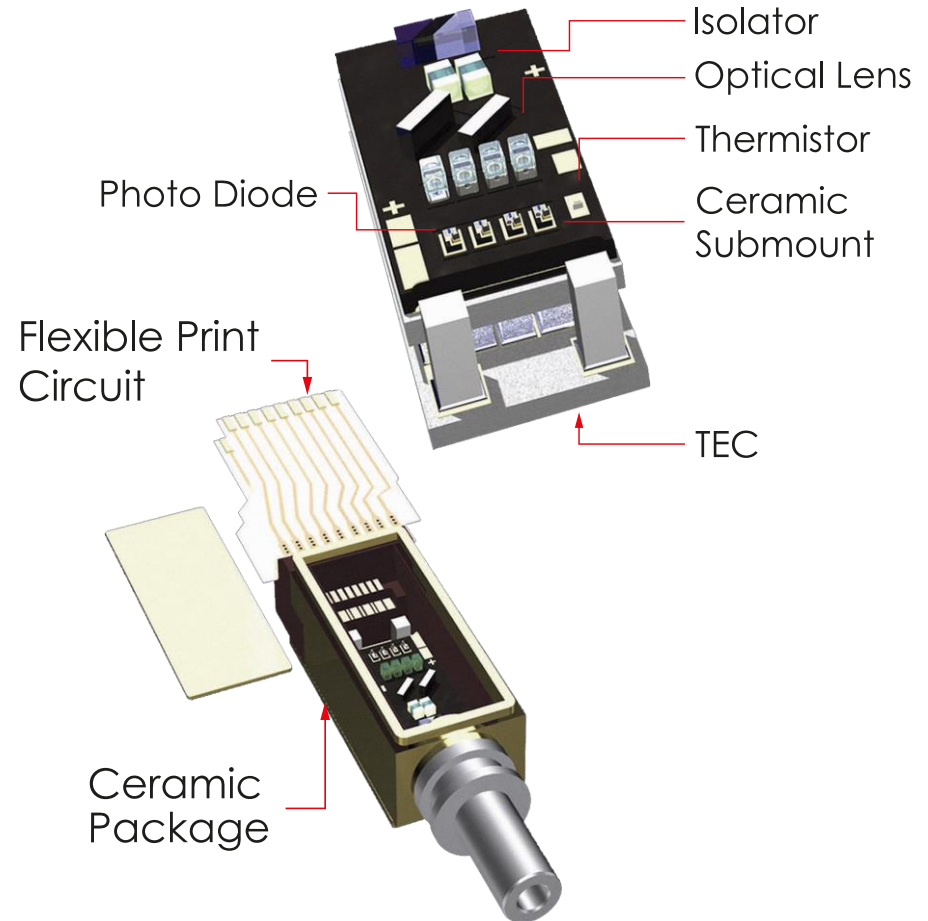
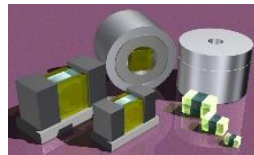
Ceramic Package

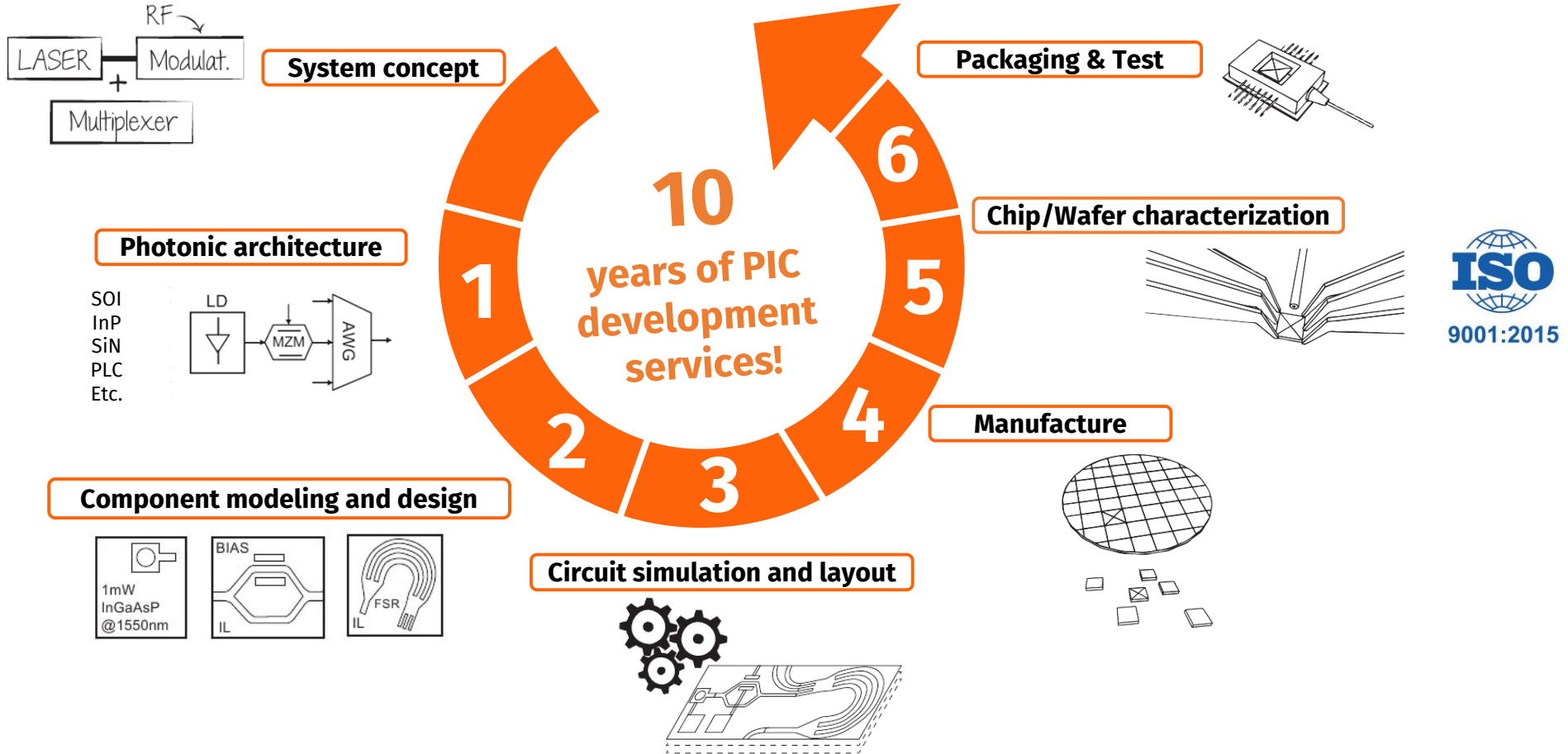


Ceramic Submount



Isolator

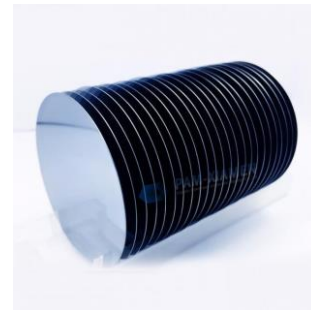




- **It helps to speed up chip development and lower risk and cost, by licensing validated designs that can be embedded into more complex circuits.**
- **Semiconductor design IP has been well established in the last two decades:**
  - +3.6B\$ market in 2018
  - Fabless companies
  - ARM (45%) and Synopsys (17%) dominate market share
  - Most of it is digital electronics design
- **Main categories are:**
  - Processor: CPU, DSP and GPU
  - Interface: protocol-based function like USB, PCI Express, Ethernet, MIPI, SATA, DP, but also Die-to-Die (D2D) interface and memory controller.
  - Other Physical: SRAM and other memory compiler, physical library, Analog & Mixed-Signal, Wireless Interface, etc...

# Differences with photonic design IP

- **Wafer fabs:**
  - Electronic foundry landscape dominated by 5 main players: TSMC, UMC, SMIC, Samsung, GF. Well established IP ecosystem and framework.
  - Photonics foundries are less and smaller. No IP licensing framework.
- **Cost of design IP validation:**
  - >250M wafers/year in electronics, very high yields.
  - Lot's of R&D, NRE and legal expenses required in photonics compared to the possible market, given the lower TRL.
- **Market demand:**
  - Global electronics market is several orders of magnitude larger than photonics one.
  - Most of the photonic product developments are being done by start-ups now.



- **Most of the players have developed a full fab process, or custom module on top of a generic foundry process.**
  - Not so fabless anymore, significant CAPEX tied to a fab (~IDM's)
  - Differentiation not in design but in front-end/back-end
  - Usually offer optical engines = validated PICs
  - No open access libraries or PDKs
- **Lack of standards:**
  - Many new emerging applications: quantum, LIDAR, AI, AR...
  - Design IP is still very customized, limiting its potential customer base
  - Risk of development obsolescence in a quickly evolving field
- **Lots of interesting patented or published designs by academics or small start-ups lack real-world applicability.**
- **Validation for a guaranteed commercial offering still very challenging.**





- ❑ **It is still critical to do extensive component / circuit characterization when validating PIC designs towards production.**
  - Optical alignment
  - Opto-electronic measurement
  - Processing and Root cause analysis
  
- ❑ **When moving to PIC volume production, scalability becomes an issue:**
  - Functional circuit testing is still required beyond fab metrology and PCM
  - Need fast and low cost Wafer/KGD sorting and packaging
  - Parallelization is hard, significant CAPEX and setup time required

# Advantages of outsourcing the photonic back-end

## ☒ Infrastructure investment:

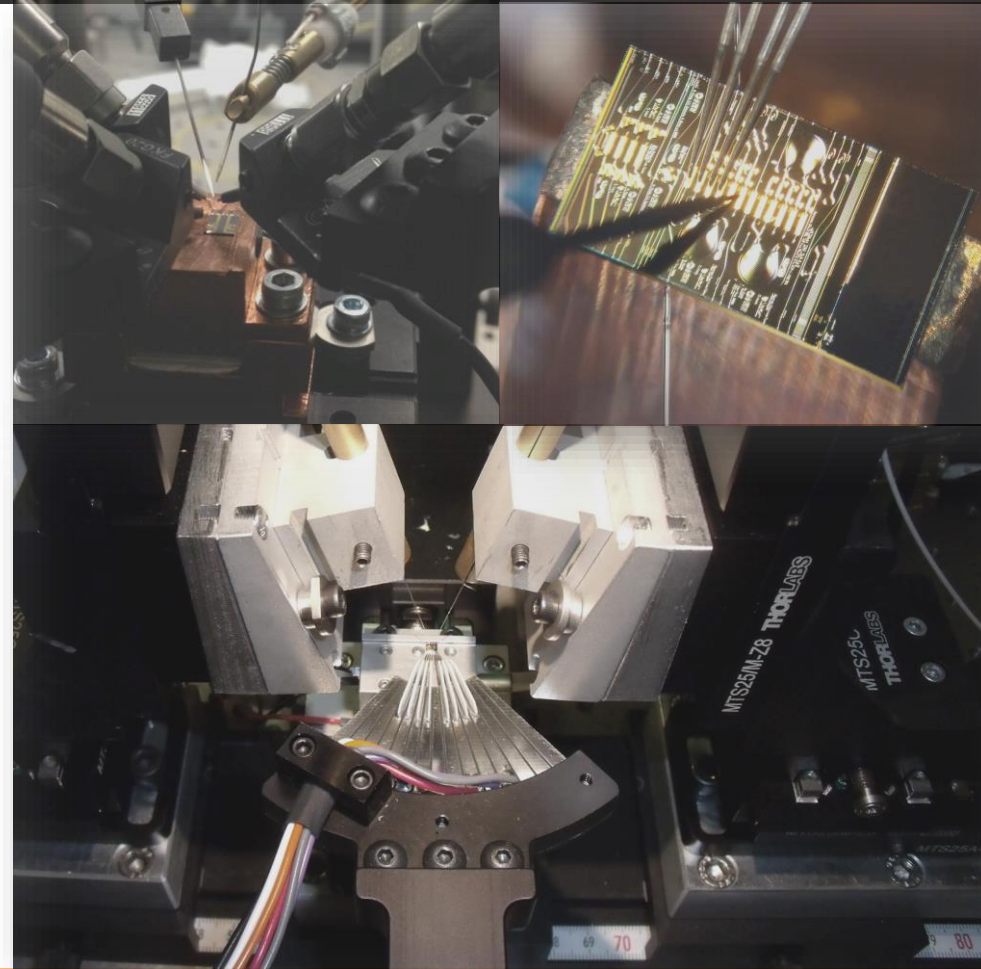
- Cleanroom lab
- Opto-electronic probing stations
- High-end instrumentation
- Consumable stocking
- Redundancy for non-stop operations

## ☒ Engineering expertise:

- Automation
- Photonics
- Big data processing and analysis
- Quality certifications & calibrations

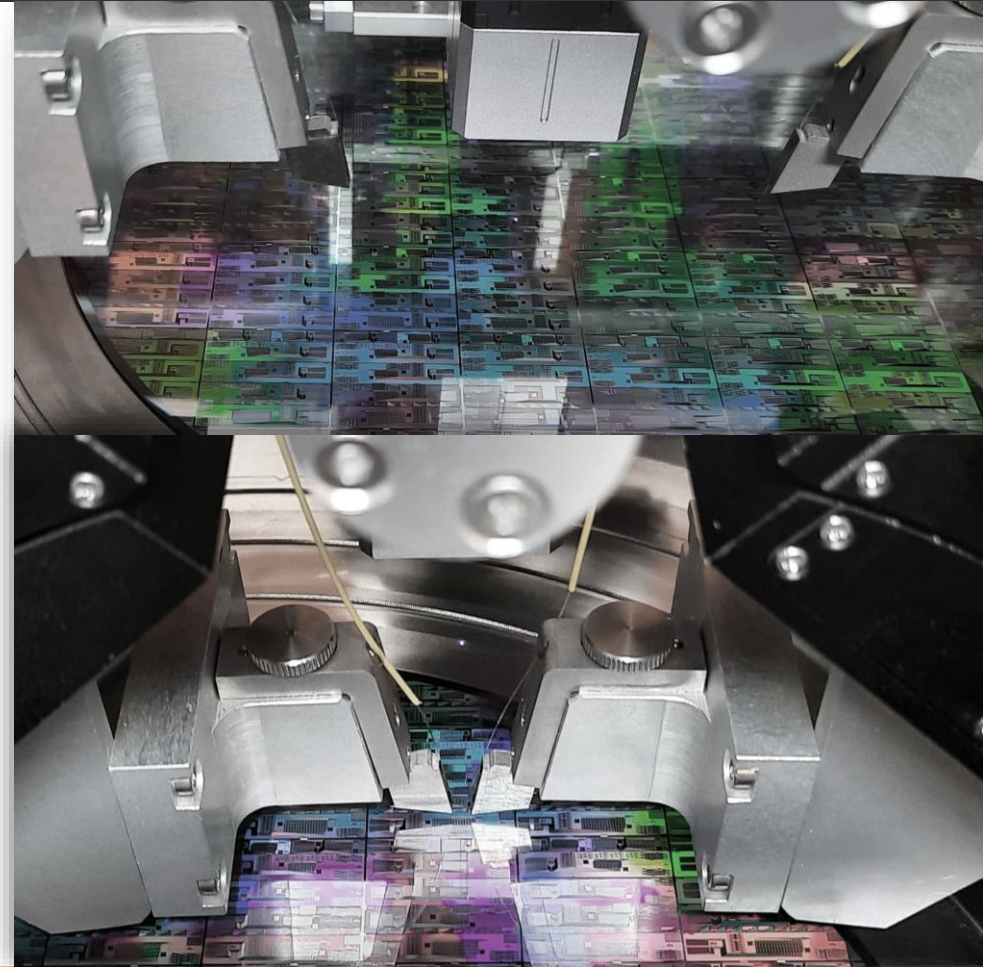
## ☒ Timing:

- Procurement
- Installation and configuration
- Hiring and training



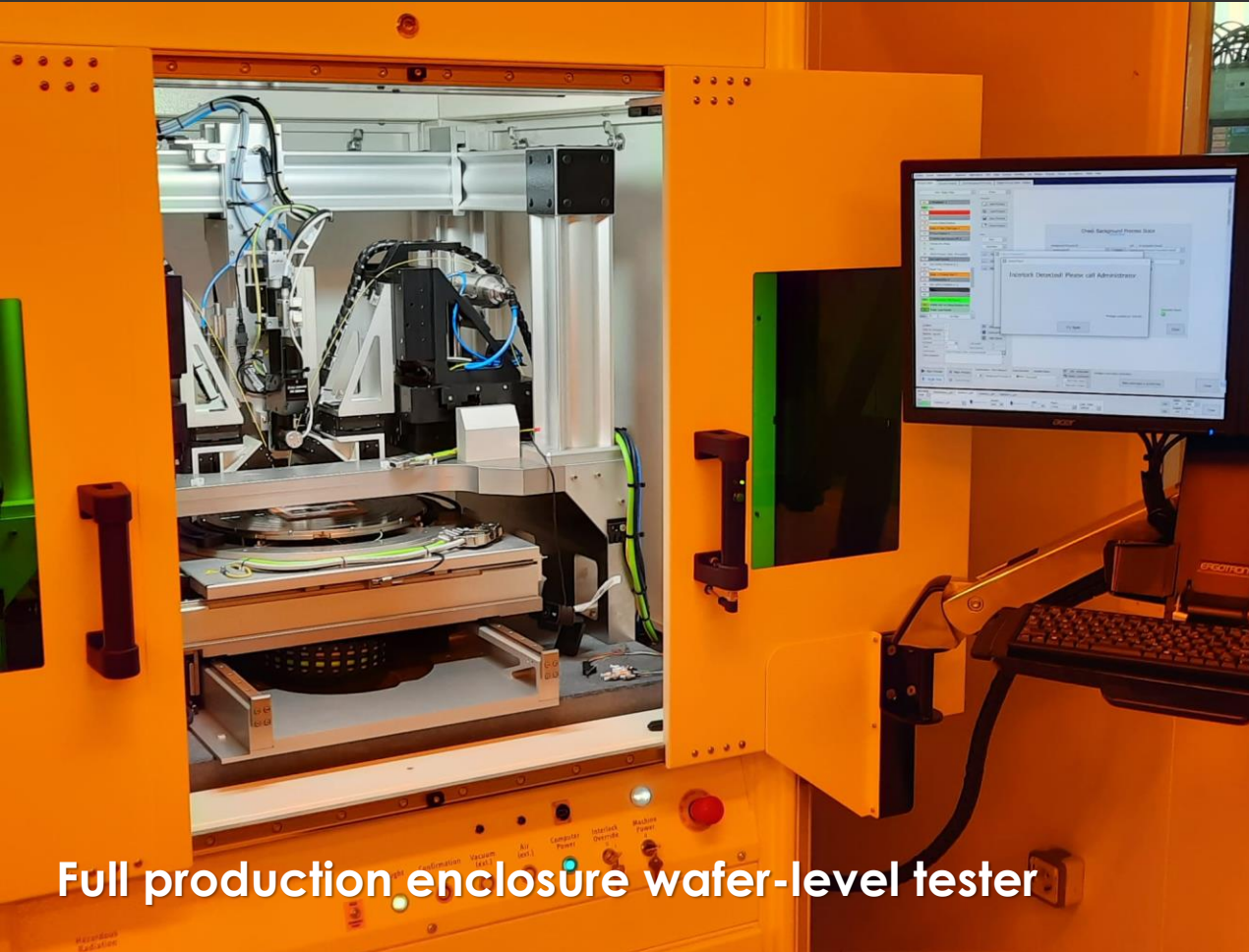
# Focus on characterization & test

- Close design loop from fabricated to measured devices with big data, allowing for statistical parameter modelling.
- Provide feedback to customers & foundries for process yield improvement, to accelerate product development and volume ramp up.
- Automate identification of KGD to sort dies/wafers in production, and towards packaging.

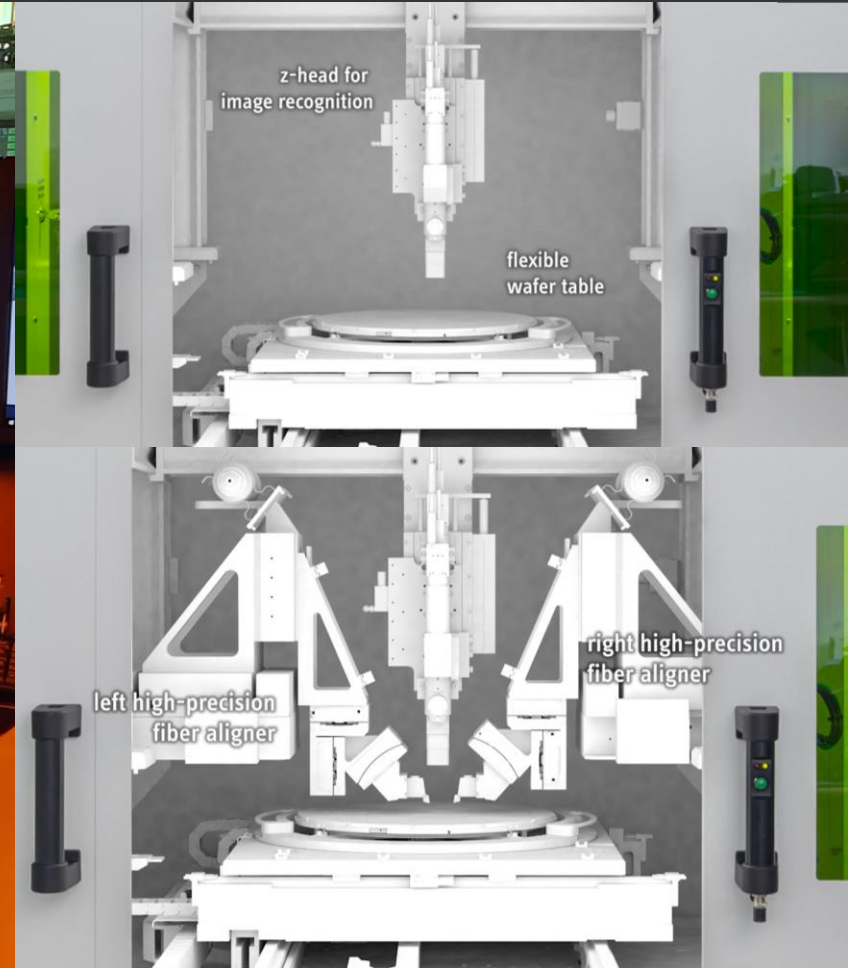




# Automated Wafer-level Photonic tester



Full production enclosure wafer-level tester



z-head for  
image recognition

flexible  
wafer table

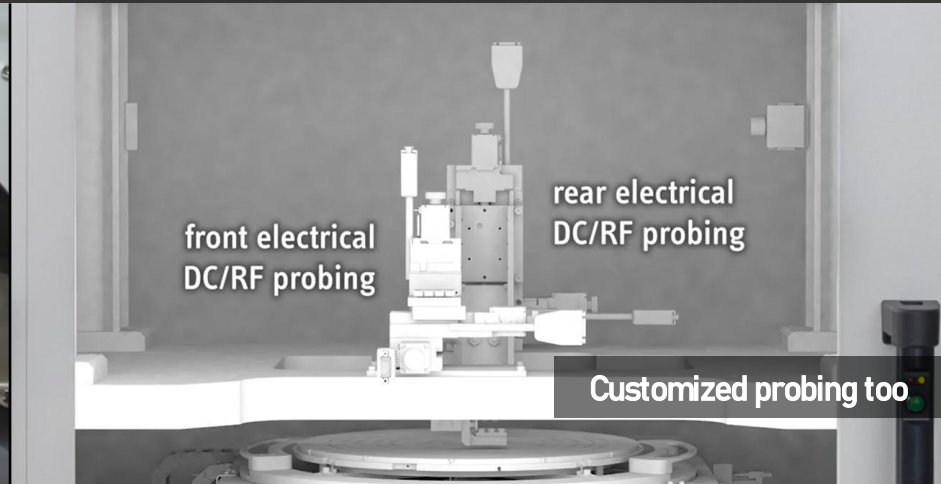
left high-precision  
fiber aligner

right high-precision  
fiber aligner

# Automated Wafer-level Photonic tester



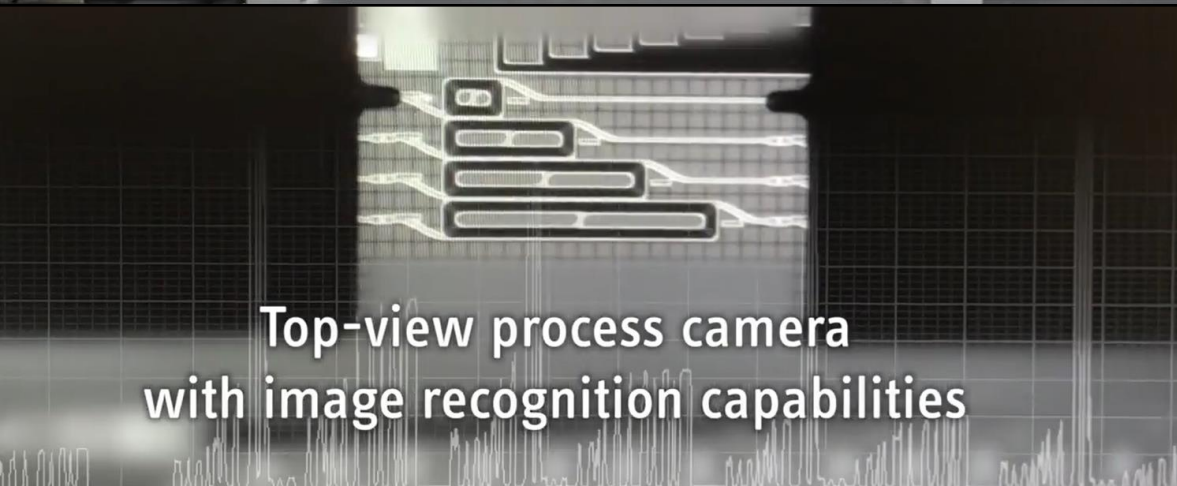
Thermally controlled chuck  
for up to 12" wafers



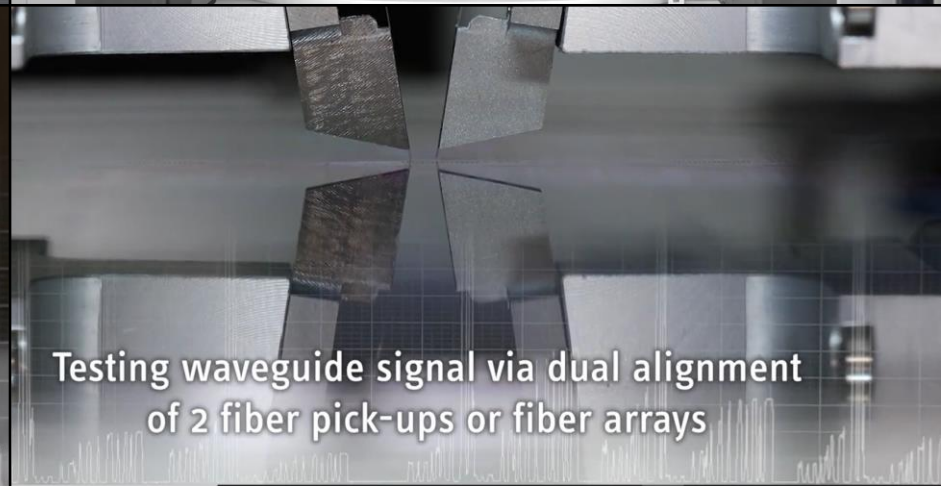
front electrical  
DC/RF probing

rear electrical  
DC/RF probing

Customized probing tool



Top-view process camera  
with image recognition capabilities

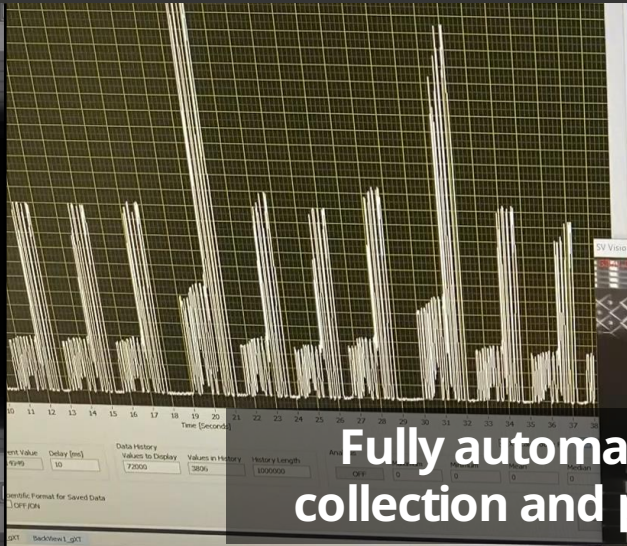


Testing waveguide signal via dual alignment  
of 2 fiber pick-ups or fiber arrays

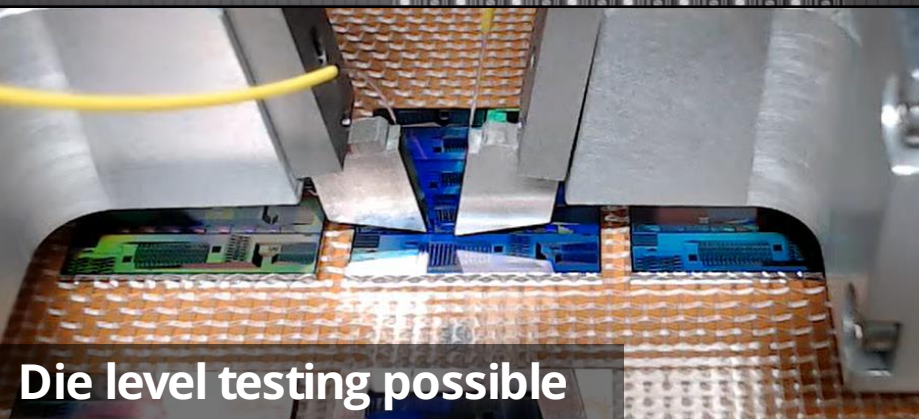
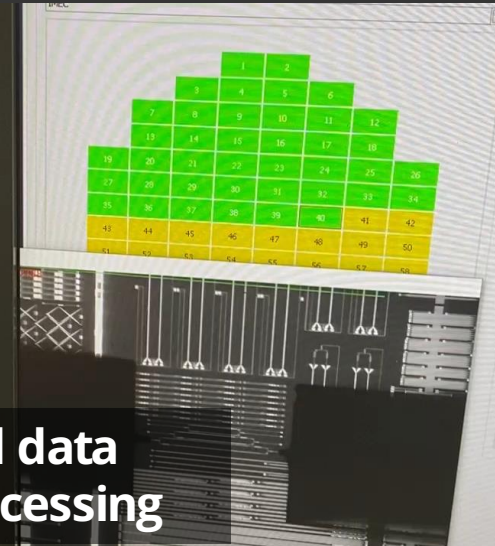


# Automated Wafer-level Photonic tester

<4s optical alignment  
0.1/0.4 dB repeatability  
Depends on fab process and  
grating coupler design



Fully automated data  
collection and processing



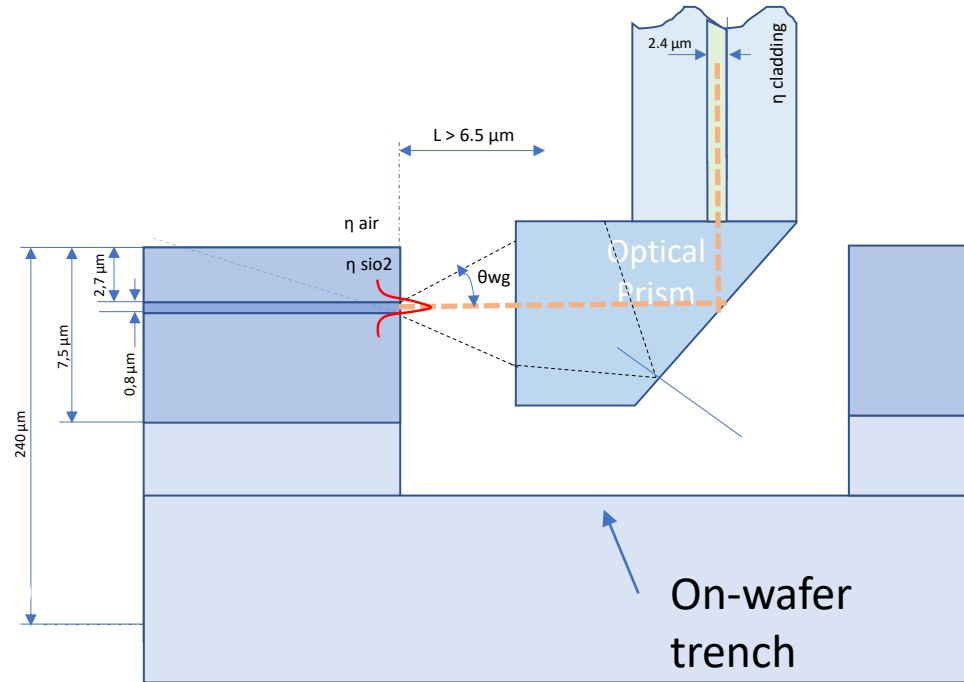
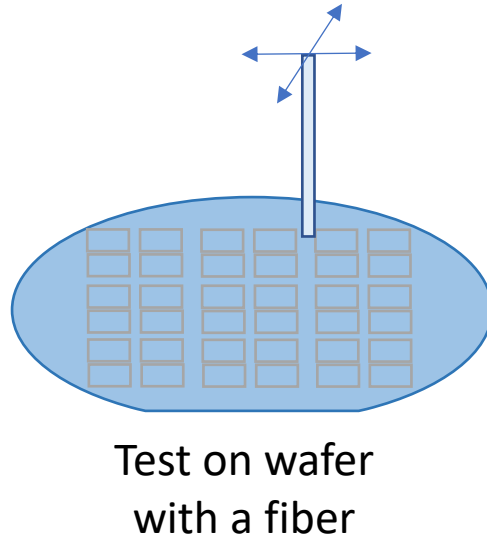
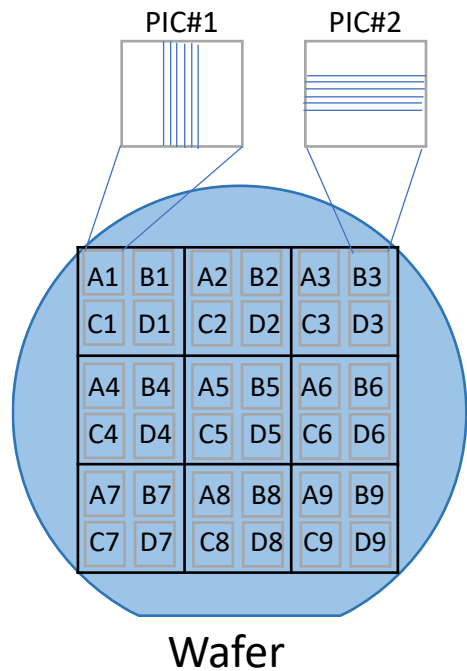
Die level testing possible



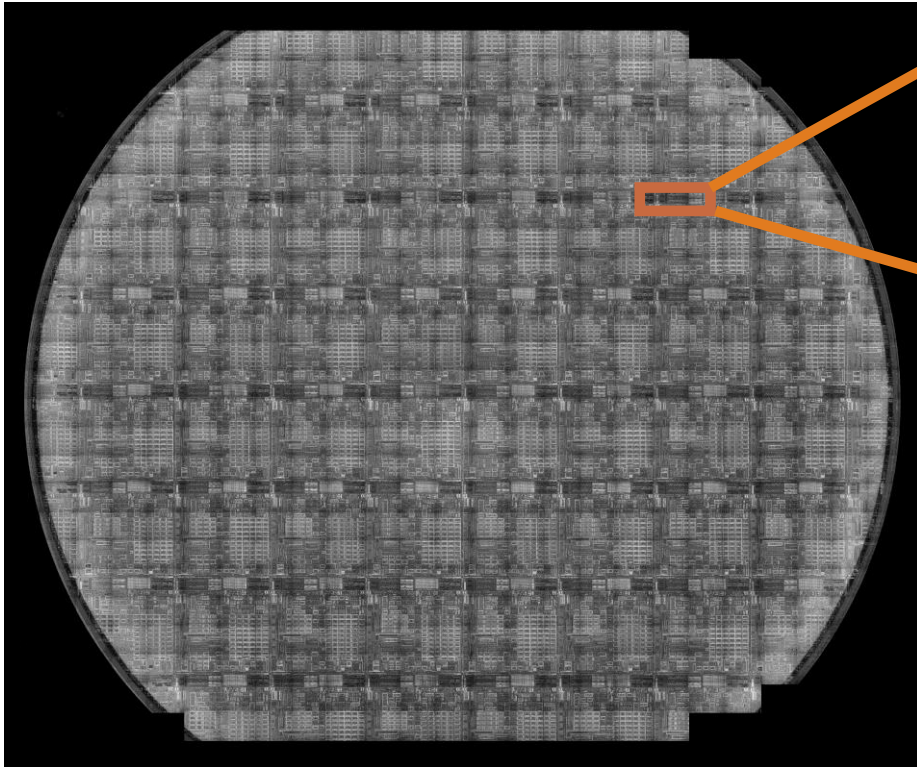
Tool and setup scale-up options

# Edge coupling WLT

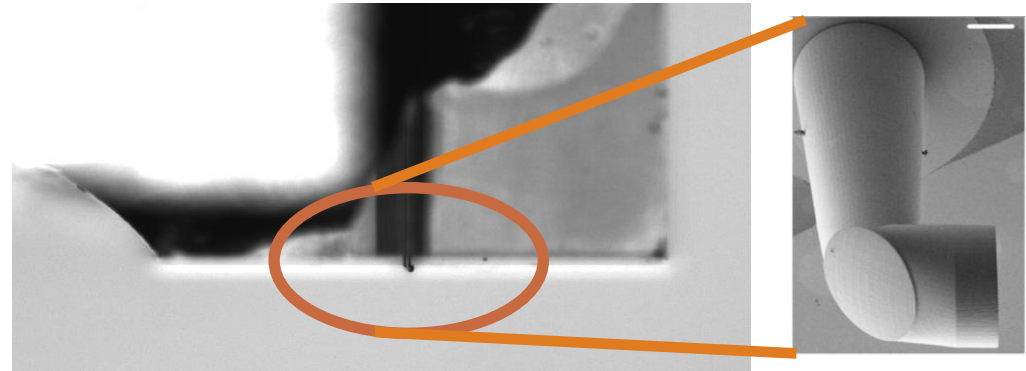
- Tool adapted for optical edge coupling via deep-etch wafer trenches.



# Edge coupling WLT (II)



V-groove  
trenches



3D printed micro-lens

MFD 2.3-10.4  $\mu\text{m}$

# Speed and Repeatability are key

## Examples of previous projects:

DUT	Structures	Measurements
Six 6" wafers, >300 dies	>5k	~50k
Two 8" wafers >1800 dies	>14.5k	~58k
>50 dies	>140	>31k

- Fast probing and trace acquisition times are essential when scaling up.
- Smart characterization plan needed for insightful but time-practical test campaign.

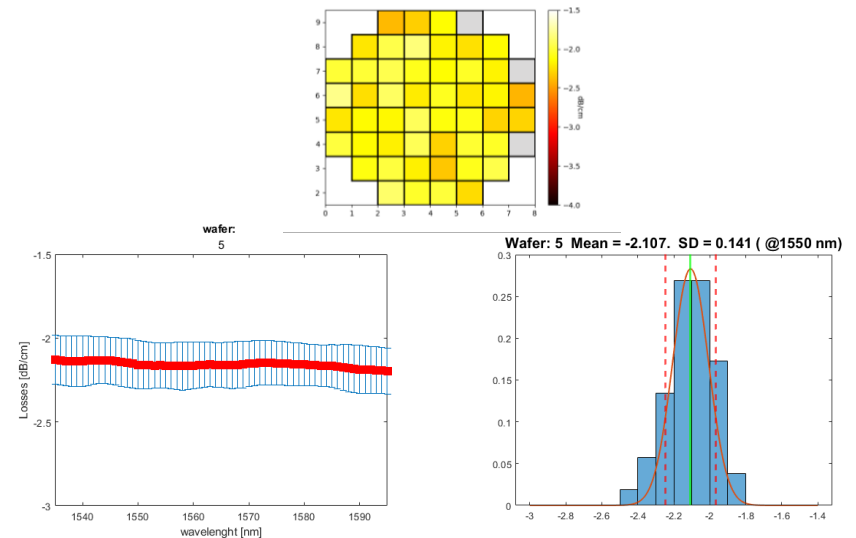
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- Repeatability of bare die measurements with manual alignment is poor (>0.5 dB).
- WLT ensures that alignment and trace acquisition are done automatically with minimal variations (mechanical, thermal etc.)







- **Lightwave Component Analyser (LCA) for parametric testing of devices like high speed modulators in datacom transceivers.**
  - 110 GHz Turn-Key Test System for Optical RX and TX
  - Suitable for die and wafer level testing
  - Return to zero and nonreturn-to-zero (RZ / NRZ) and pulse amplitude modulation (PAM) formats
  - S-parameter testing over the full 1260 nm to 1620 nm range
  - Available for both automated die and wafer level testing

1. To develop design IP or productize any PIC, **characterization and test** are significant **cost & time bottlenecks**.
2. To produce state-of-the-art PICs in volumen, any **photonic back-end technology needs to be scalable** from the start.
3. **VLC/Hitachi High-tech** have the resources and expertise to support PIC developments all the way to production.

# Thank you for your attention!

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Contact details

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