

Silicon Photonics and Electronics for High-Speed Transceivers

Peter Ossieur, on behalf of the IDLab-Design and Silicon Photonic colleagues

Upcoming targets - pluggable transceivers

Ethernet Alliance 2022 roadmap



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Upcoming targets - co-packaged transceivers

- Co-packaged Optics Collaboration www.copackagedoptics.com and OIF
 - 3.2Tb/s Optical Module to support 51.2Tb/s switch: 16 modules surrounding switch ASIC



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Silicon Photonic Platforms for High-speed Optical Transceivers



- Co-integration of passive and active components supporting 56-128Gb/s lane rates
- Most components are available for O-band and C-band operation

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High-Speed Silicon Photonic Modulators - example demonstrations

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Carrier-depleted Mach-Zehnder Modulator

Reference O-band design in IMEC PDK

Phase Shifter

P++



Rib Waveguide

P+ P/N N+

N++



Traveling-Wave MZ Modulator	Value	Unit
Phase-shifter length	I.5	mm
DC Insertion Loss @ 0V	~2	dB
Vπ @ 0V	10.5	V
S21 Bandwidth @ IV	37	GHz
SII (0.1 GHz—I GHz) @0V	< -15	dB

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 - Features Optical Equalizer as additional means to trade V_{π} versus bandwidth
 - On-going development work



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MZM w. OEQ					
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MZM	3.1	6.13	4.96	32.4	

- Dual-polarization IQ modulator for coherent transceiver applications
 - Features Optical Equalizer as additional means to trade V_{π} versus bandwidth
 - On-going development work
- View MZM as tapped delay line (FIR filter) (pat.)
 - Introduce taps through choice of phase shifter length sections
 - Introduce crossings for tap sign inversions





High-Speed Silicon Photonic Modulators - example demonstrations Vertical pn-junction ring modulator

From lateral to vertical pn junction



Y. Ban et al., IEEE Optical Interconnects Conference 2019: "Low-Voltage 60Gb/s NRZ and 100Gb/s PAM4 O-band Silicon Ring Modulator", OI conference 2019.

High-Speed Silicon Photonic Modulators - example demonstrations Vertical pn-junction ring modulator

• From lateral to vertical pn junction: improved modulation efficiency



Diode Type	ν _π L _π (V.cm)	Loss (dB/cm)	ME (pm/V)
LPN	0.71	97	30
VPN	0.42	86	47

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60Gb/s NRZ



50Gbaud PAM-4

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High-speed Silicon Photonic modulators

C-band GeSi Electro-absorption modulator

Franz-Keldish effect modulator on Silicon Photonic platform



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Franz-Keldish effect modulator on Silicon Photonic platform



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Silicon Photonics Platform

On-going developments



 O-band QCSE electro-absorption modulator integrated and waveguide-coupled in a Silicon Photonic platform



S.A. Srinivasan et.al., "60Gb/s waveguide-coupled O-band GeSi quantum-confined stark effect electro-absorption modulator", OFC'2021, paper Tu1D.3

Silicon Photonics Platform

On-going developments



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Drive voltage: 2Vpp

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Electronic front-ends for 100Gbaud operation and beyond

SiGe BiCMOS front-end electronics



- 4-ch. linear Mach-Zehnder modulator driver
- STM 55nm SiGe BiCMOS
- •~90GHz bandwidth, 2.5Vpp swing
- Linear response, Traveling wave based



SiGe BiCMOS front-end electronics



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- STM 55nm SiGe BICMOS
- •~90GHz bandwidth, 2.5Vpp swing
- Linear response, Traveling wave based



- 4-ch. linear transimpedance amplifier array
 STM 55nm SiGe BiCMOS
- ~60GHz bandwidth
- Linear response, trav. wave based



Ultra high-speed signal generation 120Gbaud capable multiplexer / equalizer











120Gbaud capable 4:1 multiplexer and equalizer

- Symbol-spaced, 7-tap equalizer
- Analog bandwidth >80GHz bandwidth, >1Vpp drive
- Power consumption including input decoding of 4x quarter-rate input channels: 2W

M.Verplaetse, H. Ramon, N. Singh, B. Moeneclaey, P. Ossieur and G.Torfs, "A 4-to-1 120Gb/s PAM-4 MUX with a 7-tap mixed-signal FFE in 55nm BiCMOS", *Custom Integrated Circuits Conference* (CICC 2021), April 2021.



Ultra high-speed signal generation

Quad channel 106Gbaud 2:1 multiplexer with modulator driver and clock generator





Input-side, each channel: two 53Gbaud PAM-4 input signals (for example)

Function: linear interleaving, amplification using modulator driver (single-ended EAM driver in this case)

Output-side, each channel: one 106Gbaud PAM-4 output signal (for example)

Ultra high-speed ADCs and DACs

- Conventional approaches such as time-interleaved SAR-ADC running into limitations
- Research focussed on breaking through these limitations





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Specification	ADC Research Targets
Technology	5nm CMOS
Sampling rate [GS/s]	> 150
3dB bandwidth [GHz]	> 60
Resolution	7
Full scale ENOB	5 6
Power [mW]	Targeting record efficiency
Specification	DAC Research Targets
Specification Technology	DAC Research Targets 5nm CMOS
Specification Technology Sampling rate [GS/s]	DAC Research Targets 5nm CMOS > 150
SpecificationTechnologySampling rate [GS/s]3dB bandwidth [GHz]	DAC Research Targets 5nm CMOS > 150 > 60
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Conclusion

- Next-generation optical transceivers to support Terabit/s capacities
 - Energy efficiency: pJ/bit
 - Density: Gb/s/mm or Gb/s/mm2
 - Low-cost: \$/bit

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- Next-generation optical transceivers to support Terabit/s capacities
 - Energy efficiency: pJ/bit
 - Density: Gb/s/mm or Gb/s/mm2
 - Low-cost: \$/bit
- Solutions according to trade-offs
 - Ultra high baudrate:
 - Integration of novel materials onto photonics platforms to achieve modulation and detection bandwidths
 - Advanced packaging, co-development with electronics critical
 - Optical IO
 - Ultra high integration density and low power

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