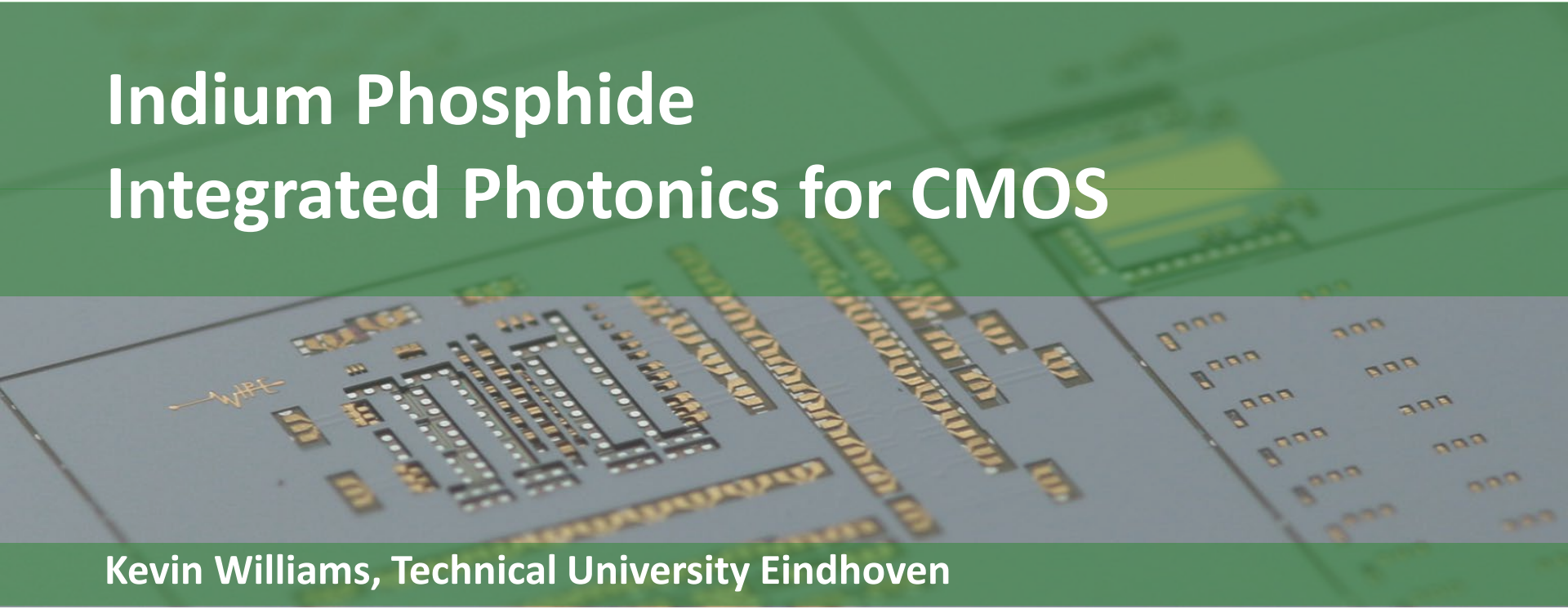
7-8 September 2022

EHCI EINDHOVEN HENDRIK CASIMIR INSTITUTE TU/e

Indium Phosphide Integrated Photonics for CMOS



Kevin Williams, Technical University Eindhoven

EPIC Meeting on CMOS Compatible Integrated Photonics at imec, Leuven, Belgium

Outline

Photonic integration research at Eindhoven

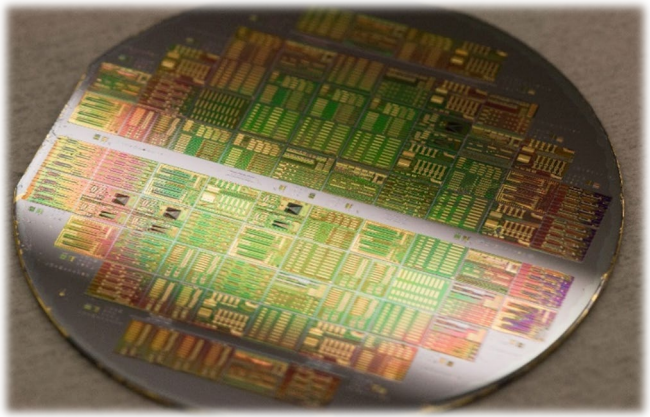
High-performance, foundry-compliant InP integrated active devices

Electronic-photonic integration

Integrating with semicon manufacturing

Outlook

Photonic Integration Research in Eindhoven



Research group numbering over 50 within the larger Hendrik Casimir Institute

Full process technology from epitaxial (re)growth to wafer bonding and dicing

Design and test with use cases from sensing to communications

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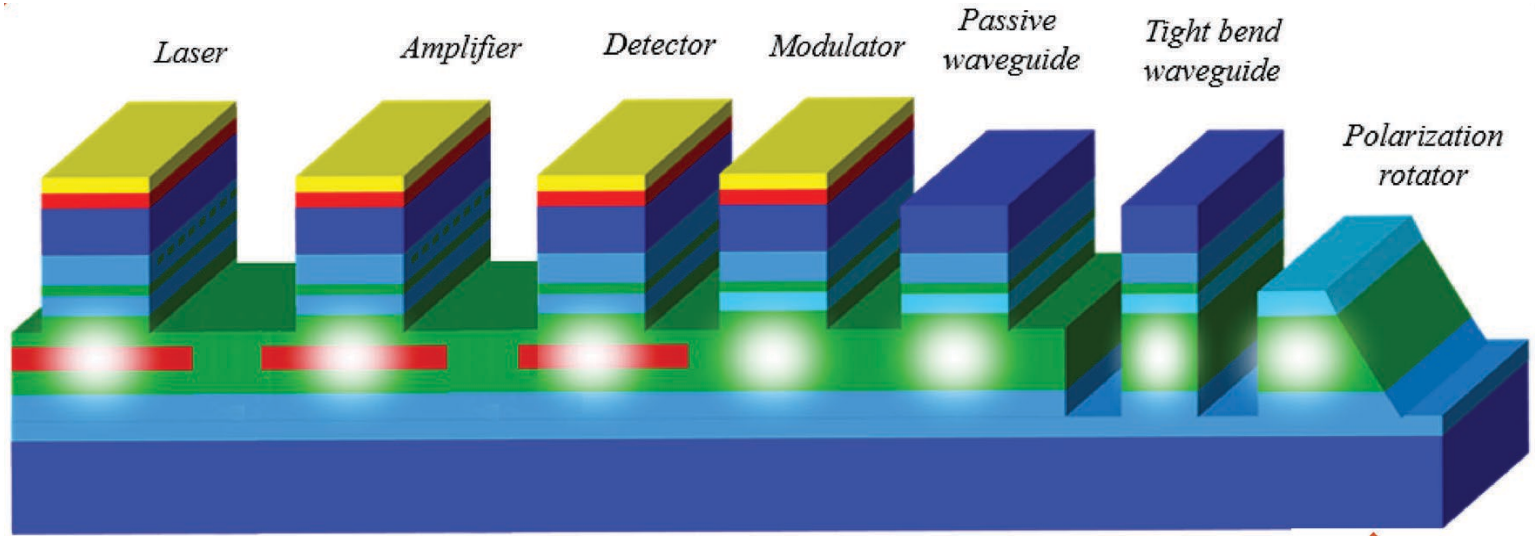
Indium phosphide integrated photonics

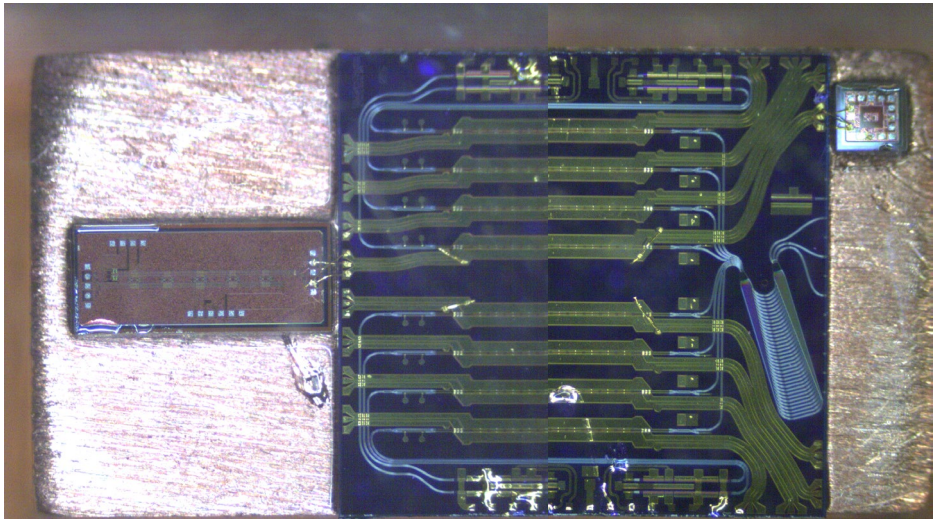


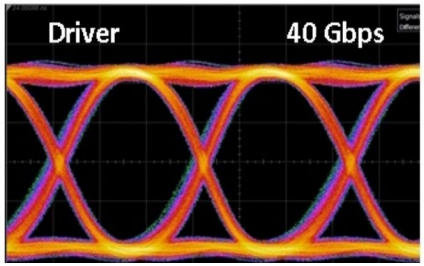
No compromise photonic integration platform with native lasers, amplifiers, MQW modulators, InGaAs detectors plus passives

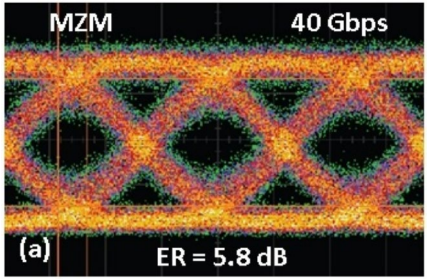
Optical interfaces designed in at mask level for reproducibly low parasitics

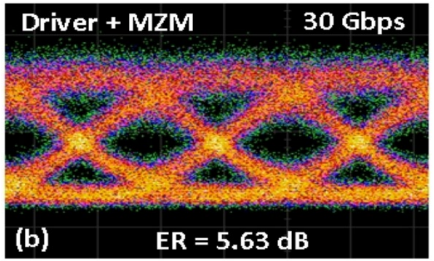
But InP PICs at 3 & 4" wafer sizes.

Electronic photonic co-design









Layout and circuit matching between SiGe driver and terminations on NXP process and Oclaro PIC.

Decoupling capacitors and inductors removed through co-design.

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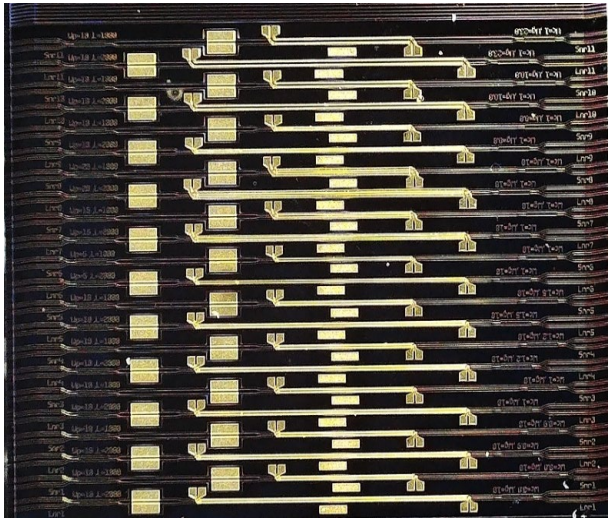
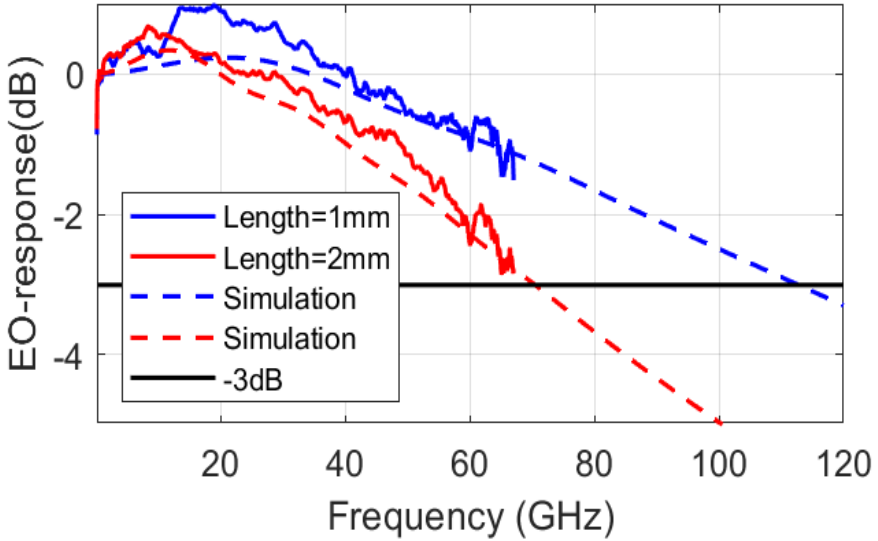
High Speed and High Density Modulators



High density Mach-Zehnder modulators on a 4.6 x 4.0 mm² MPW cell



Measured small signal electro-optic performance.

Ultrawide band modulators with narrow 25 micron pitch on the SMART Gen 2 platform through impedance and velocity matching

High-Density 100 GHz-Class Mach-Zehnder Modulators integrated in a InP Generic Foundry Platform, Meighan et al., CLEO 2022

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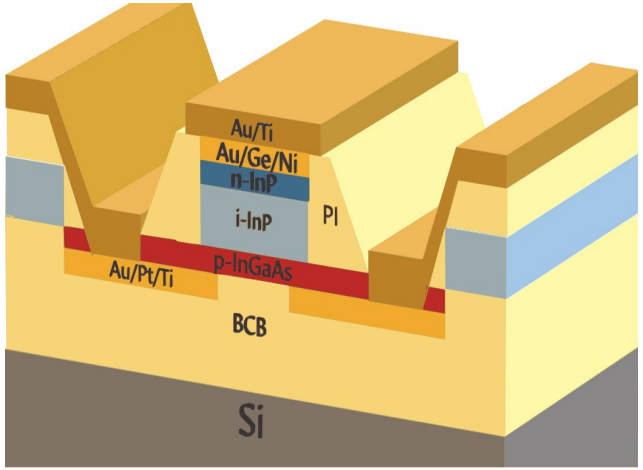
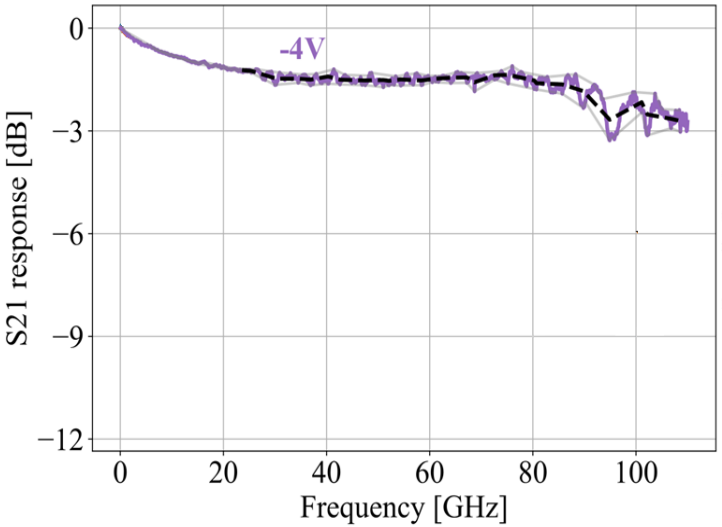
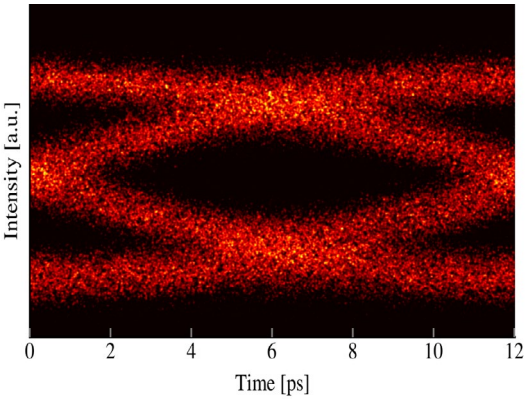
Miniaturising detectors to micron-scale







Speed of processing and detecting light detection limited by the electronic connections, but ever smaller devices allow ever-wider bandwidth

Uni-travelling carrier detectors on the IMOS nanophotonic platform

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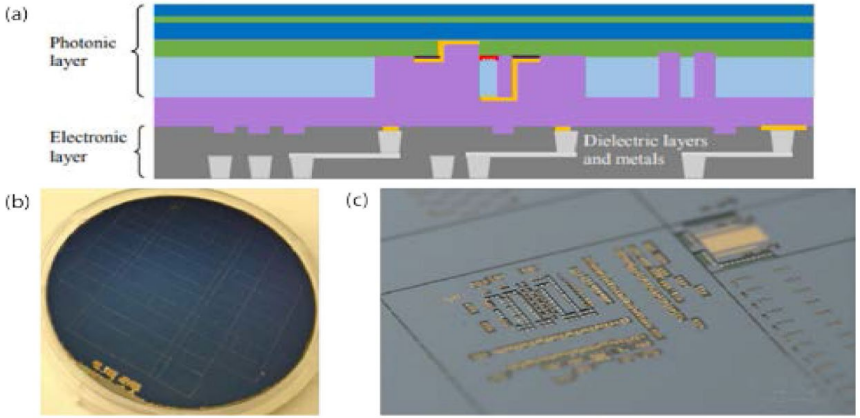
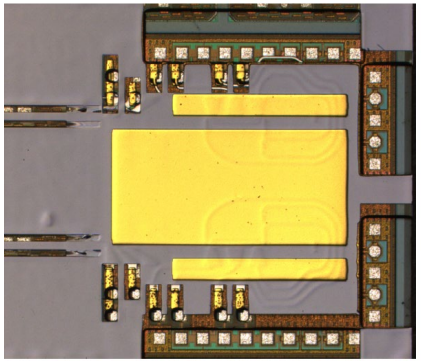
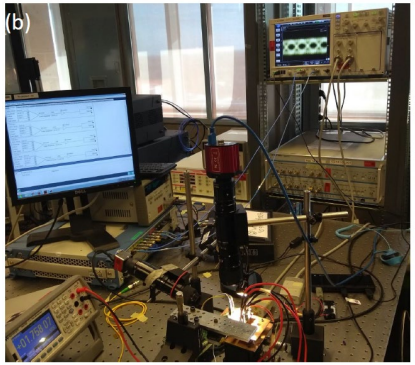
Wafer bonding electronics and photonics



Wafer bonding concept, and realisation for 3” wafers. InP PIC from HHI.



Detail for DFB laser in SiGe electronics



Lab evaluation of receiver with imec, Ghent

Yao et al., 'Towards the integration of InP photonics with silicon electronics: Design and technology challenges', JLT, 39, 4, 999, 2021
Spiegelberg, 3D–Integration on Wafer Level of Photonic and Electronic Circuits, PhD thesis, 2021

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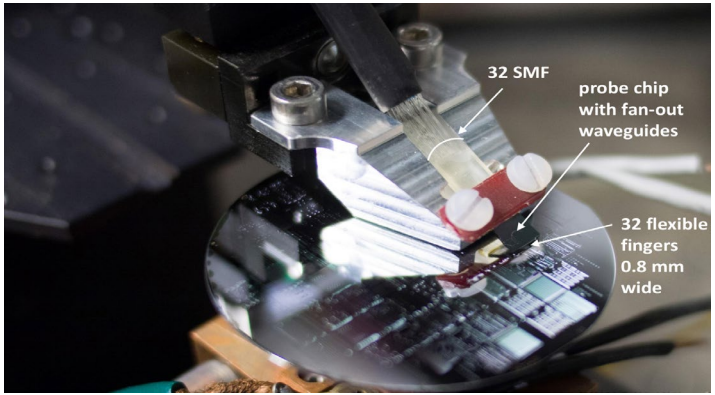
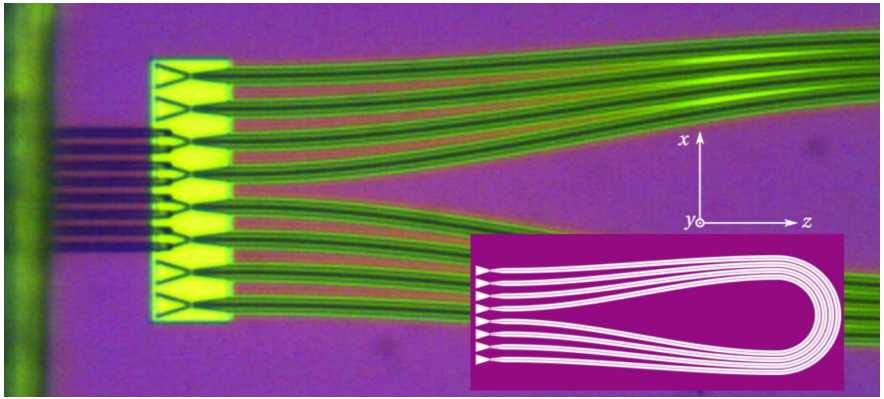
Wafer scale optical input and output



Passively connecting SiN and InP waveguides.
32 can be landed simultaneously



Eight SiN flexible waveguides visible left, landing on a InP PIC;
Example shown with Lionix waveguides and Oclaro PIC

Wafer scale connection of InP PICs using flexible SiN waveguide arrays

Self-aligning micro-structures allow reproducible passive interconnection

High Density Multi-Channel Passively Aligned Optical Probe for Testing of Photonic Integrated Circuits, Leijtens et al IEEE Photonics Journal, 13, 1, 2021

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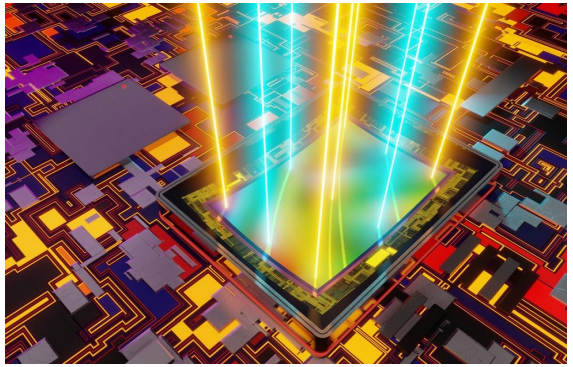
200mm and beyond with transfer printing

Density: techniques for amplifiers and modulators targeting pitches of 10 microns.

Multi-band-gap coupons: Amplifiers, lasers, and modulators all in the same coupon

Low parasitics: Active-passive regrowth for non-absorbing, low-reflection vertical tapers between active PICs and silicon nitride photonics

Yield: 193nm scanner lithography for sub-100nm critical dimension and sub-20nm mask overlay for precision mode-matching and manufacturability



Project partners:

imec embracing a better life

XCeleprint

SMART PHOTONICS

AMIRES

THALES Building a future we can all trust

UNIVERSITY OF CAMBRIDGE

INSPIRE

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https://www.inspire-h2020.eu/

Outlook

- **Density roadmap**: Indium phosphide and imos nanophotonics providing component density scaling
- **100GHz class** components demonstrated. Limited primarily by design and test rather than technology
- **Codesign** methods to integrate electronics and photonics at 3‘’ wafer scale
- **200mm and beyond**, supporting high-density micro transfer printing with route to yield
- **Foundry access**: becoming available as an industry service with a rapidly maturing design, fab and test eco-system at jeppix.eu

Acknowledging researchers

and partners

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