# Silicon Photonics Platform: Current and Future Trends

Philippe Absil, VP R&D

**EPIC Meeting on CMOS Compatible Integrated Photonics at imec**

# Imec Leuven

**Hyperspectral imaging lab & demo room**

**Integrated imagers lab**

**Smart sensor lab**

**Exascience lab**

**NERF labs**

**300mm cleanroom**
- (High-NA) EUV, Attolab, advanced patterning
- State-of-the-art etch, implant, cleaning, metrology, deposition, ... equipment from leading-edge OEMs
- Ballroom type of cleanroom (7,200m$^2$, Class 1,000)
- 24/7operational

**Measurement & testing lab**

**Material and device characterization labs**

**Bio labs**
- Cell & tissue culture labs
- Optical labs
- Wet chemistry labs
- Clinical labs
- Pre-PCR lab
- Neuropixels lab

**RF & high-power lab**

**Photonics labs**

**200mm cleanroom**
- Silicon pilot line for prototyping and low-volume manufacturing
- iSiPP200 and iSiPP50G photonics prototyping platform
- 200mm GaN-on-Si platform
- Quantum computing lab
- 5,200m$^2$

**GaN Lab**

WORLD-CLASS INFRASTRUCTURE

**> 12,000 $M^2$**

**CLEANROOM**

CAPACITY

MORE THAN

**5,000 SKILLED PEOPLE**

FROM OVER 95 NATIONALITIES

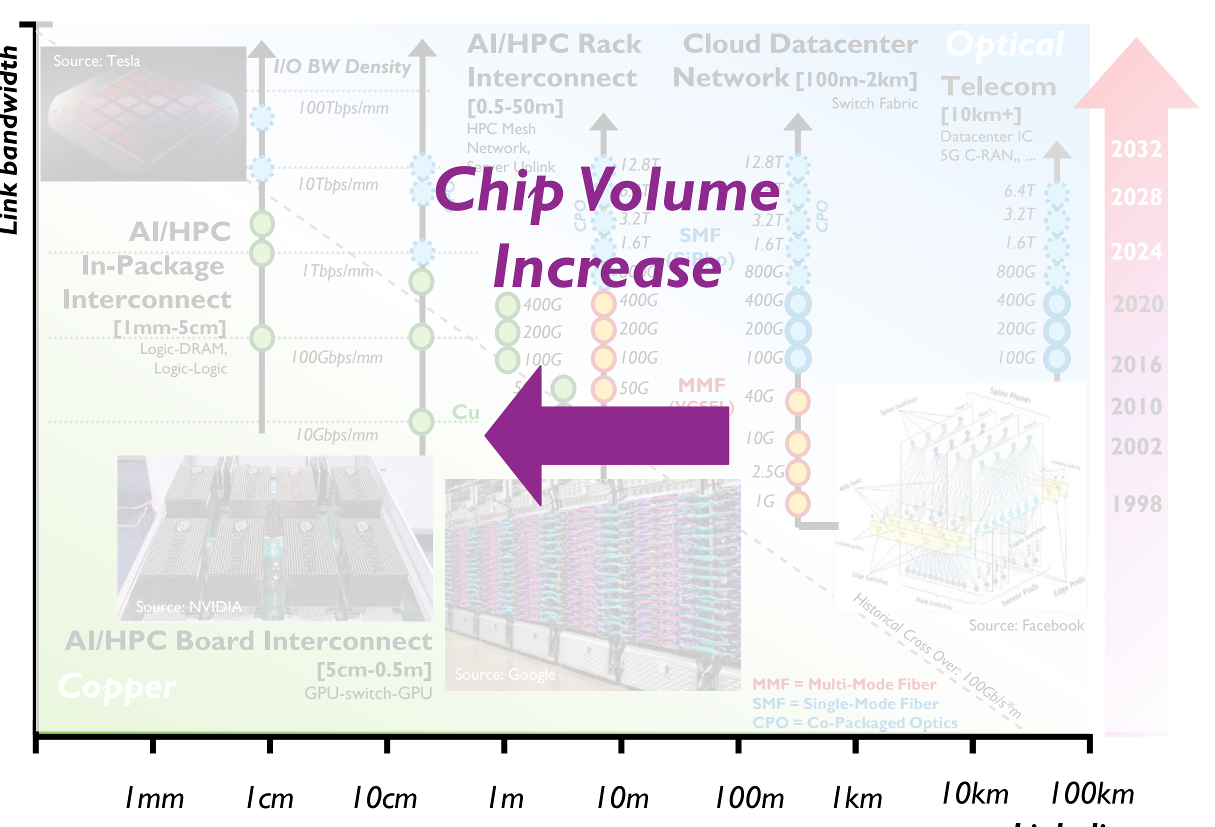
A

**TRUSTED PARTNER**

FOR COMPANIES, STARTUPS & ACADEMIA

# Silicon Photonics Has Become An Industrial Reality

# Optical Interconnect Landscape and Roadmap

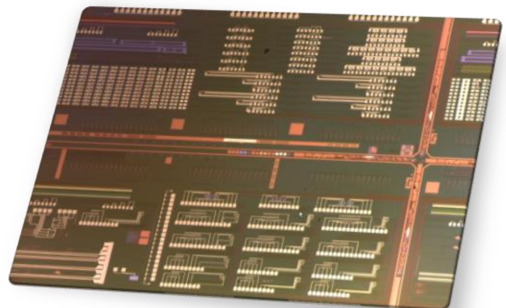



- **Multi-Terabit/s Optical Interconnectivity** needed by **mid 2020's, driven** by **Cloud** and **AI/HPC**
- **Optical Interconnects** will move into the **rack, board and package**
- **Silicon Photonics** is a **key enabling technology** for **Terabit-scale Optical Interconnects,** from **1cm to 100km+**

# Silicon Photonics Benefits

- Chip level integration of various photonic functions
  - Integration of complex optical functions (passive / active)
  - Large-scale integration
  - Integration electronics and photonics

- Wafer-scale processing using existing CMOS-fabs
  - CMOS-shared Production Infrastructure
  - Focus on <u>one</u> common technology
  - Re-use of advanced CMOS development

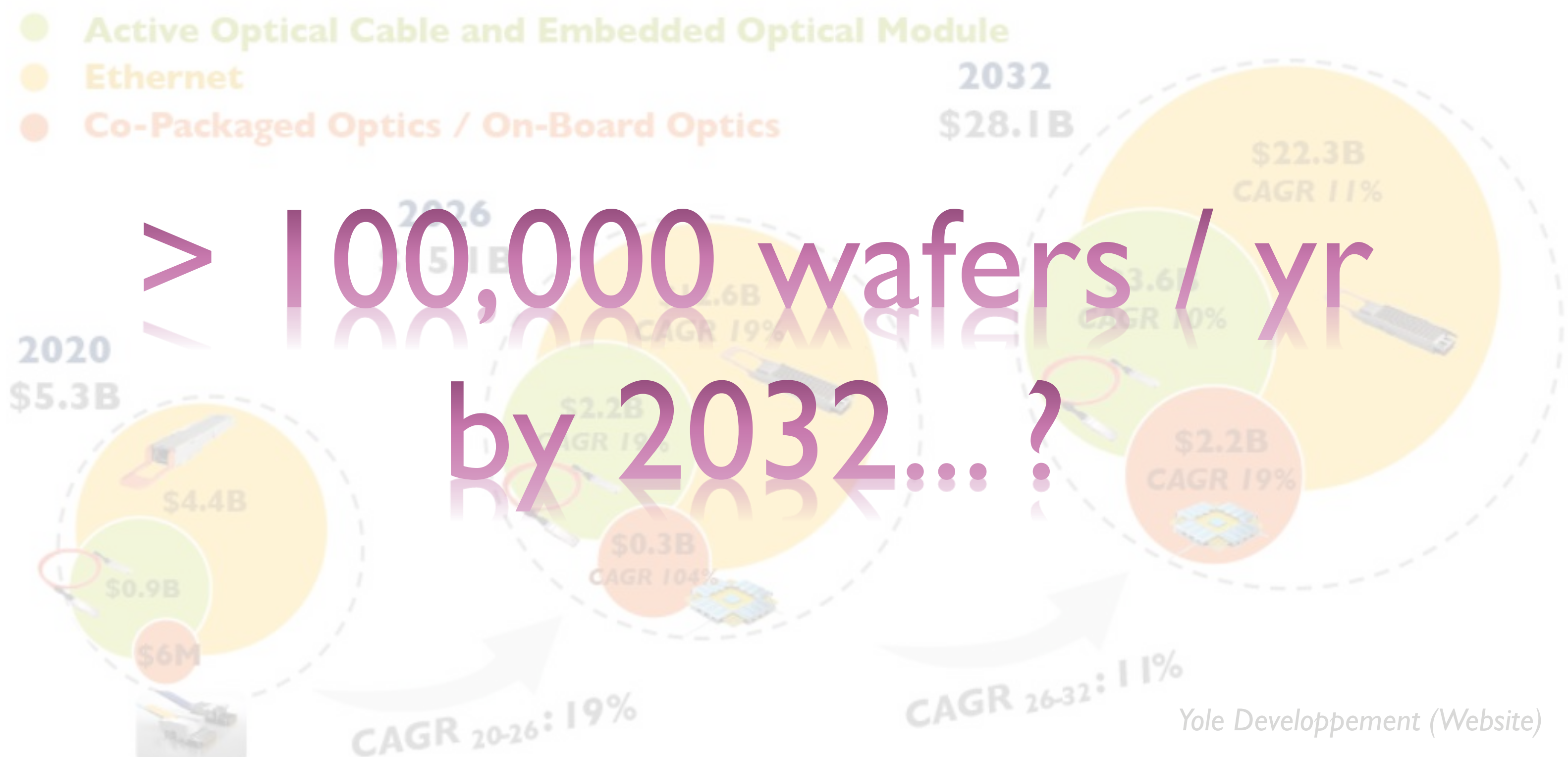




PUBLIC

# Datacom Optics Revenue Growth Forecast

The market driven by 1.6T and 3.2T optical engines

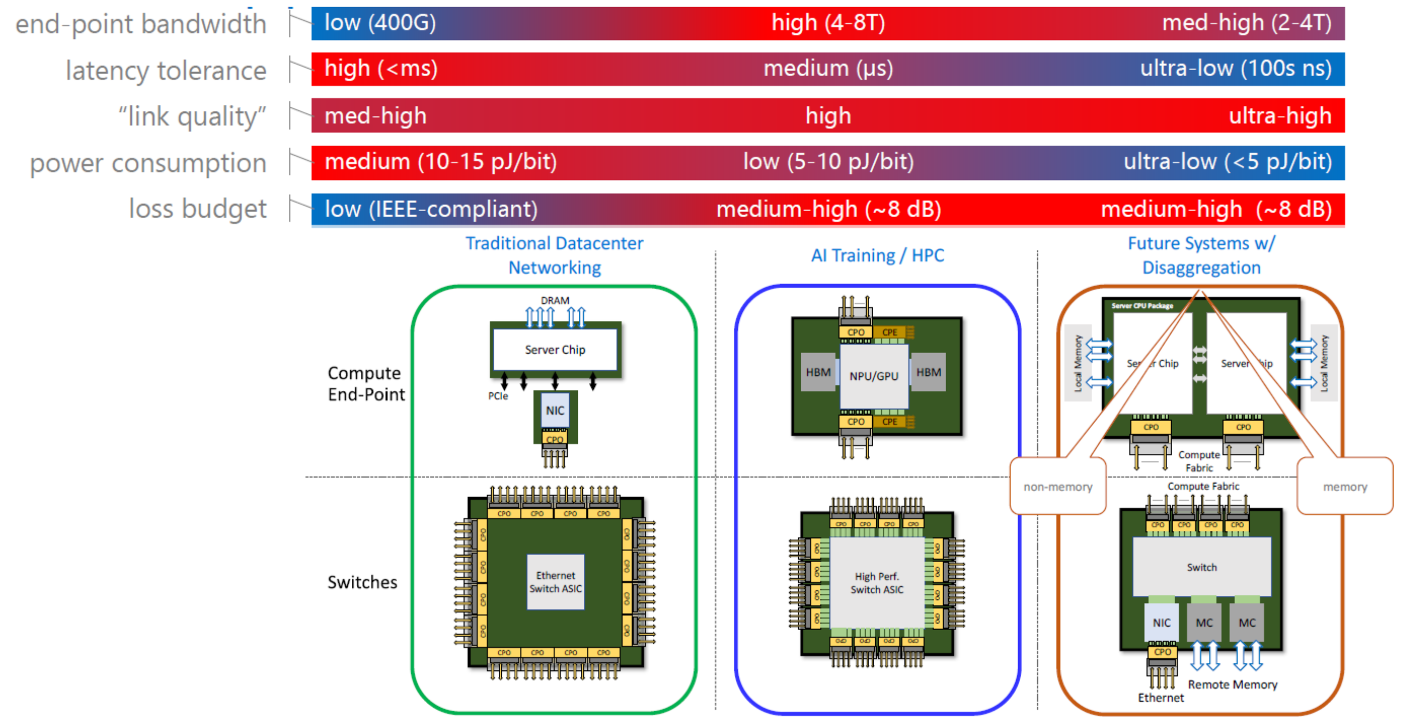



> 100,000 wafers / yr by 2032... ?

*Yole Developpement (Website)*

# Optical Interconnect Requirements

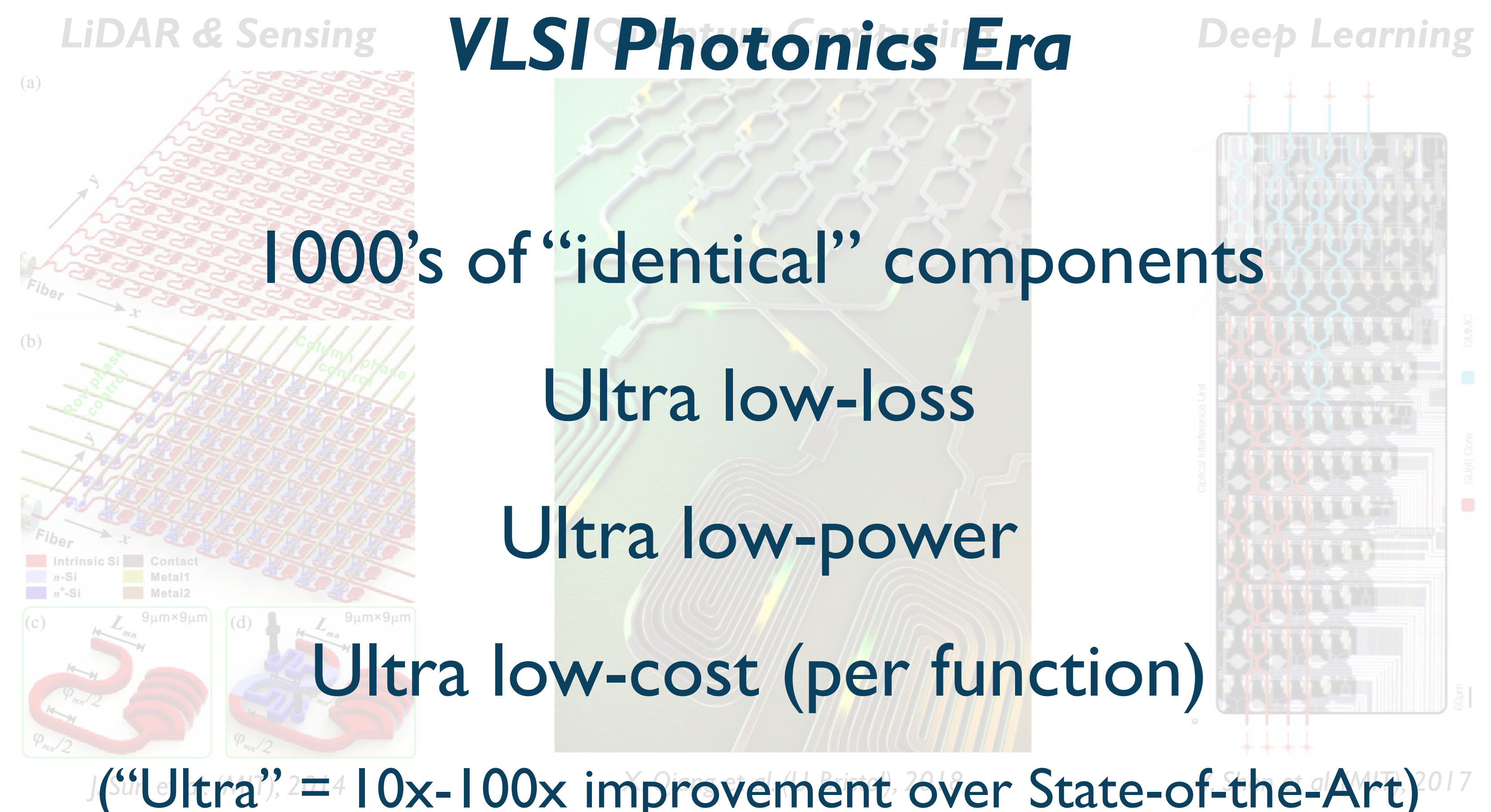
*Specific to the Application*




***Reference**:*
*M. Filer (Microsoft), ARPA-E Phase-2 Kick-Off Meeting, Jan 2021*

- **AI/HPC** and **System Disaggregation** have the **most demanding** optical link specifications

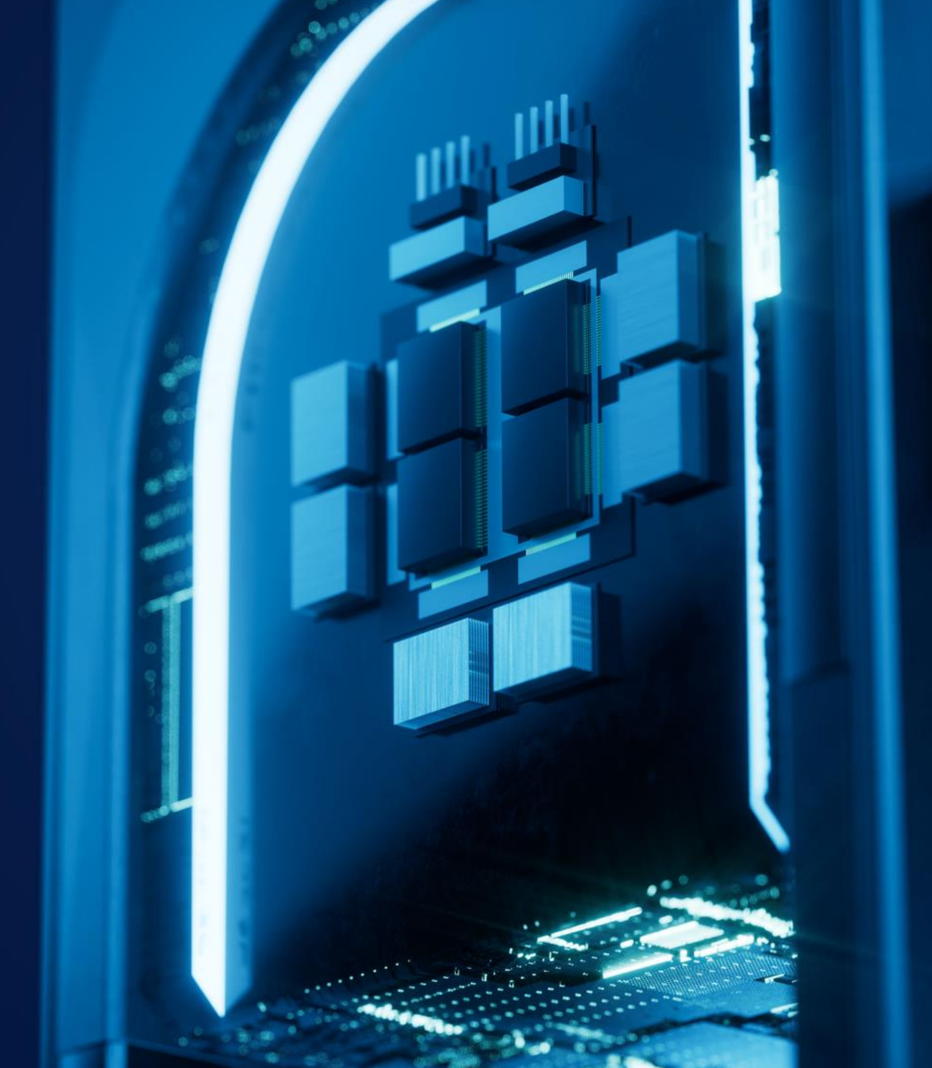
# Emergence of new applications





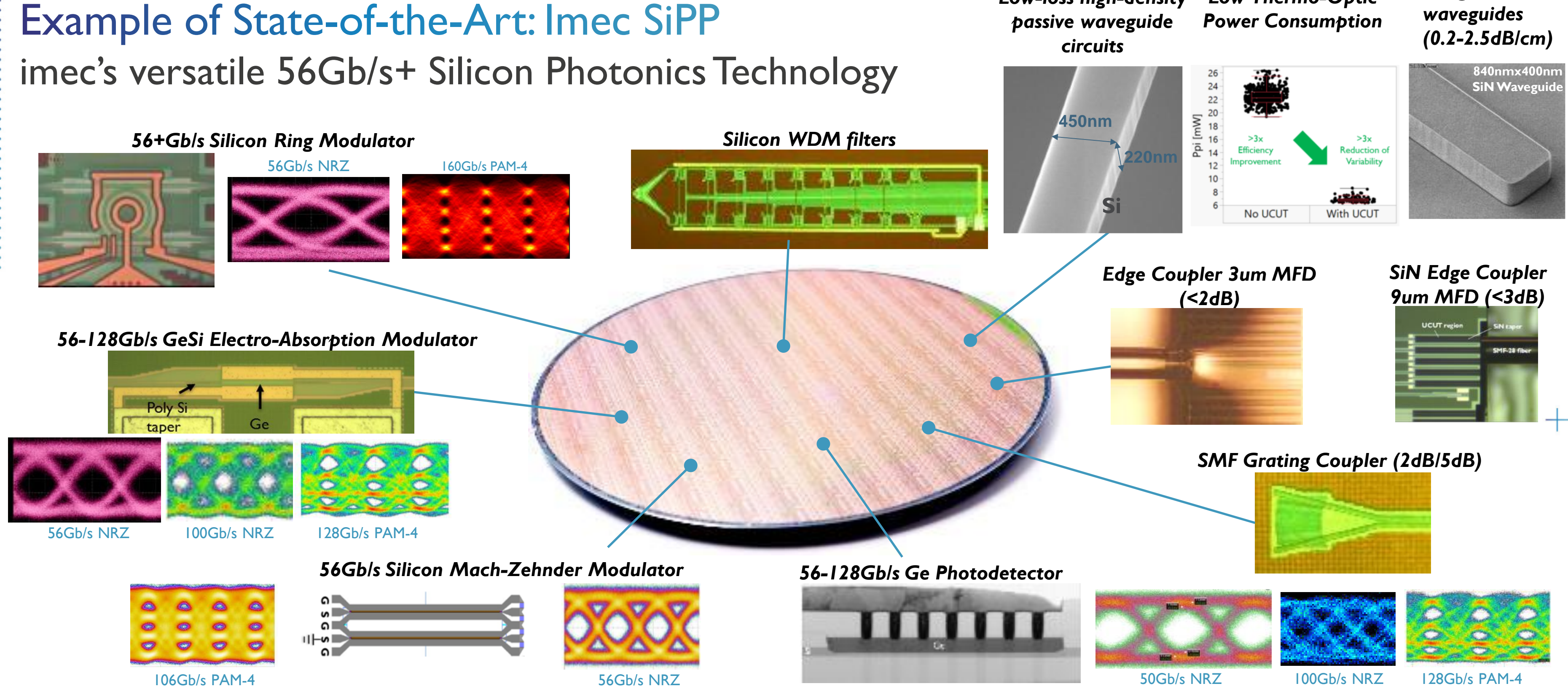

PUBLIC

# Current State-Of-The-Art



# Example of State-of-the-Art: Imec SiPP

## imec's versatile 56Gb/s+ Silicon Photonics Technology

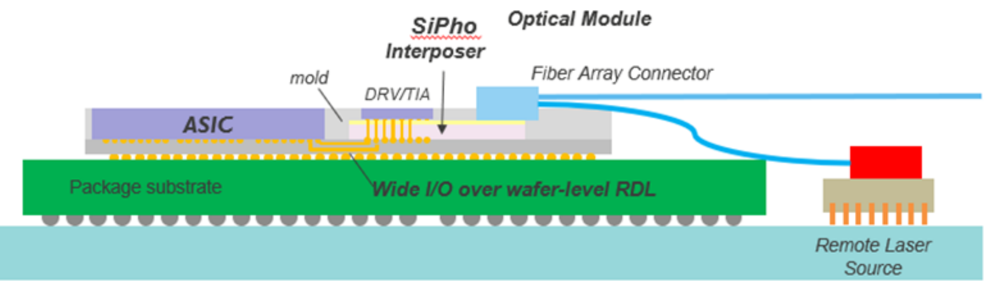


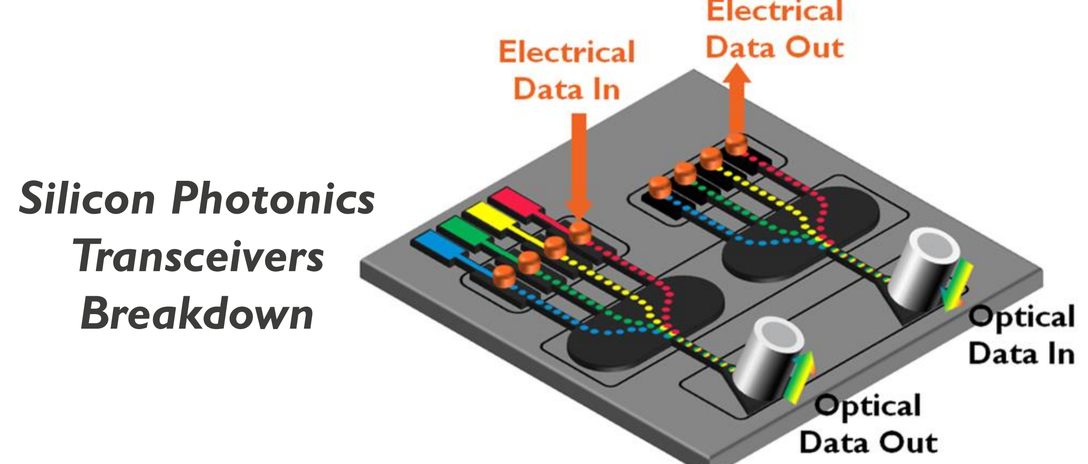

**Fully Integrated Silicon Photonics Platform for 1310nm/1550nm Wavelengths**

- Low-loss Passive Silicon Waveguide Devices and Fiber Coupling Structures
- 56Gb/s+ (Ge)Si Modulators and Ge(Si) Photodetectors

PUBLIC

# PIC Technology Challenges




***Photonics*** **PPAC Challenges**

- ✓ Device Optical Insertion Loss
- ✓ Device E-O Conversion Efficiency
- ✓ Device E-O Conversion BW
- ✓ Device dimensions
- ✓ Heterogeneous Integration Cost

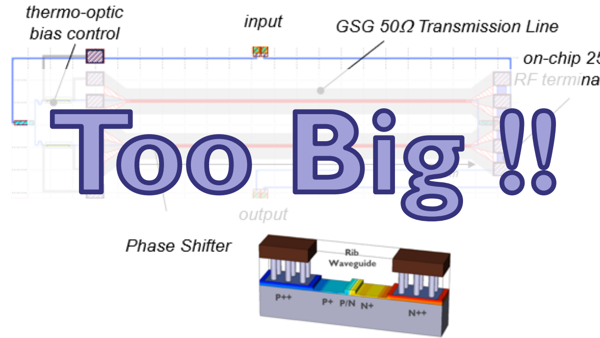


PUBLIC

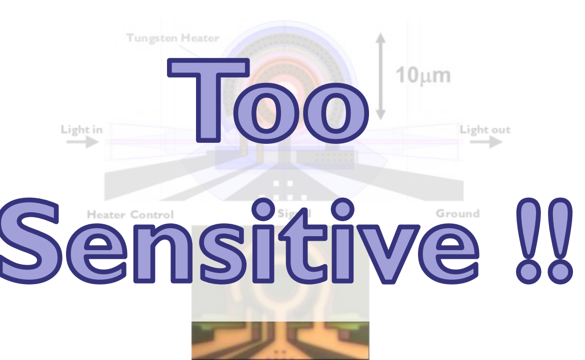
# E-to-O Conversion: The Optical Modulator

"Conventional Approaches"

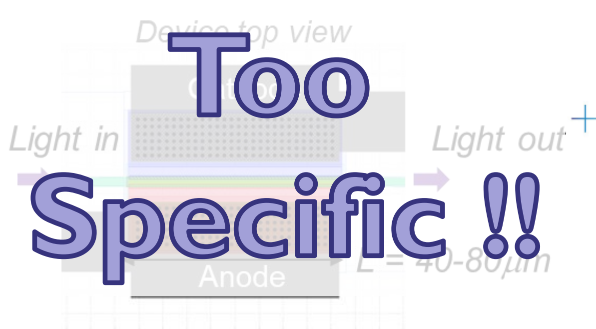
(industry reference)




## MRM




## GeSi EAM

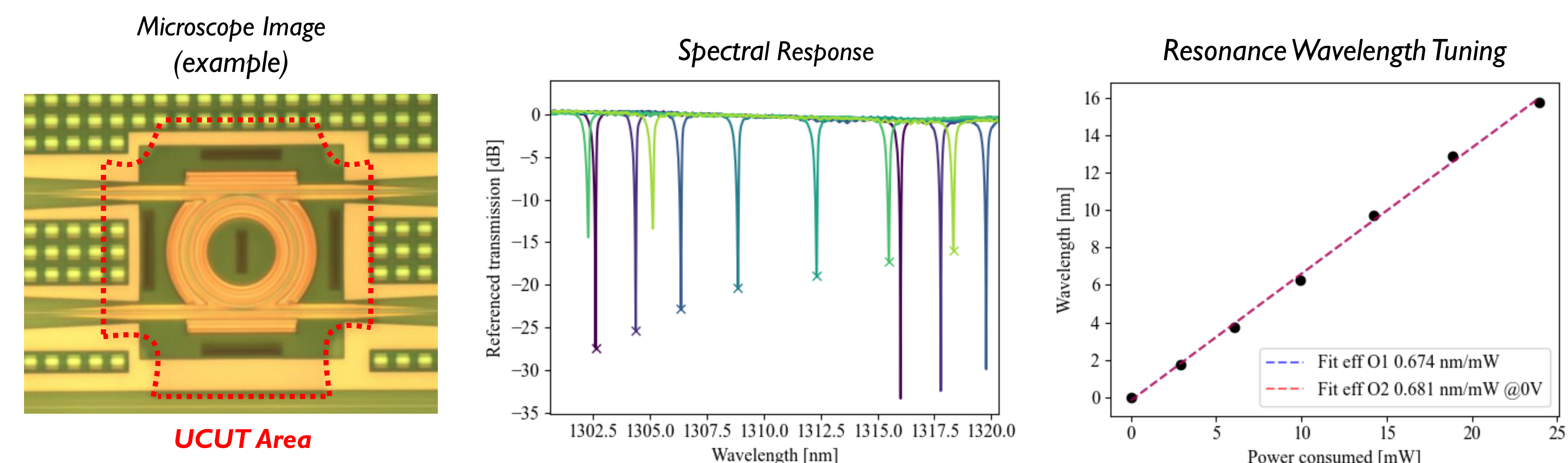





PUBLIC

# Silicon Ring Modulator

## *High-Efficiency Heaters with Si Substrate Undercut (UCUT)*



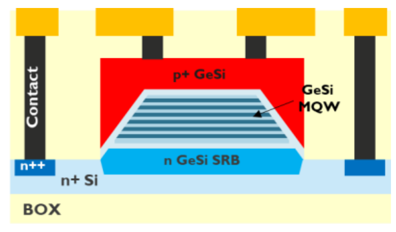

High-Speed Si Ring Modulator with **Undercut Si Substrate** achieves **0.68nm/mW** or **118GHz/mW** thermal tuning efficiency

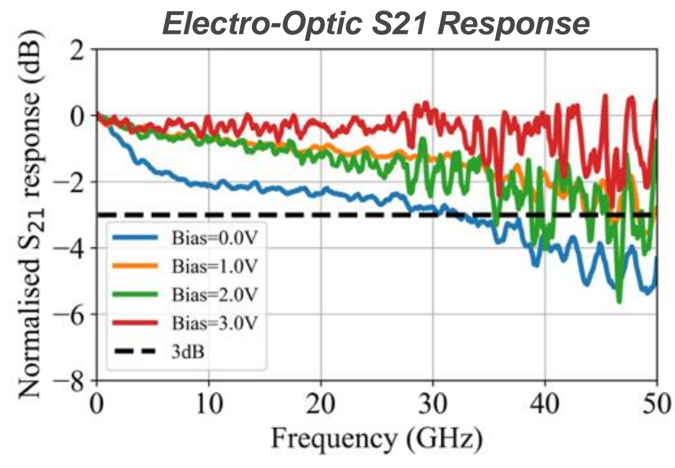
Defectivity < 500ppm (pre-packaging sorting)

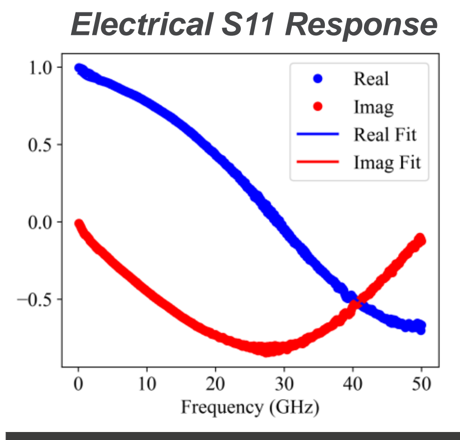
PUBLIC

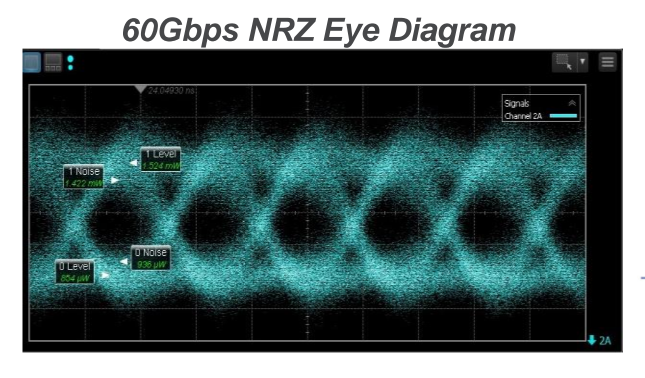
# O-band GeSi Electro-Absorption Modulator

*QCSE-EAM: High-Speed Performance*




*Drive swing = 2Vpp*
*ER ~ 2.5dB*

| Bias | 0V | -1V | -2V |
|---|---|---|---|
| Cj (fF) | 80 | 64 | 60 |
| Rs (Ohm) | 11.5 | 9 | 8 |
| iRC f3dB (GHz) | 173 | 276 | 331 |

- Modulation bandwidth $\mathbf{f_{3dB}}$**~50GHz** (from 50Ω)
- Capacitance $\mathbf{C_j}$**<80fF**, intrinsic RC bandwidth $\mathbf{f_{RC}}$**>>100GHz**

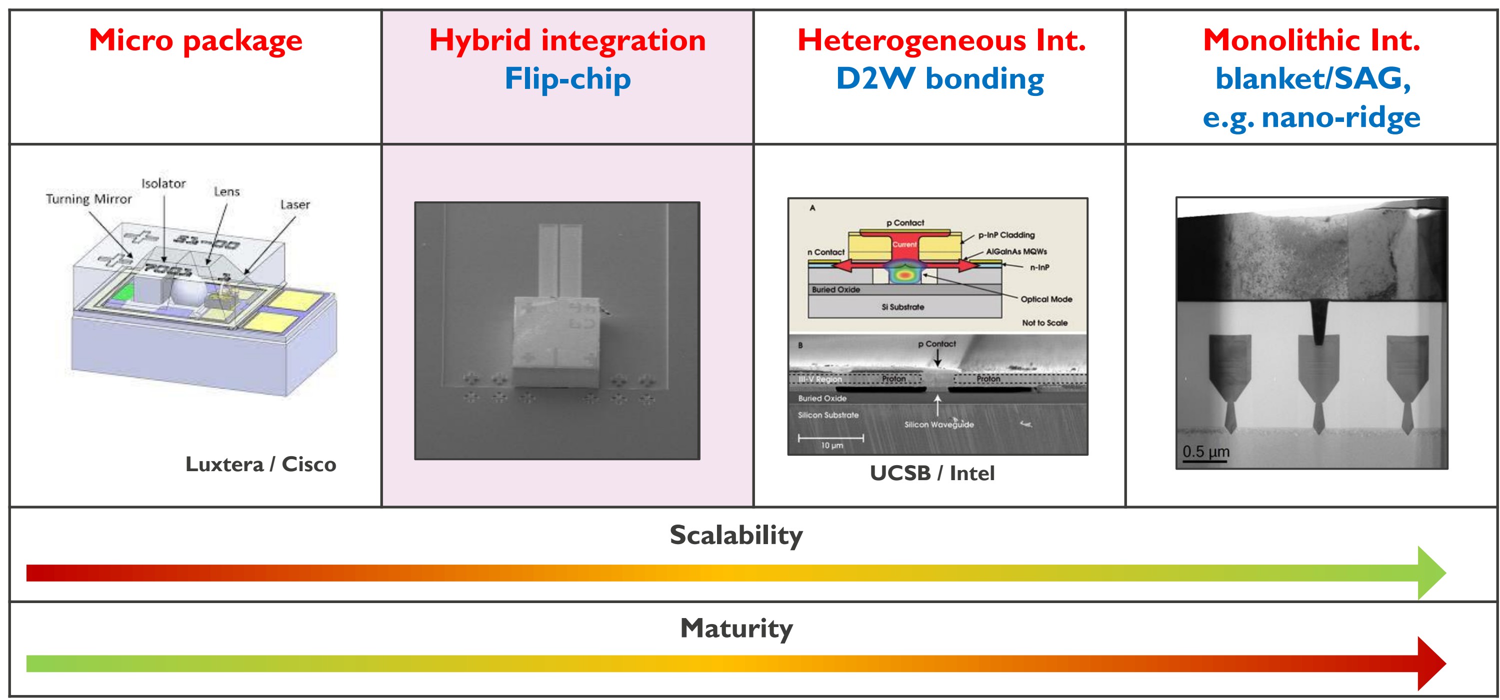
# Other Modulator Alternatives

- Graphene integration (and other 2Ds)
- III-V epitaxy (optically pumped devices + detectors, not yet lasers I assume)
- Alternative EO-materials
- BTO
- PZT

PUBLIC

# Laser Integration onto Silicon Photonics PIC

+ Various approaches in development or production
+ Imec short term plans: Flip-Chip Laser “Passive” Assemblies
+ Imec long term plans: Heterogeneous III-V layer transfer or Monolithic Integration

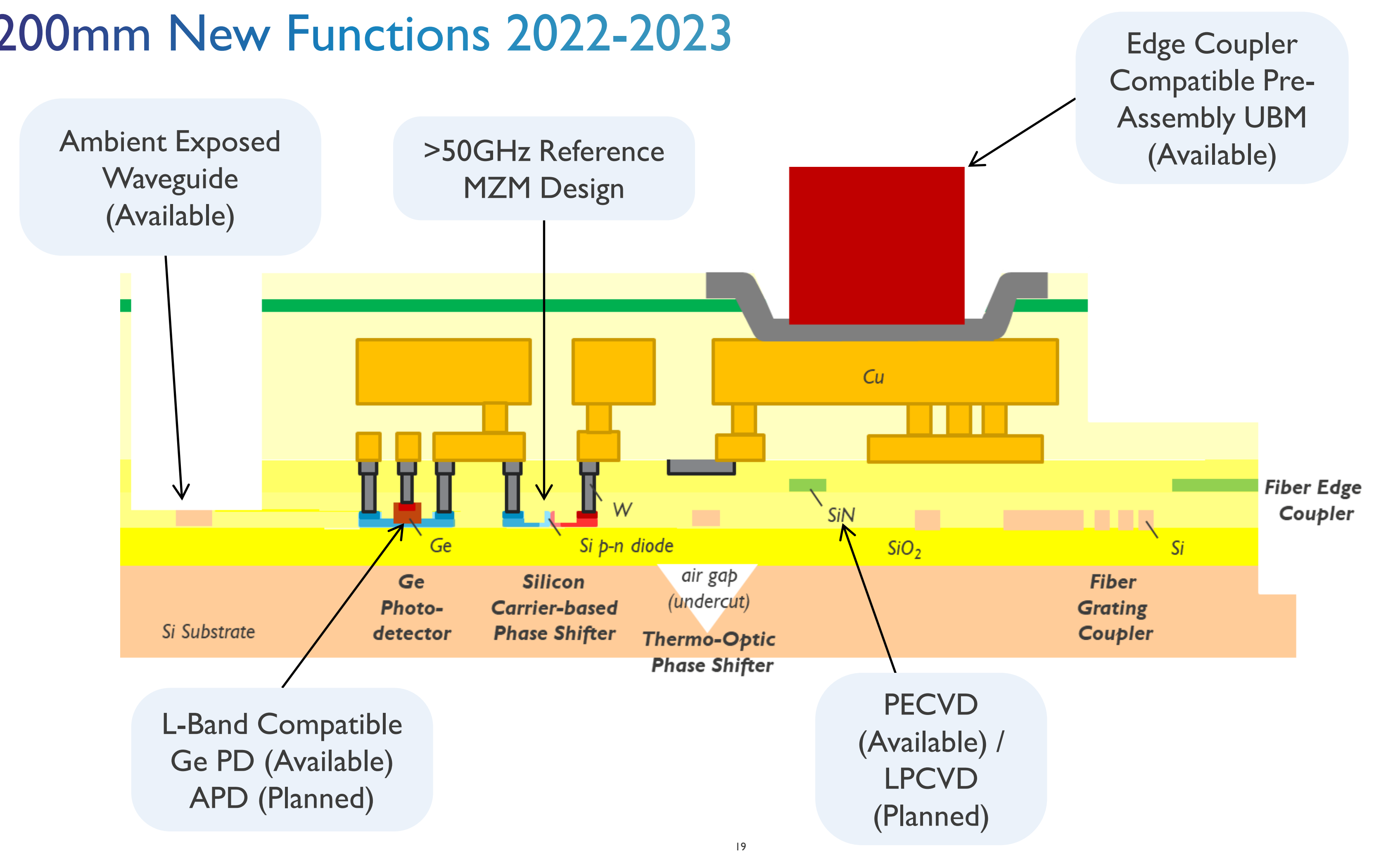





PUBLIC

# Imec Silicon Photonics Platform

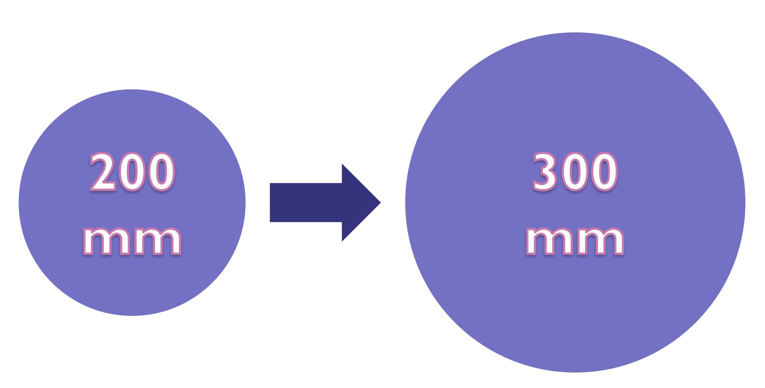
## Future Trends

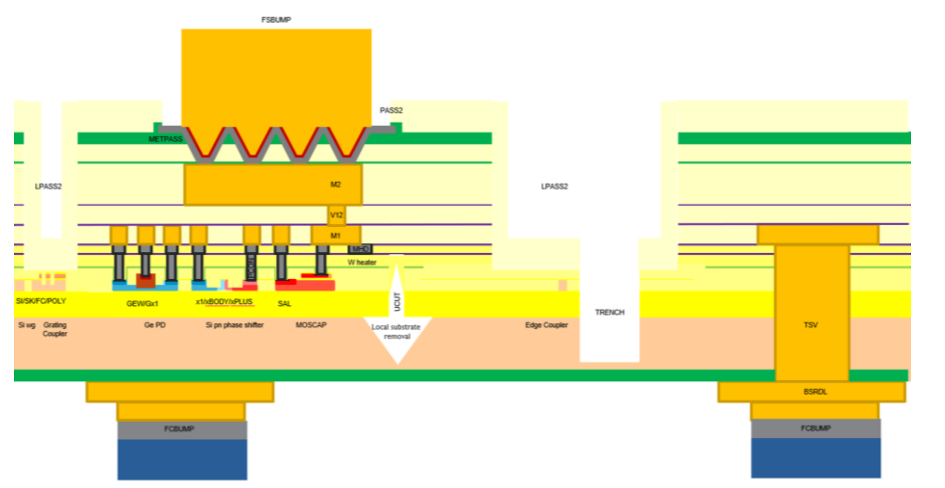





PUBLIC

# Upscaling to 300mm – Silicon Photonics Interposers For CPO




***300mm Key Differentiators***

- Sub-100nm Feature Size (193-***i*** litho)
- nm-scale Process Control
- 3D assemblies (TSV, μBumps, Hybrid bonding)

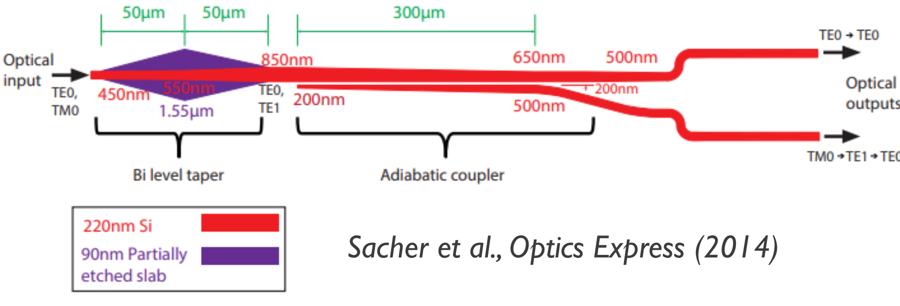


PUBLIC

# AI-Driven "Inverse" Design

## Example: Polarization Splitter

### *"Traditional" Design*



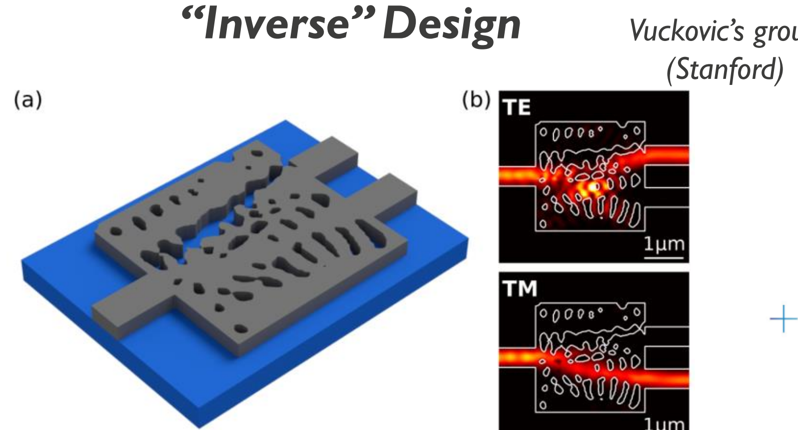

*Sacher et al., Optics Express (2014)*

Typical Minimum Line / Space ~150-200nm

Somewhat Regular Shapes

### *"Inverse" Design*

*Vuckovic's group (Stanford)*




Typical Minimum Line / Space **<100nm**

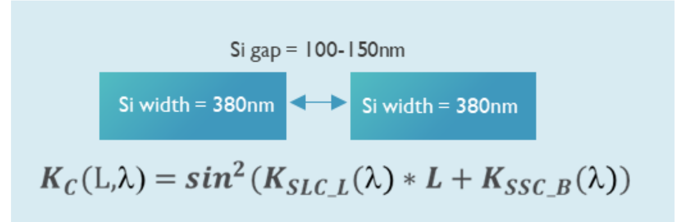
**Irregular** Shapes

*New patterning requirements !*



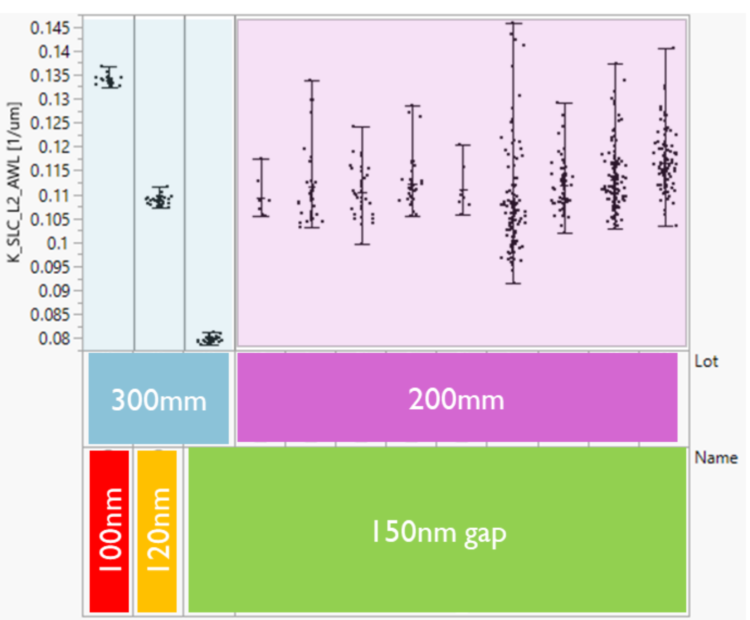
PUBLIC

# Waveguide Device Process Control




***Silicon Directional Coupler***

- 5-10x reduction in wafer variability
- Yielding 100nm Si gap

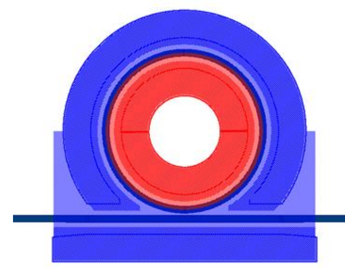


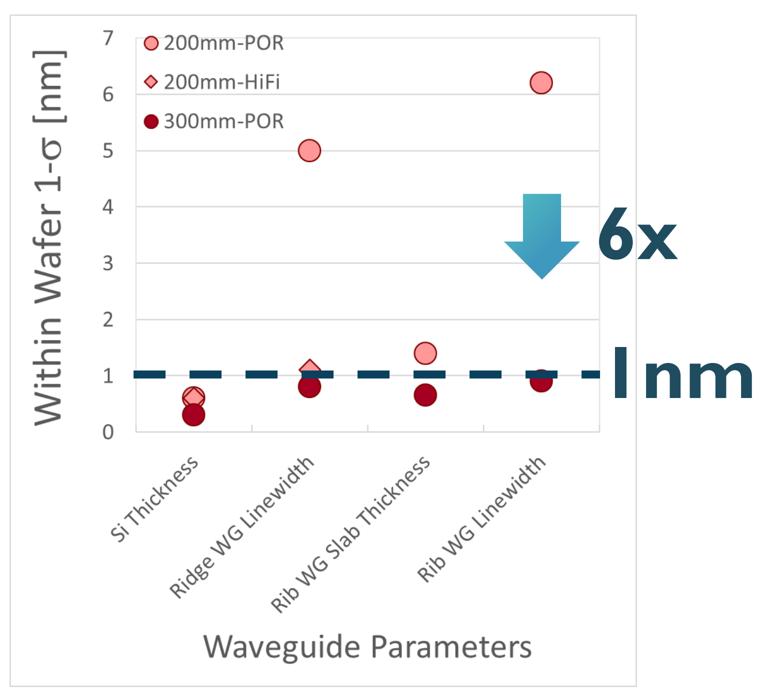

*Courtesy of Peter De Heyn*

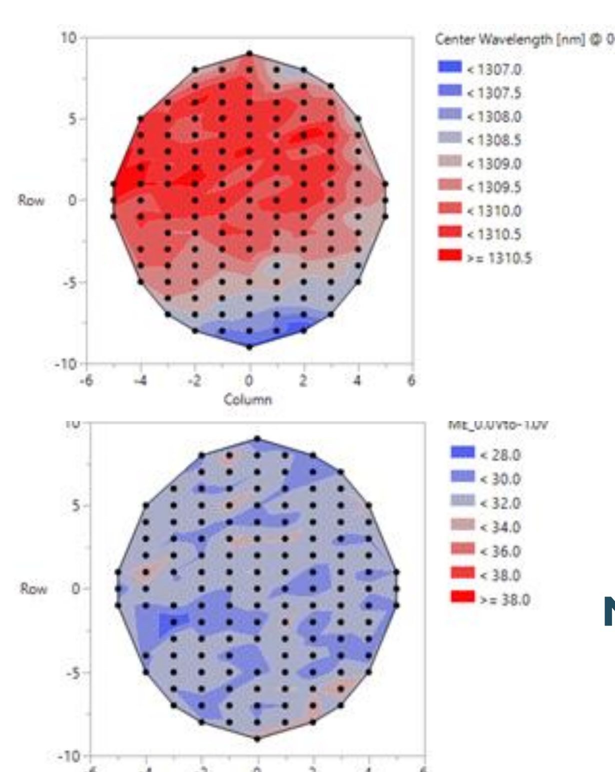


PUBLIC

# Waveguide Technology with Sub-nm Control – 300mm





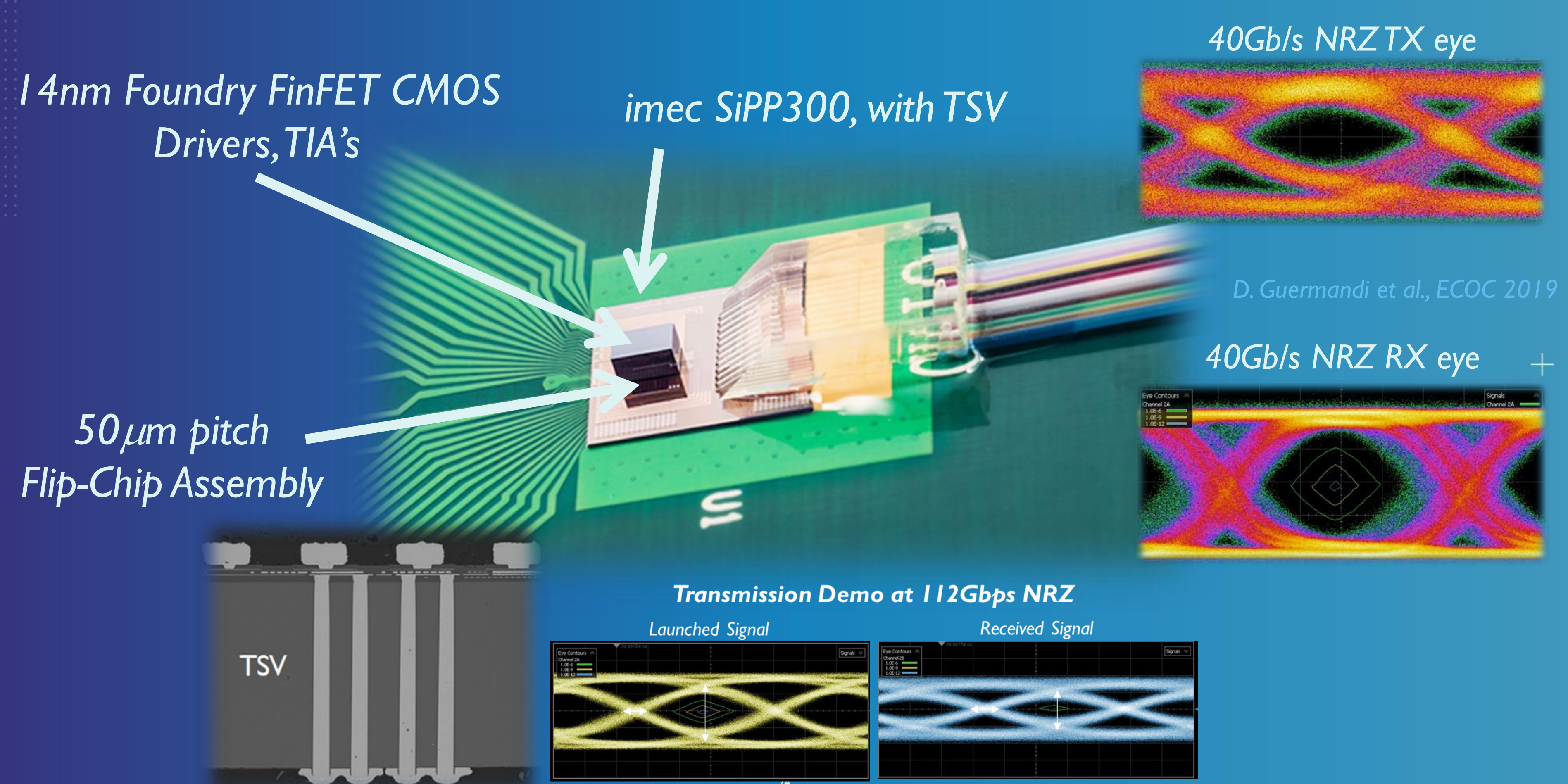

**Modulator $\lambda_{resonance}$**
**1-σ ~ 0.9 nm**

**Modulator Efficiency**
**1-σ ~ 1.4 pm/V**



PUBLIC

# 3D EIC-PIC: 40Gb/s TSV-Enabled Silicon Photonics



# Conclusions

Silicon Photonics is an industrial reality, in the critical path of Datacenters and AI scaling

Advanced CMOS Processing & Heterogeneous Integration will be necessary to address the (Si) photonics scaling challenges