EPIC Online Technology Meeting on Co-packaged Optics for Hyperscale Datacenters

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Fraunhofer IZM

Empowering Photonic Interconnects for Data Center and NGC

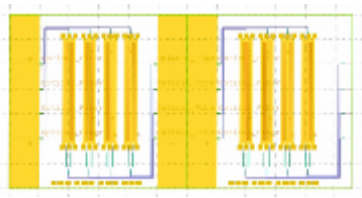
- System concept and design
- Photonic and RF component design
- Signal integrity and board design
- Silicon photonics interposer
- Through silicon via
- 3D integration
- Flip chip assembly
- Co-package
- System evaluation
- Benchmarking

480 Gb/s
12 ch. Tx/Rx

1.6 Tb/s
8x8 switching matrix

1.6 Tb/s
16-ch. WDM

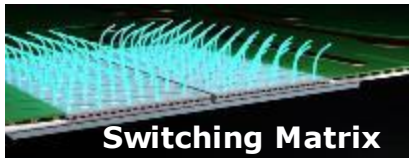
MASSTART



Transceivers for Tb/s inter and intra Data Centers applications

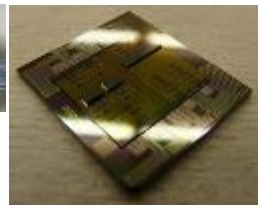
L3MATRIX
LARGE, LOW POWER AND LOW COST DATA CENTRES

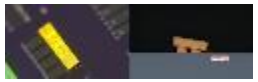
Co-Package Technology Platform



PhoxTroT

Optical Interconnections & 3D Integration Technologies





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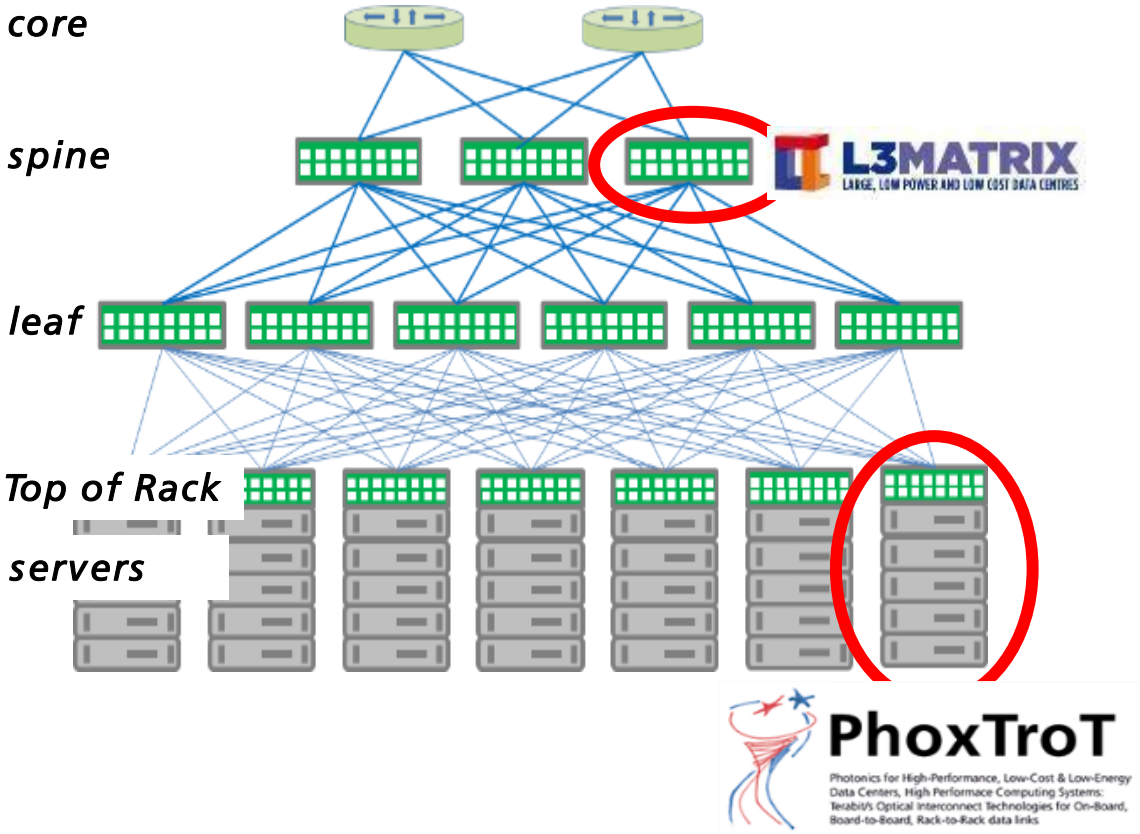
Data Center Network



- A server is connected to all other servers (full mesh topology)
- Servers are connected via the DC network composed from Ethernet switches
- The data center network is hierarchical – adding a new switch layer when running out of capacity
- Optical connectivity between switch hierarchies
- DC bandwidth demand grows exponentially, >70% traffic stays in the data center

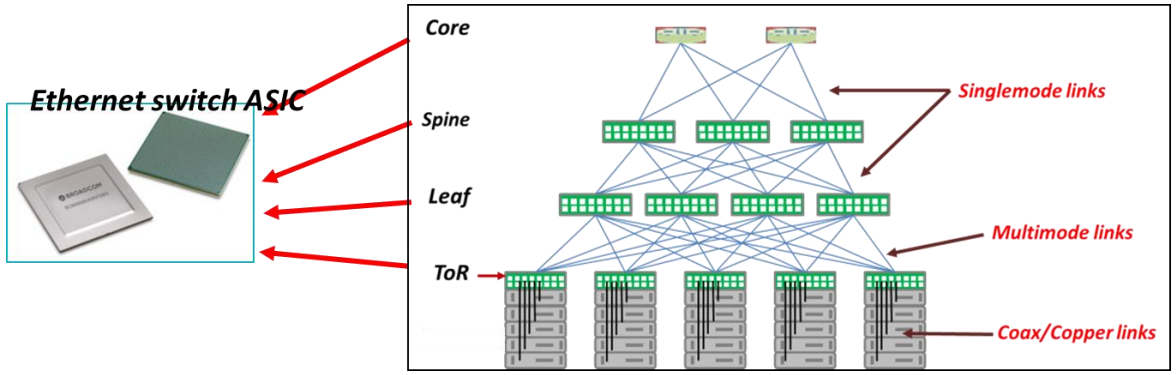
DC Network Topology - Limited Chip Radix

- A non-blocking Clos topology can be realized if:

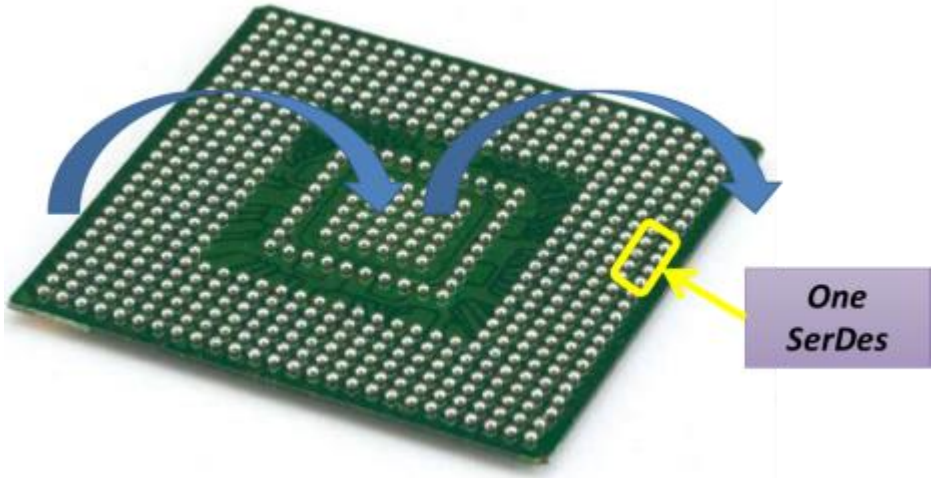
a) **The node has enough interfaces to connect to all switches**

b) **The switch has enough interfaces to connect to all nodes symmetrically**

- High Ethernet switch radix is an enabler for large scale data center networks



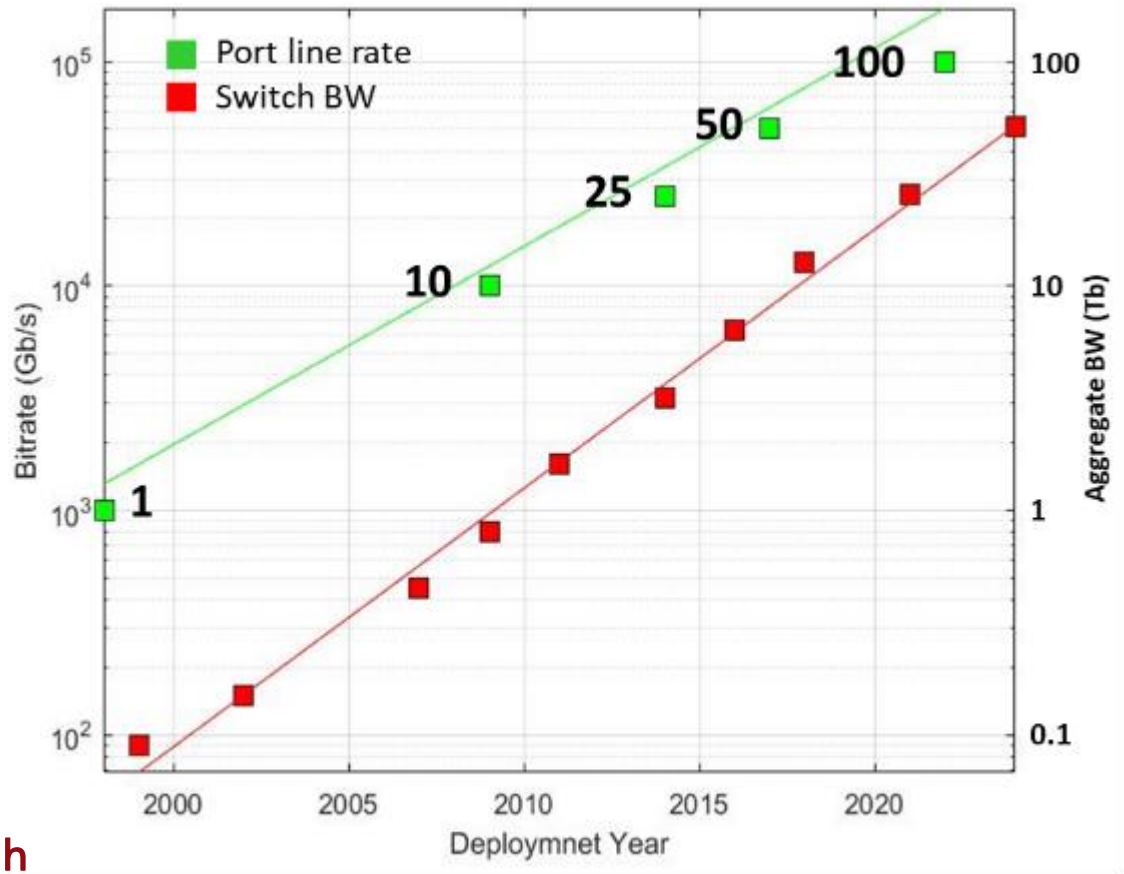
- The largest SerDes array are 256 elements
- BGA technology does not limit the array size
- The number is limited due to PCB routing constraints
- SerDes can be placed only on the chip perimeter



Data Center Network

The transceiver data rate follows
the ethernet switch port speed

Switch Bandwidth [Tb/s]	Chip Radix	SerDes speed [Gb/s]	Ports	Port Speed [Gb/s]
0.64	64	10	64	10
1.28	128	10	32	40
3.2	128	25	32	100
6.4	256	25	64	100
12.8	256	50	32	400
25.6	256	100	64	400
51.2	512	100	64	800



Adapted from A. Ghiasi Opt. Exp. 2015

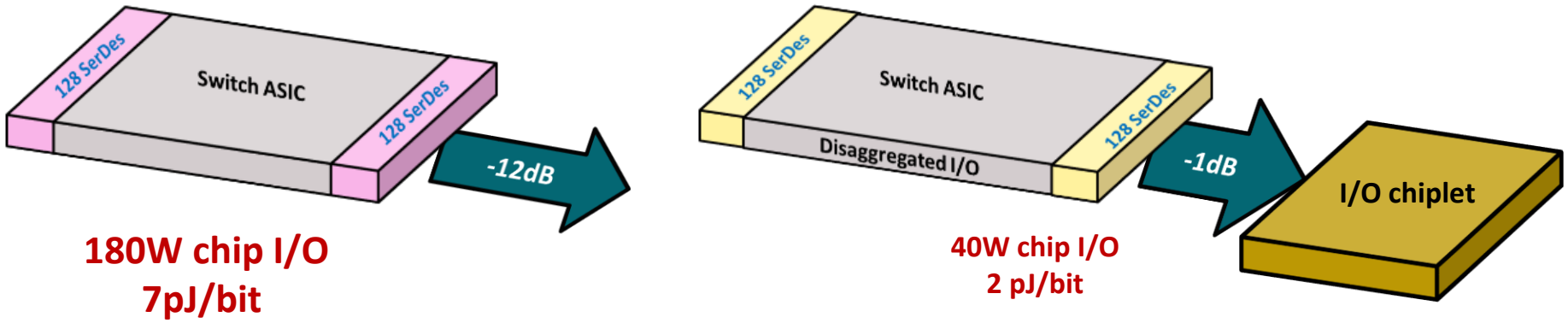
However, SerDes power consumption increases with bitrate

Cost Considerations

- Optical transceiver cost is a key limitation to data center scaling
  - Target cost for SM transceivers is $1/G
  - Given 32 ports on the switch front panel, the optics cost is $10-13k
  - About $50M per data center….

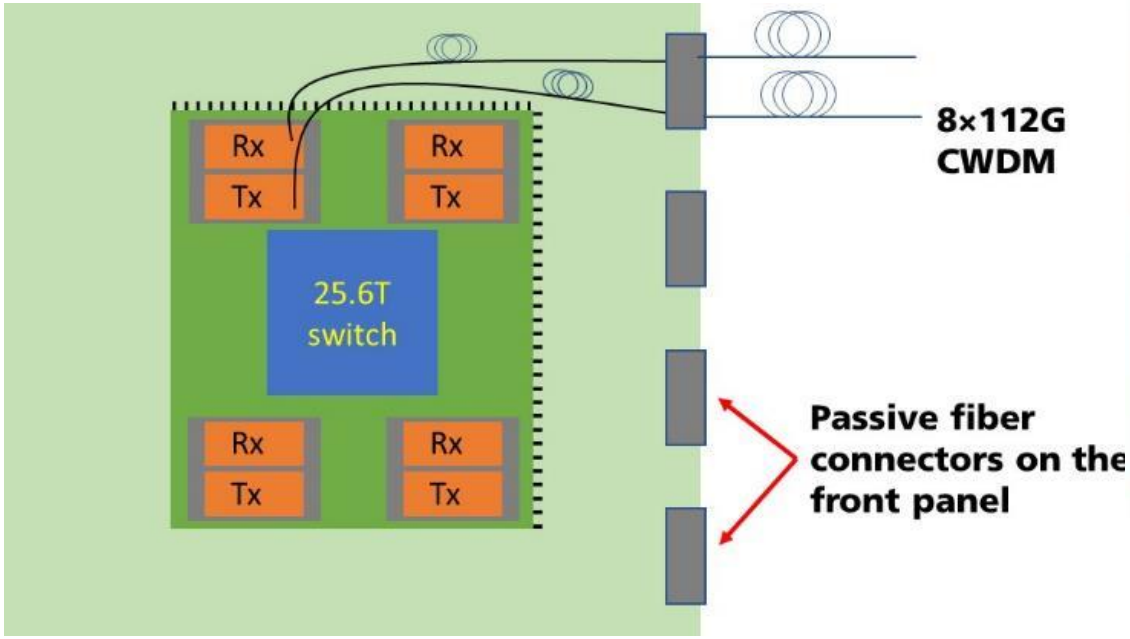
Decoupling Logic and I/O

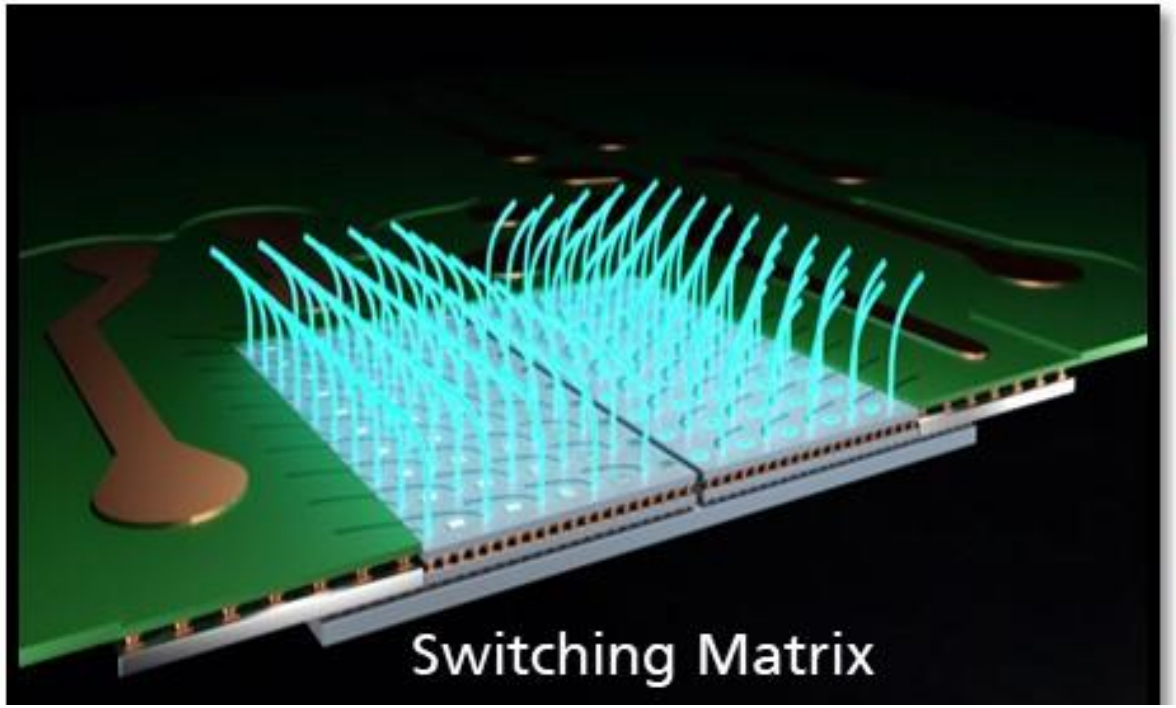
- Reduces power consumption by decoupling I/O from the switch ASIC
- Chip I/O is handled by several chiplets located <10mm from the switch on a common package
- The SerDes reach drops from MR/LR to USR; power consumption drops significantly
- No need for a retimer for the USR link
- The SerDes array size can be doubled (for 51T devices); routing is within the package with dense L/S
- Use an optical interface on the I/O chiplet to further reduce the power consumption



Co-Package of Photonics with Digital CMOS

- The switch ASIC and 2-4 ‘optical I/O ASICs’ are co-packaged on a single MCM/interposer
- Fiber bundles connect the module and the front panel passive fiber connectors

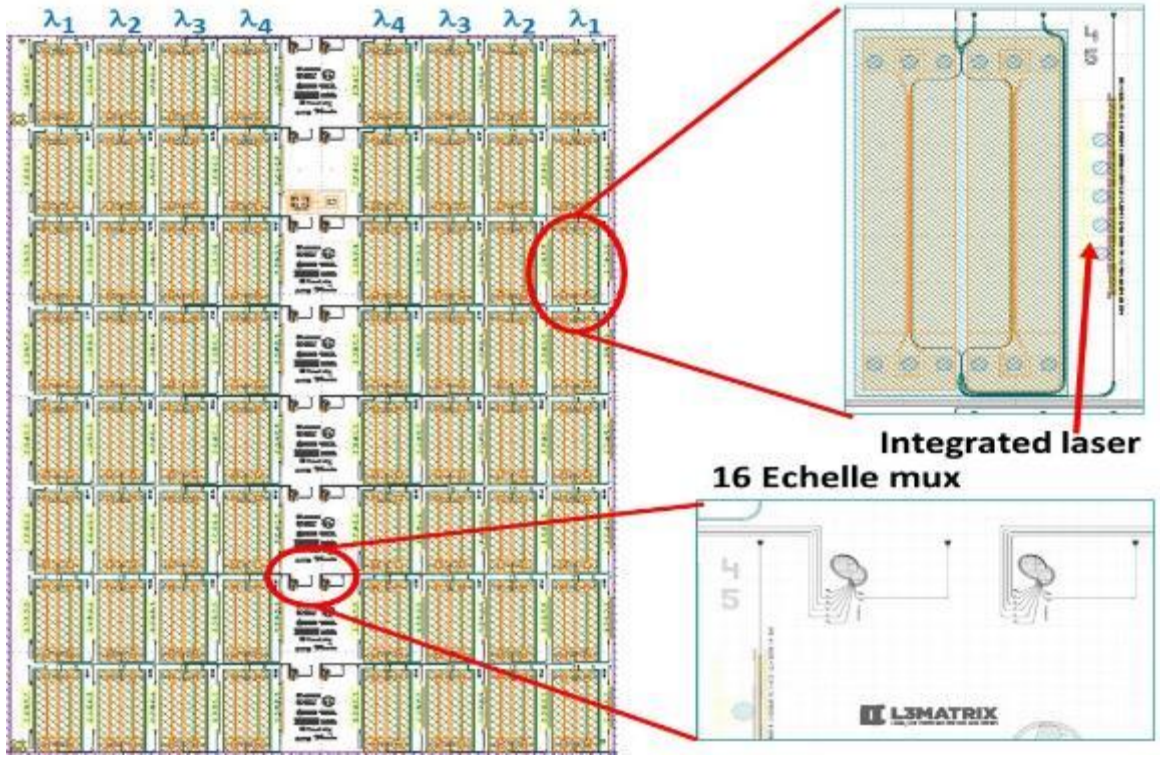


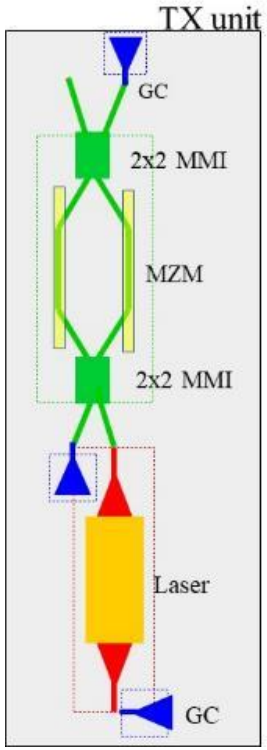


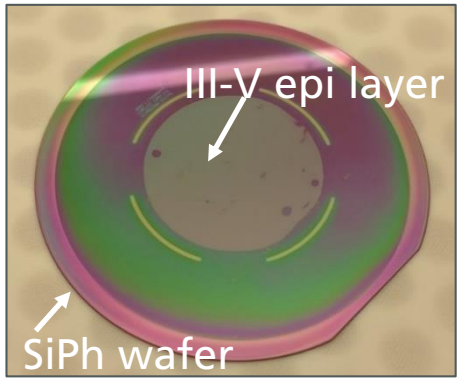
L3MATRIX : Co-Package of Photonics with Digital CMOS

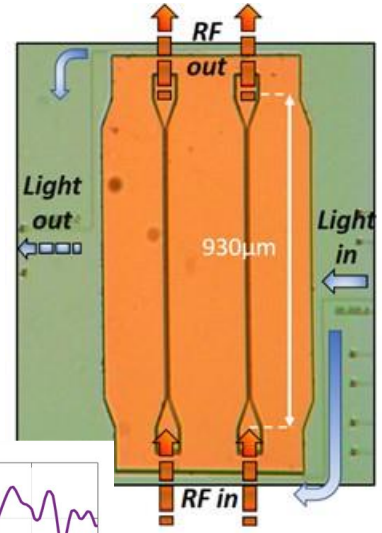
L3MATRIX - Large Scale Silicon Photonics Matrix for Low Power and Low Cost Data Centers

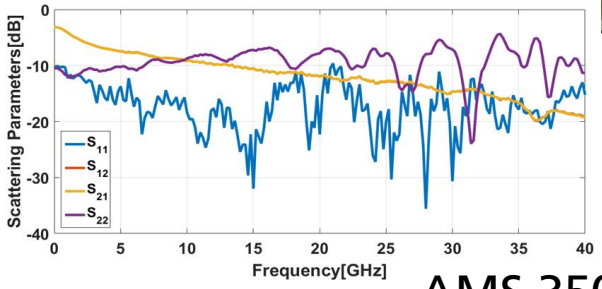
- Underlying network technology must improve in areas such as **photonic switching**, enabling scale *performance whilst keeping power* consumption in control.





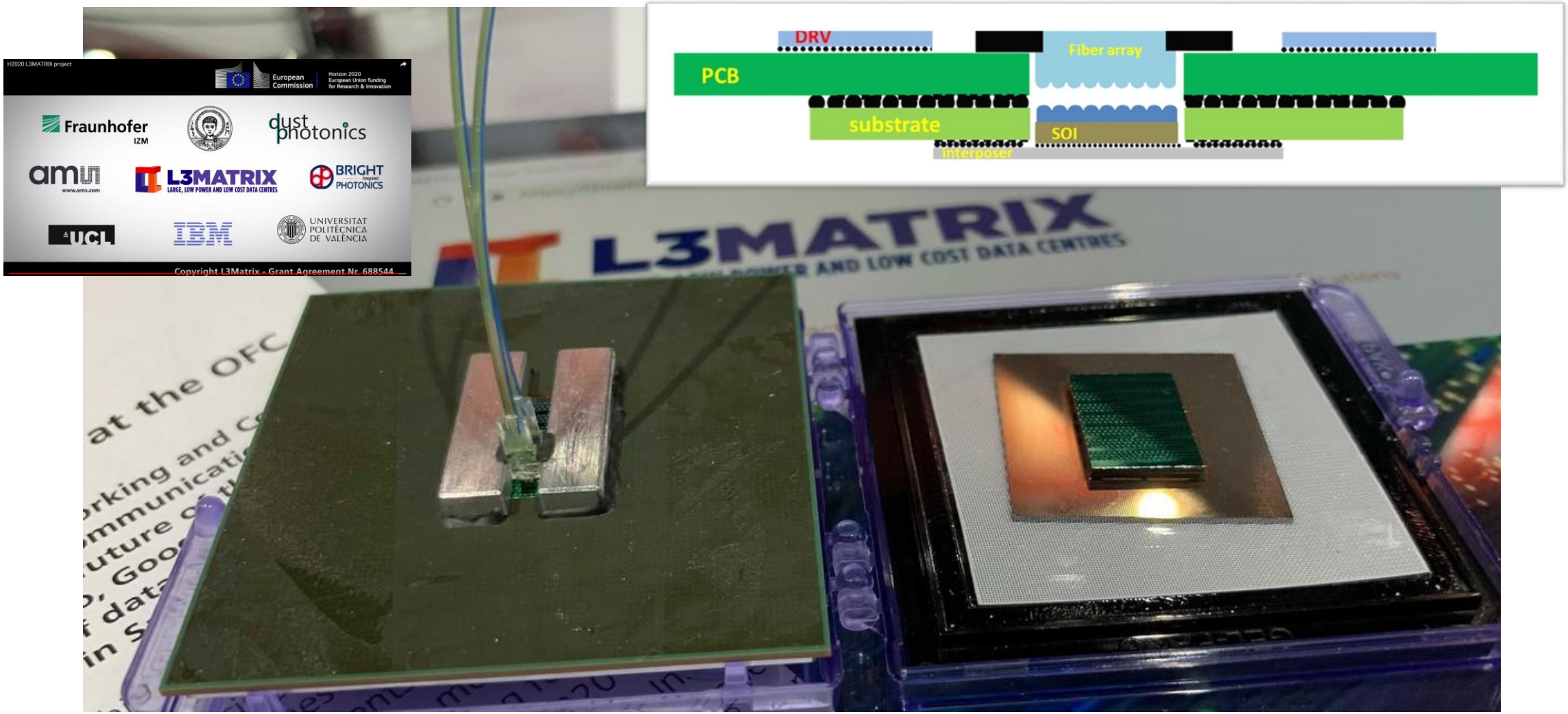






AMS 350nm CMOS

Large Scale Silicon Photonics Matrix for Low Power and Low Cost Data Centers



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PhoxTroT project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement no 318240 www.photrot.eu

MASSTART project is co-funded by the Horizon 2020 Framework Programme of the European Union with Grant Agreement Nr. 825109. https://cordis.europa.eu/project/rcn/219912/factsheet/en