EPIC World Photonics Technology Summit, January 24th, 2022

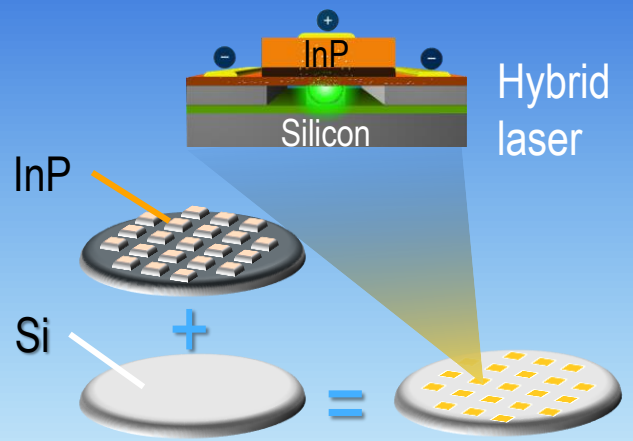
High Volume Silicon Photonics for Optical I/O and other Next Generation Applications

Robert Blum – robert.blum@intel.com

Intel Corporation

Intel Silicon Photonics: Optics at Silicon Scale

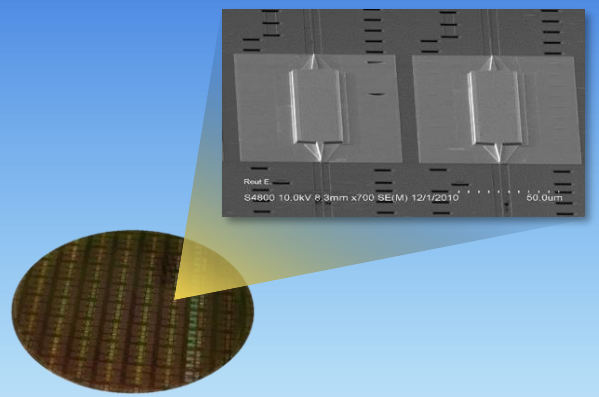
Silicon Integration



Integrated Optics, Enabled by Intel's Hybrid Laser Technology

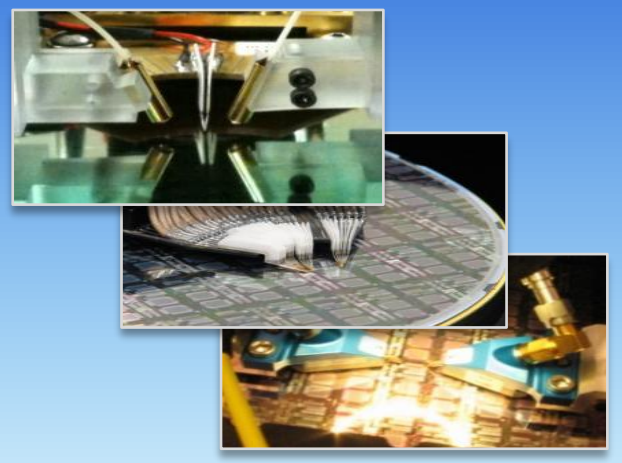
InP for lasers, SOAs, PDs

Silicon Manufacturing



Advanced CMOS Mfg Process at Intel Fabs On 300mm Wafers

Silicon Scale



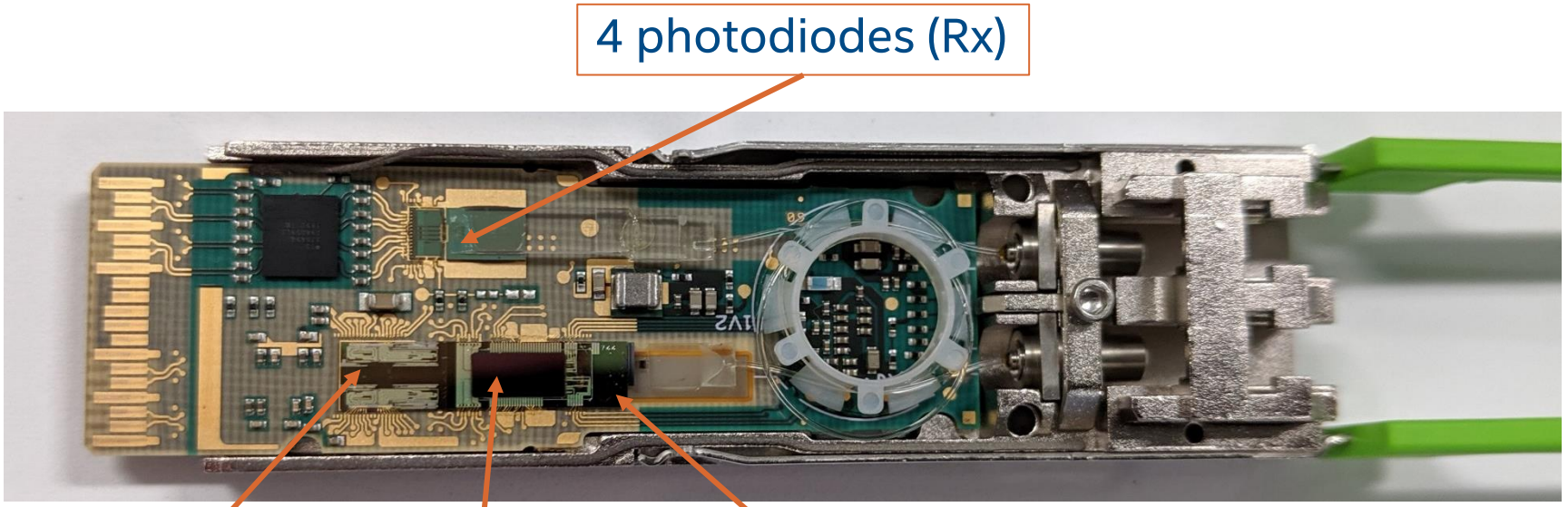
Automated On-wafer Optical, Electrical, and High-speed Test

Wafer-level burn-in

Wafer-scale manufacturing of optical sub-assembly; known good die at wafer level

Silicon Photonics High Volume Transceivers

100G CWDM4 with No Hermetic Packaging, 5M+ units shipped



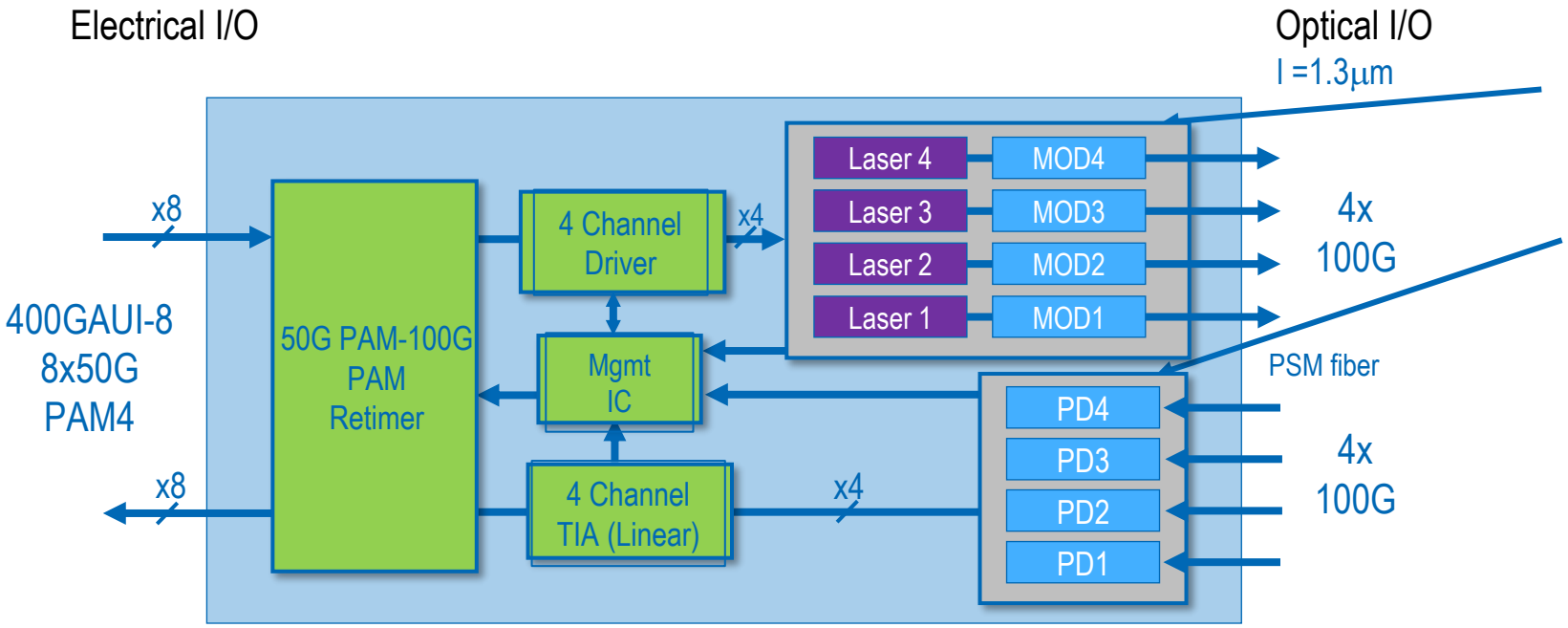
- Transmitter chip integrates 4 lasers, 4 modulators, optical multiplexer, and related monitor/control functions on a single die
- Receive path is a separate chip with 4 high speed photodiodes
- Data center operation or industrial temperature range (-40°C to 85°C)
- Industry-leading reliability and quality: ~2 FIT for laser; ~30dppm for module

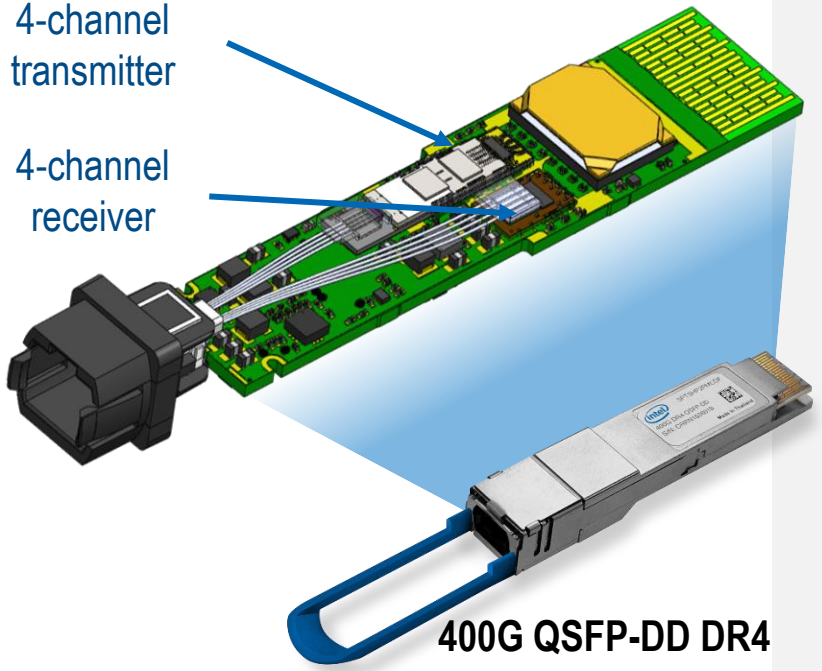
200G and 400G optics also in production and shipping in volume now; 800G sampling

Robert Blum, "Integrated silicon photonics for high-volume data center applications," Proc. SPIE 11286, Optical Interconnects XX (Photonics West 2020)

400G DR4 Silicon Photonics Optical Transceiver

- 400G Ethernet connectivity for 12.8T Ethernet switches
- Standards-compliant optical interface with extended 2km reach for 400G or 4x100G breakout
- In volume production to support hyperscale data centers

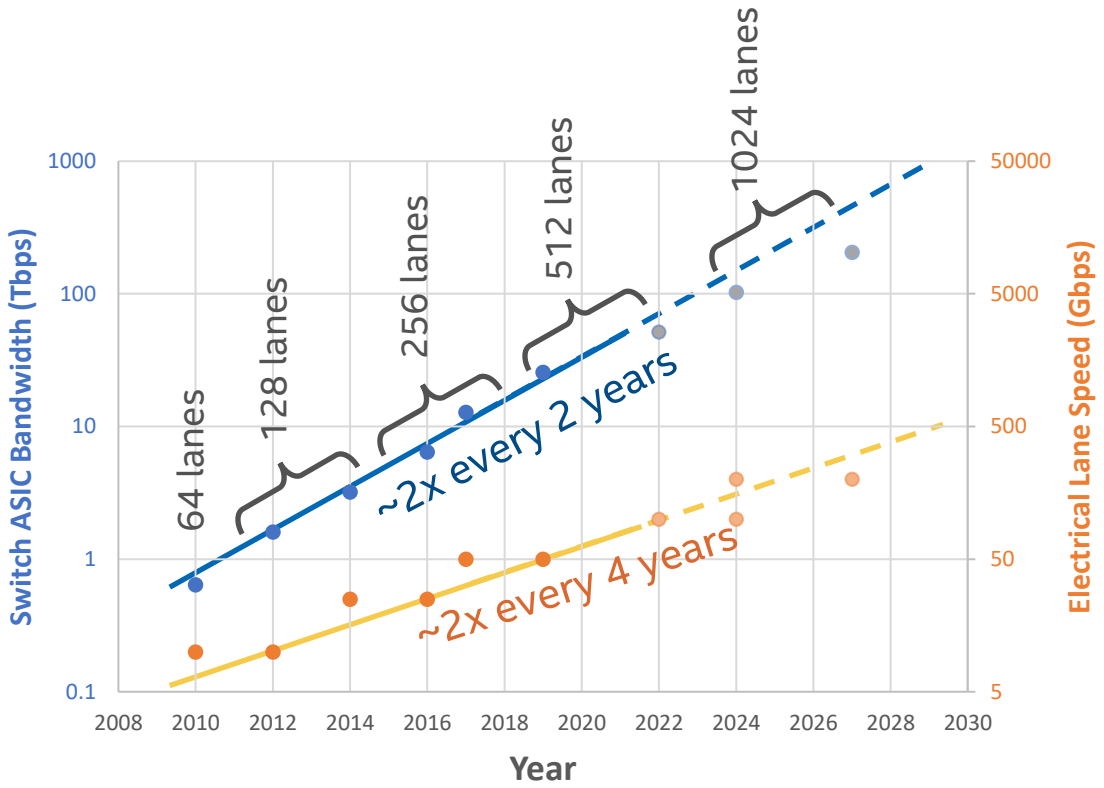




Datacenter Network Bandwidth Scaling

Fundamental challenge: I/O vs. switch scaling

- Switch: 2x bandwidth **every ~2 years**
  - Power efficiency with process node
- I/O: 2x data rate **every 3-4 years**
  - Diminishing returns in power efficiency
- Increasing share of switch ASIC power consumed by I/O
- Increasing share of link power consumed by first and last 12”
  - 40% at 100G lanes
- Increasing packaging and signal integrity complexity ($)



Directional, based on Intel estimates

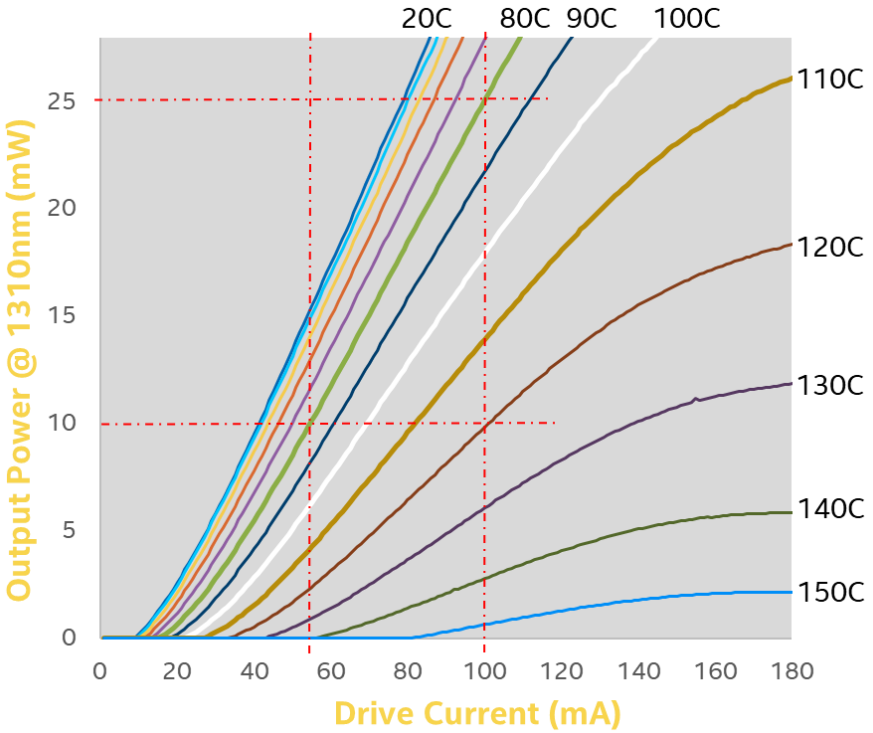
DFB Laser Performance

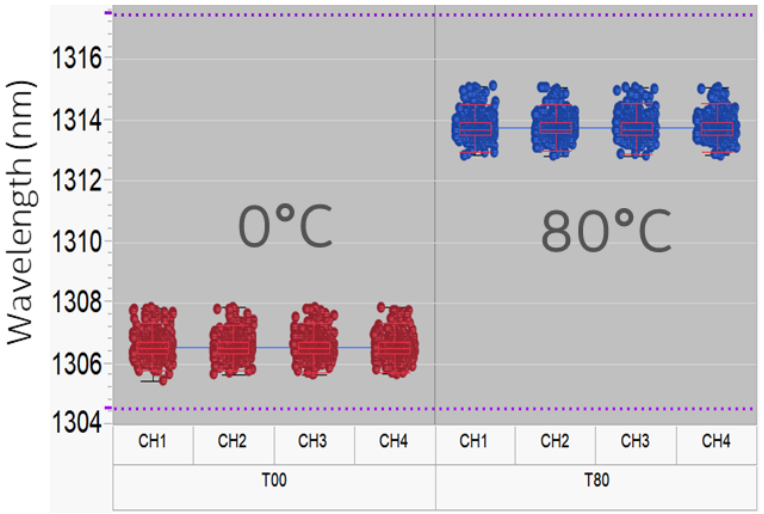
Excellent performance over temperature

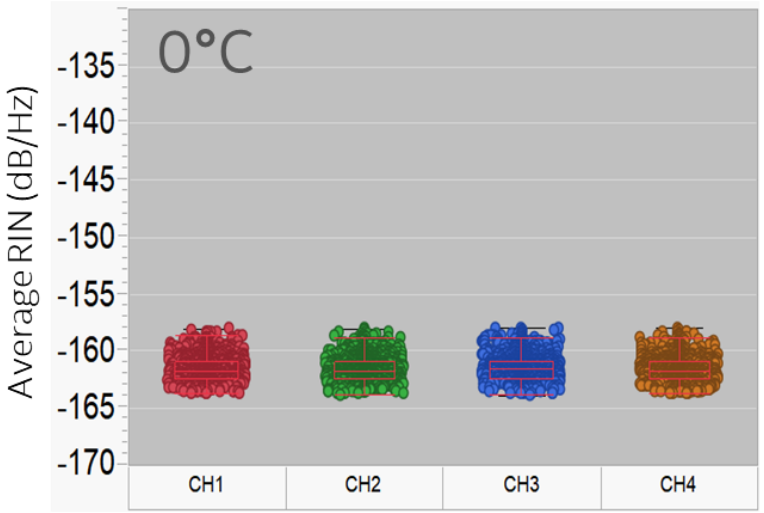
- Laser emission up to 150C
- 10mW at 80C for 60mA; 25mW at 80C for 100mA

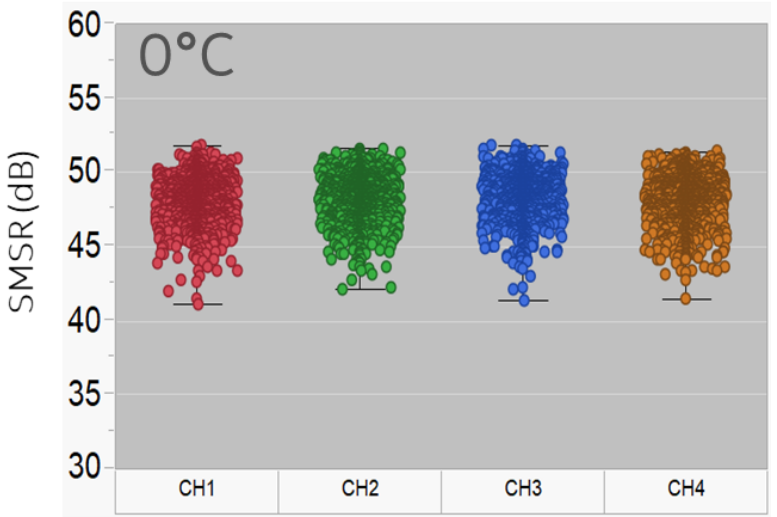
Uncooled operation enabled by tight process control on 300mm wafer

- Low relative intensity noise (RIN) < -155 dB / Hz
- High side-mode suppression ratio (SMSR) > 40dB



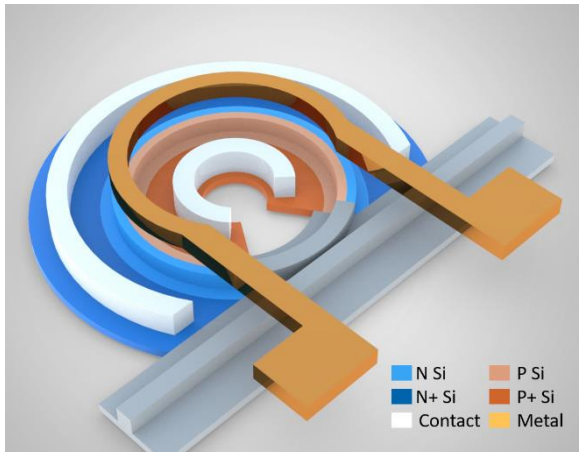


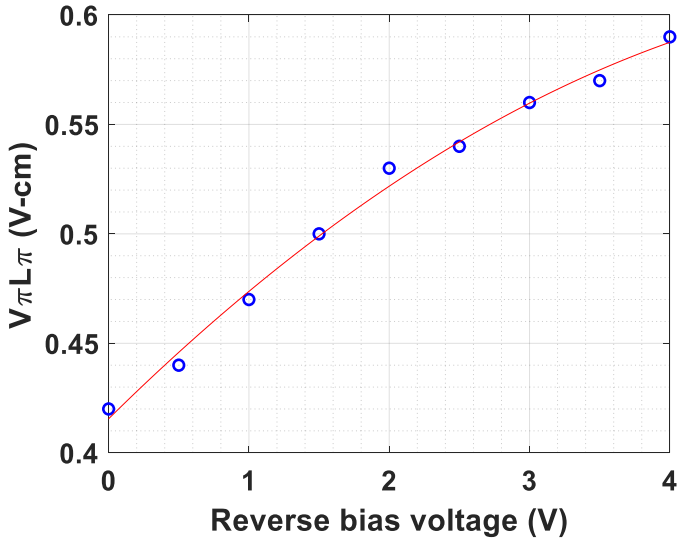


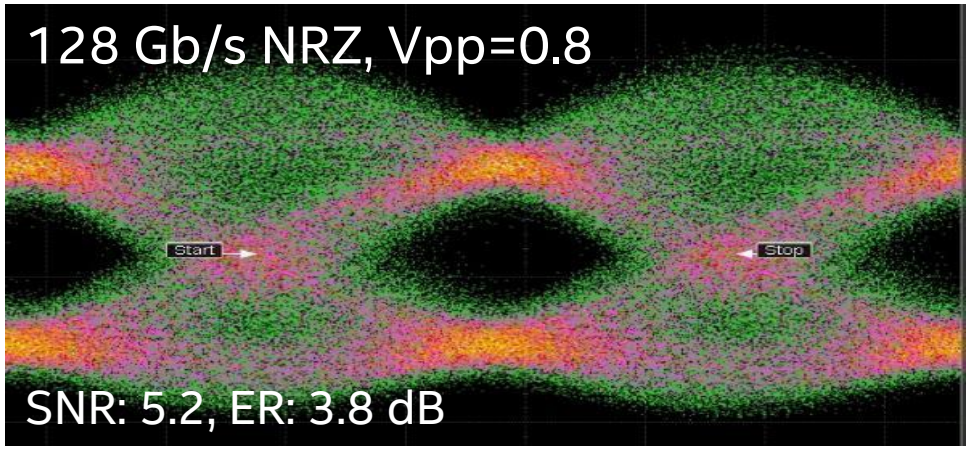


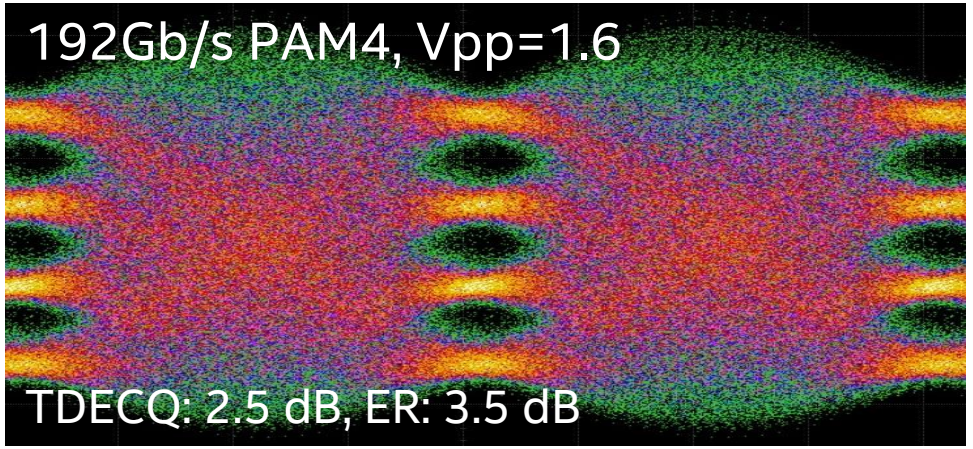
Source: P. Doussiere, "Laser integration on silicon," GROUP IV PHOTONICS, 2017
H. Yu, "400Gbps Fully Integrated DR4 Silicon Photonics Transmitter for Data Center Applications," OFC, 2020

High-speed 6-mm Micro-Ring Modulator









- ✓ **128Gb/s NRZ** is the highest data rate ever demonstrated in the industry using a ring modulator
- ✓ 8x128Gb/s = **1024Gb/s**

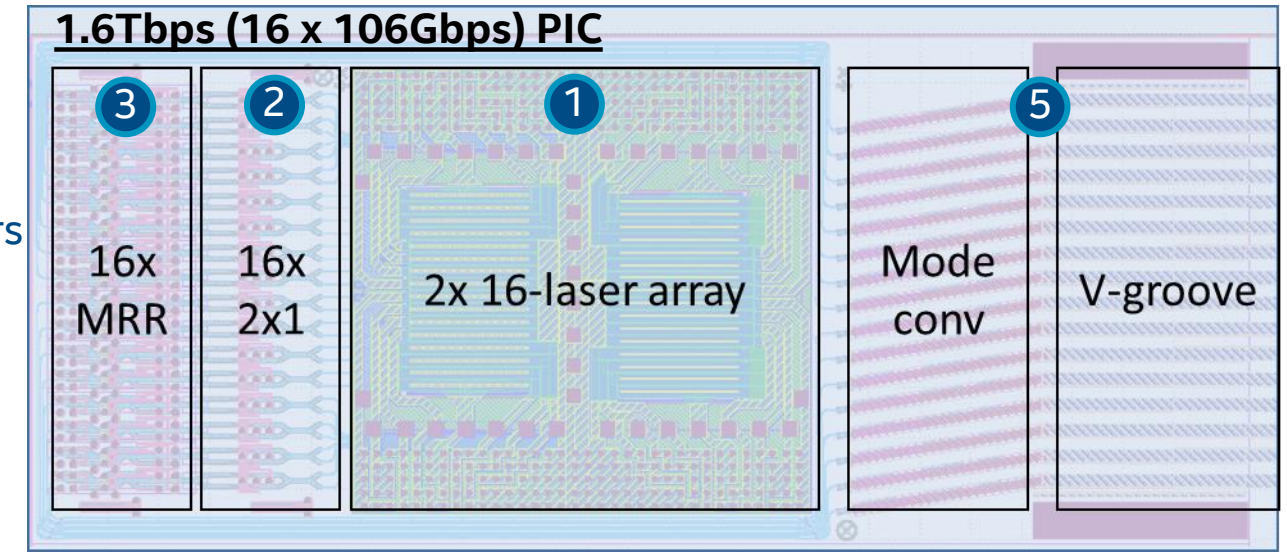
Meer Sakib et al., "260 Gb/s/λ PDM Link with Silicon Photonic Dual-Polarization Transmitter and Polarization Demultiplexer", Tu4D.1, ECOC 2021

Silicon Photonic Integrated Circuit

Integrate all Photonic Components On-Chip to Scale BW-Density & Cost

2 Laser selector switches, x16
- 2x1 MZI
- Integrated heaters

1 Lasers, x32
- Intel's hybrid-laser technology
- Full redundancy for low system FIT



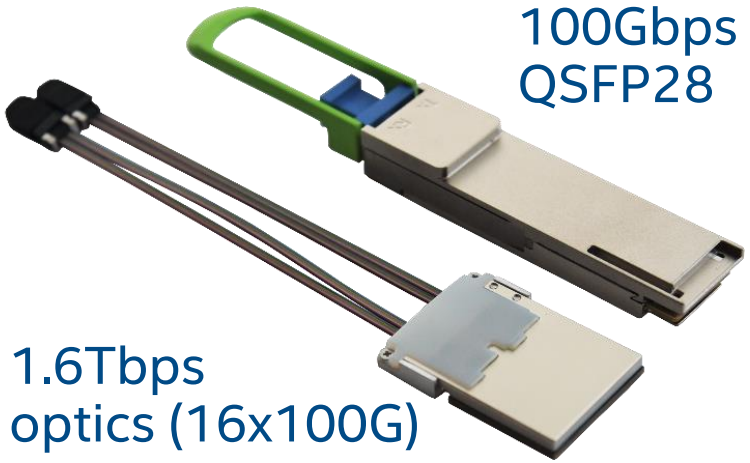
3 Si modulators, x16
- Micro-ring resonators
- Integrated heaters
- 106 Gbps PAM4

5 Passive fiber array alignment
- 10μm mode converters, x16
- Integrated V-Grooves, x16

4 Power monitor photodetectors, x48
- Germanium diodes
- 106 Gbps PAM4 capable

>30cm of WG routing
>600 active bumped pads
4x Temperature sensors

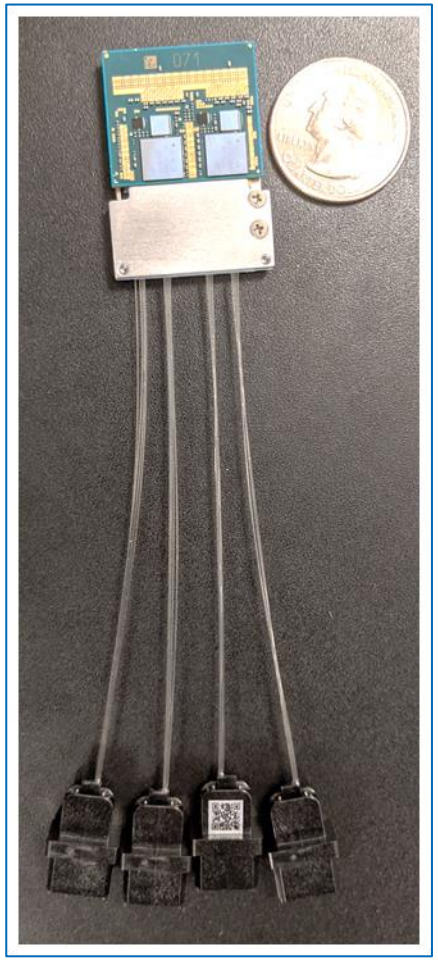
Co-packaged optics tile



40x bandwidth density

>30% energy efficiency improvement

Another >2x density and 15% efficiency improvement projected with 3.2T CPO module product

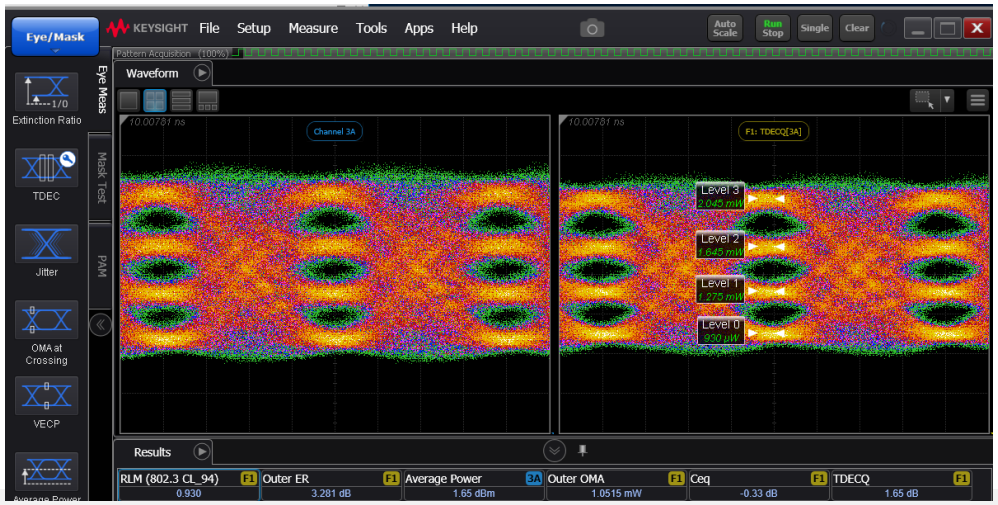


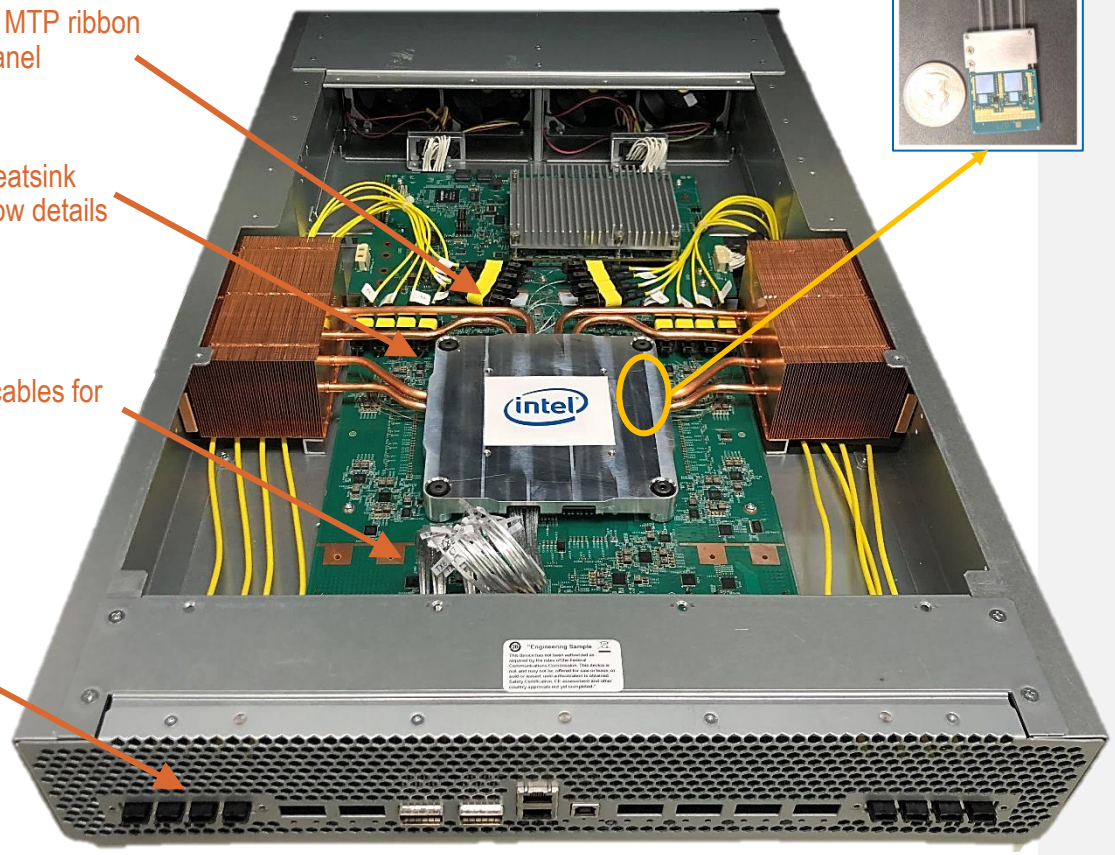
- Active development towards **product intercept with 3.2T tile for 51.2T** – parallel and WDM optics in standards-compliant CPO module
- **Hybrid integration** 2.5D package of PIC and EIC
  - Optimized and on different cadence
- High-speed, high-density **LGA socket** on bottom – compatible with XSR channel
  - Yield and testability ("Known Good Tile")
- **Passive alignment** enabled by mode converters and V-grooves

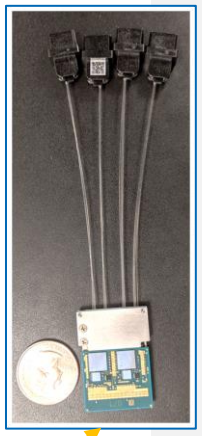
Ling Liao, "Silicon Photonics Co-Packaged Switch", Hot Interconnect 2020
Ken Brown, "Packaging Technology for coming generations of Silicon Photonics", Semicon Taiwan 2020

March 2020 Demonstration of Industry-First Co-Packaged Optics Ethernet Switch

- Barefoot Tofino 2 12.8T P4-programmable Ethernet switch
- Co-packaged with integrated photonic engines
  - 16x lasers coupled to 16x 106 Gbps PAM4 ring modulators = 1.6Tbps aggregate bandwidth
- Live 400G Ethernet traffic enabled by fully functional switch platform with co-packaged optics ports in single switch package

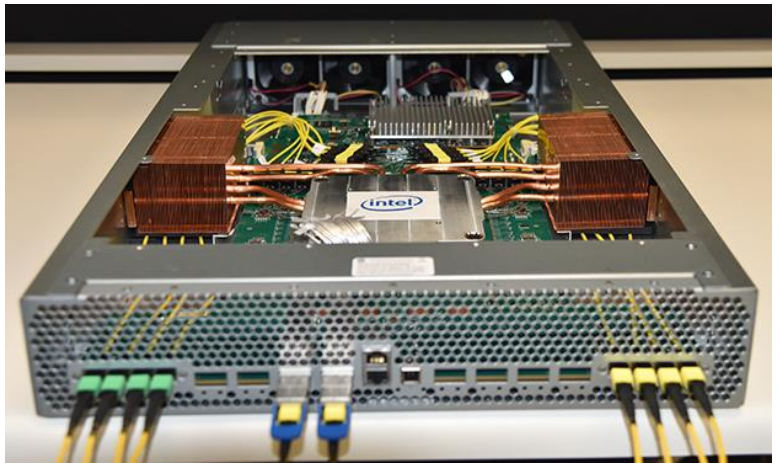






Co-packaged optics

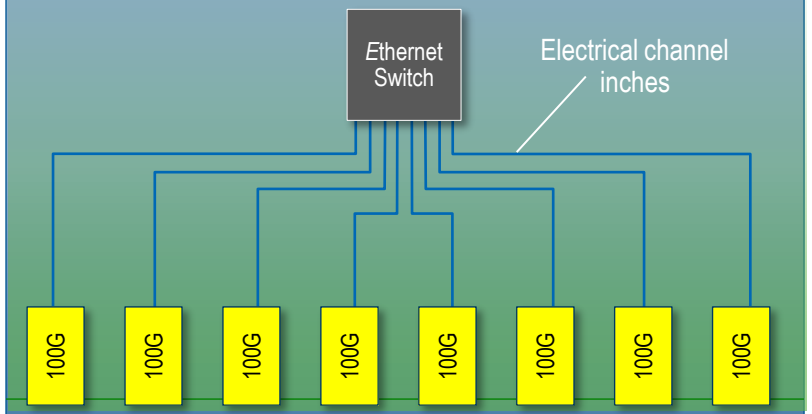
- Growth in bandwidth requirements is not slowing down – but power trajectory is unsustainable
  - Closer integration of optics to ASIC reduces system I/O power, while supporting continued scaling
- Scaling to 51Tbps switches under development;
  - Air-cooling @ >1kW challenging, but feasible
  - Power rail noise will likely be the biggest PDN challenge
  - Multi-vendor eco-system possible, but timeline is tight
- Broad adoption at 100T as enabling technology for scalability
  - With 200G I/O and 200G/λ
- Development of healthy eco-system around open standards is critical to support commercialization
  - Agreement on test points and performance targets
- Beyond switches: Co-packaged optics will be the enabling technology for bandwidth scaling across a broad range of SoCs



Silicon Photonics Enables Path to Performance Scaling

HVM Today: 100-800G Pluggable

Front plate pluggable optics
Ethernet Compliant

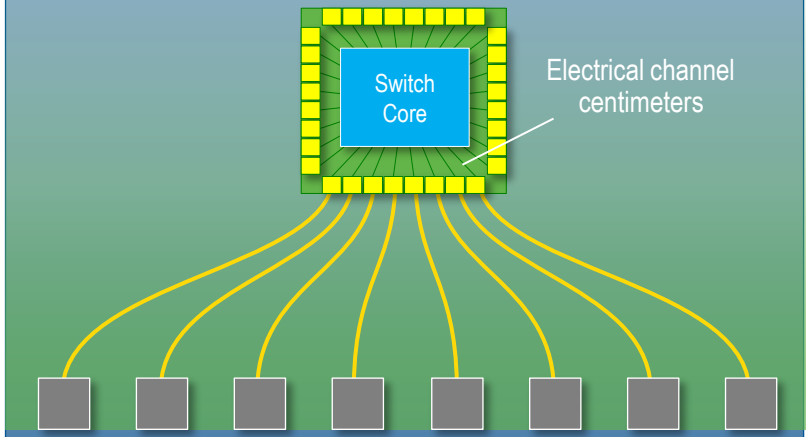


- Total data rate: 100 – 800 Gbps
- BW/shoreline: 5-40 Gbps/mm
- Energy efficiency: 30 pJ/bit

- Multiple discrete PICs and EICs
- Pluggable form factor

2020 Demo: CPO w/ Switch

Co-packaged optics
Ethernet Compliant

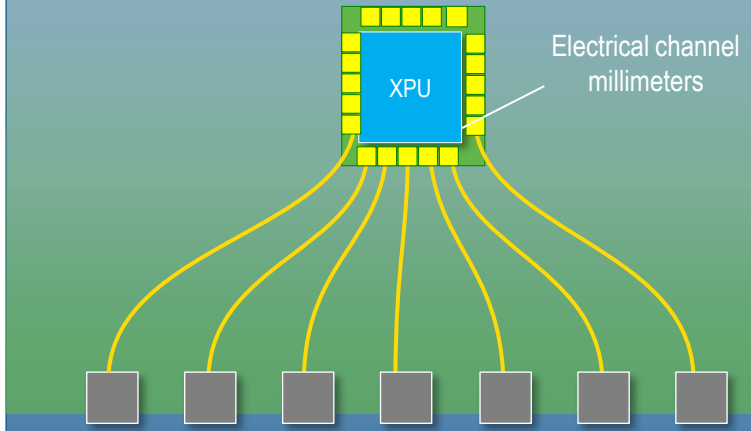


- Total data rate: 1.6- 6.4 Tbps
- BW/shoreline: 50-200 Gbps/mm
- Energy efficiency: <15 pJ/bit

- Fully integrated PIC
- 3D MCP to drive density

Future: Optical I/O

XPU optical I/O
Optimized Optical Interface



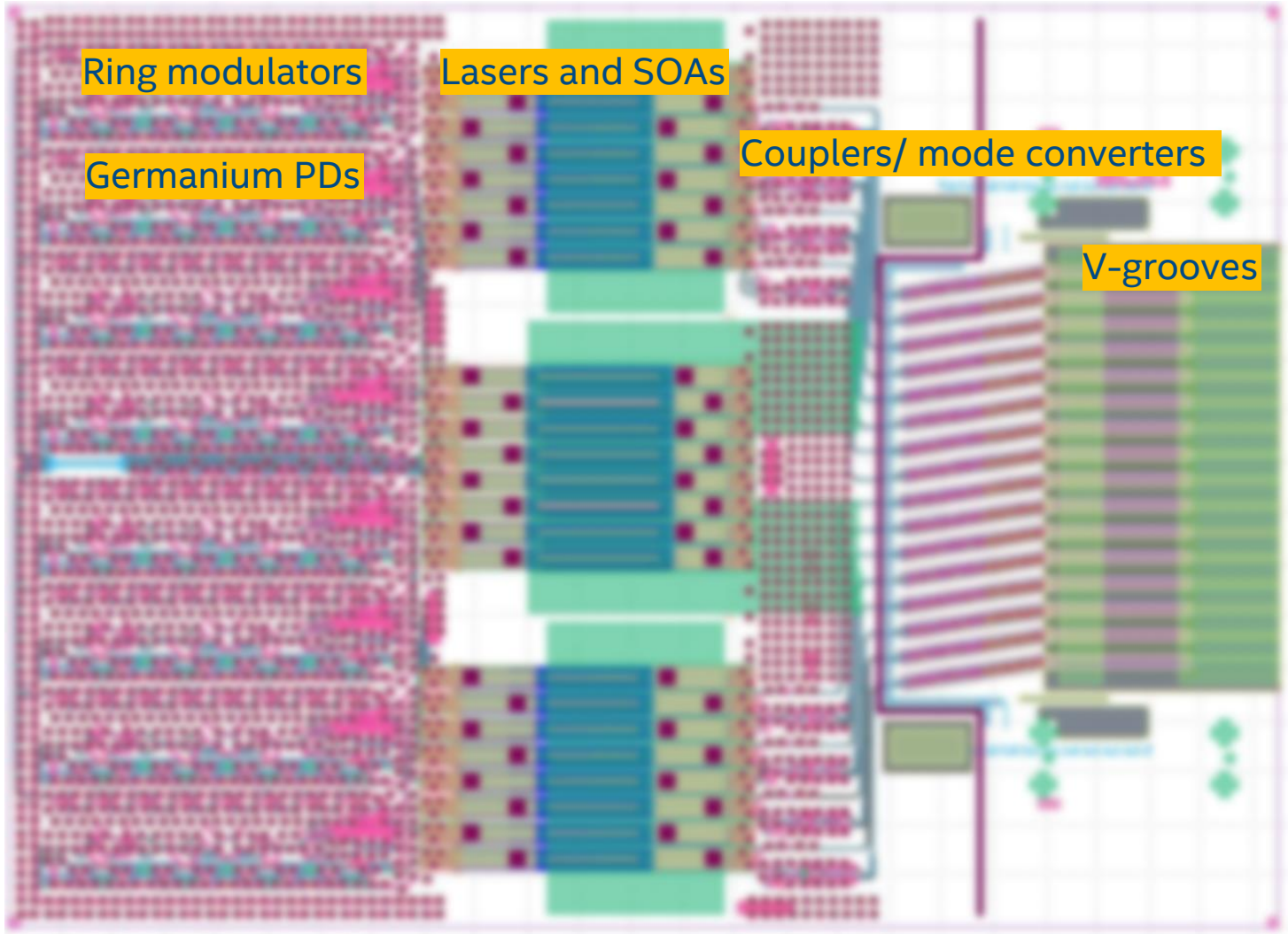
- Total data rate: 4-64 Tbps
- BW/shoreline: 500-2000 Gbps/mm
- Energy efficiency: < 3 pJ/bit

- Fully integrated PIC
- Fully integrated EIC
- Embedded bridge to further drive density

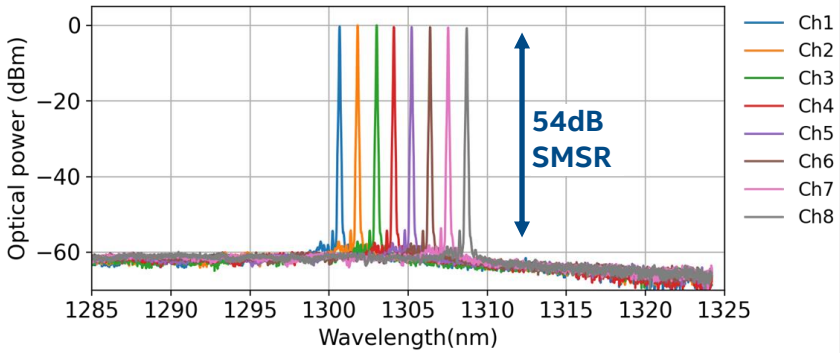
Scale optics BW density to enable closer integration and power reduction

Intel estimates, values for directional purposes

8 Tb/s Photonic IC for Optical I/O

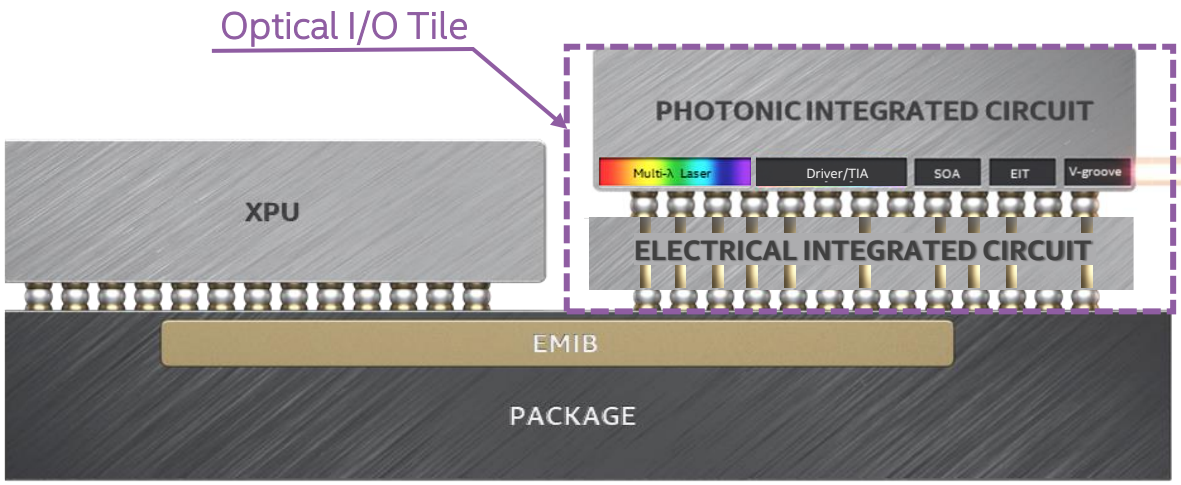


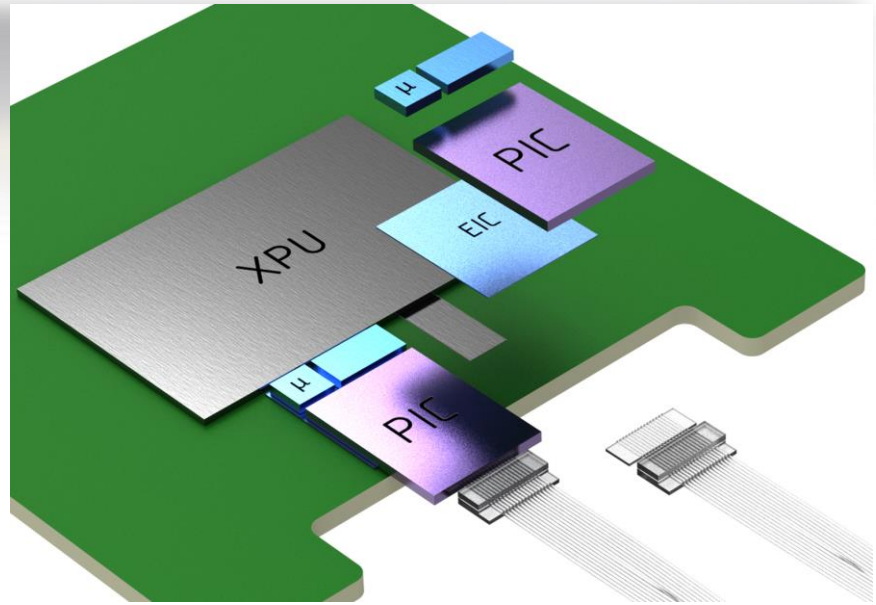
- 8 Tb/s total bi-directional bandwidth
  - 8λ x 64 Gbps NRZ per fiber
  - 8 fibers for transmit; 8 for receive
  - On-die lasers and amplifiers
  - High speed ring modulators
  - High speed Ge photodetectors
  - Polarization diverse design
  - Low-NA couplers & V-grooves for fiber coupling
- High volume platform for optical I/O
  - Compact size through ring resonators and 8-channel multiplexing
  - 8ch on-chip DFB array with 200GHz channel spacing



D. Huang et al., "8-channel hybrid III-V/silicon DFB laser array with highly uniform 200 GHz spacing and power", ISLC 2021

What to Expect from Optical I/O by 2023





Ultra-high bandwidth
~1Tbps per fiber

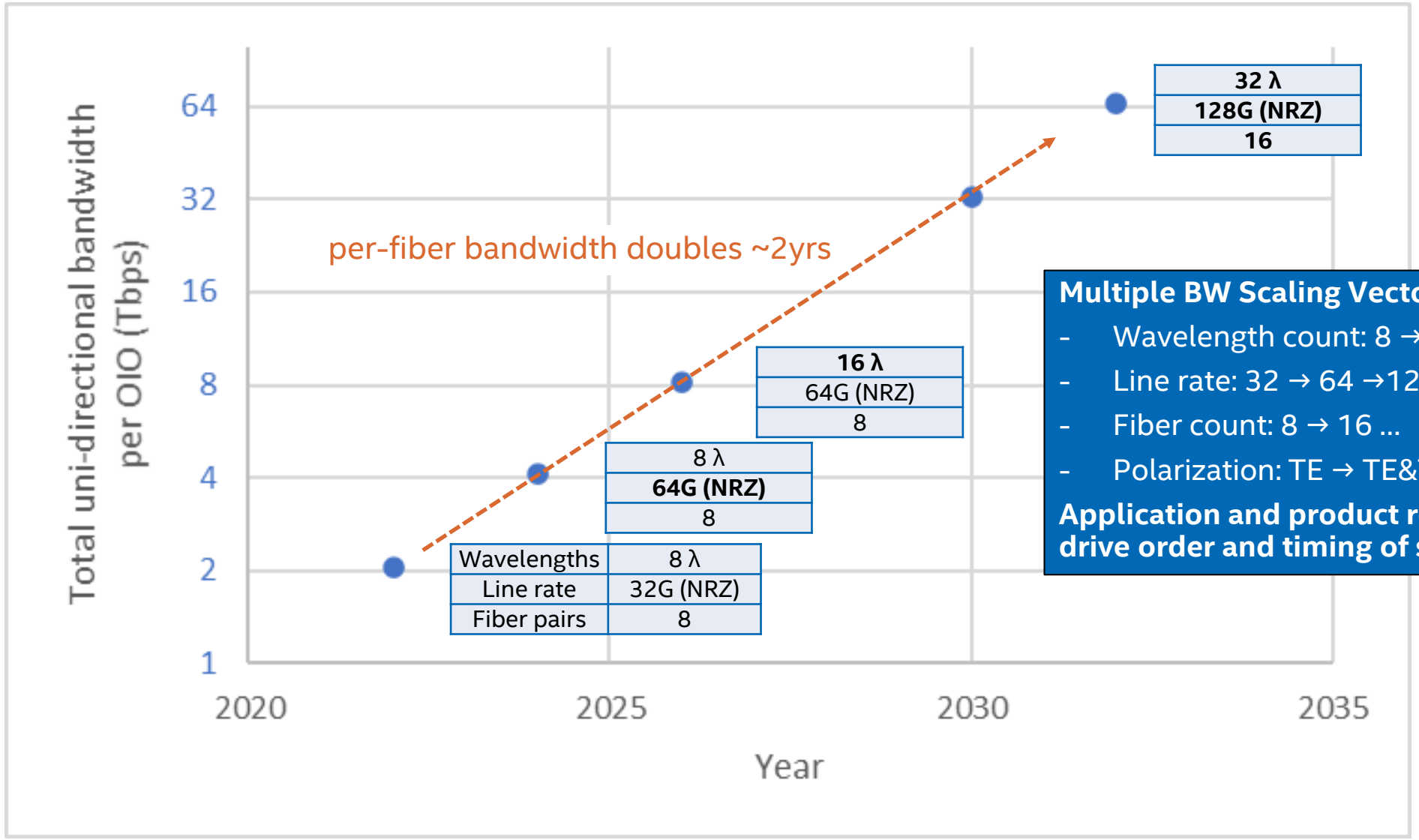
Reach
>100m, orders of magnitude better than electrical I/O

Shoreline Density
>4x improvement over PCIe6

Energy Efficiency
Trending to 3pJ/b (65% of PCIe6)

Latency
<10ns + TOF, comparable to electrical I/O

OIO Bandwidth Scaling Trajectory



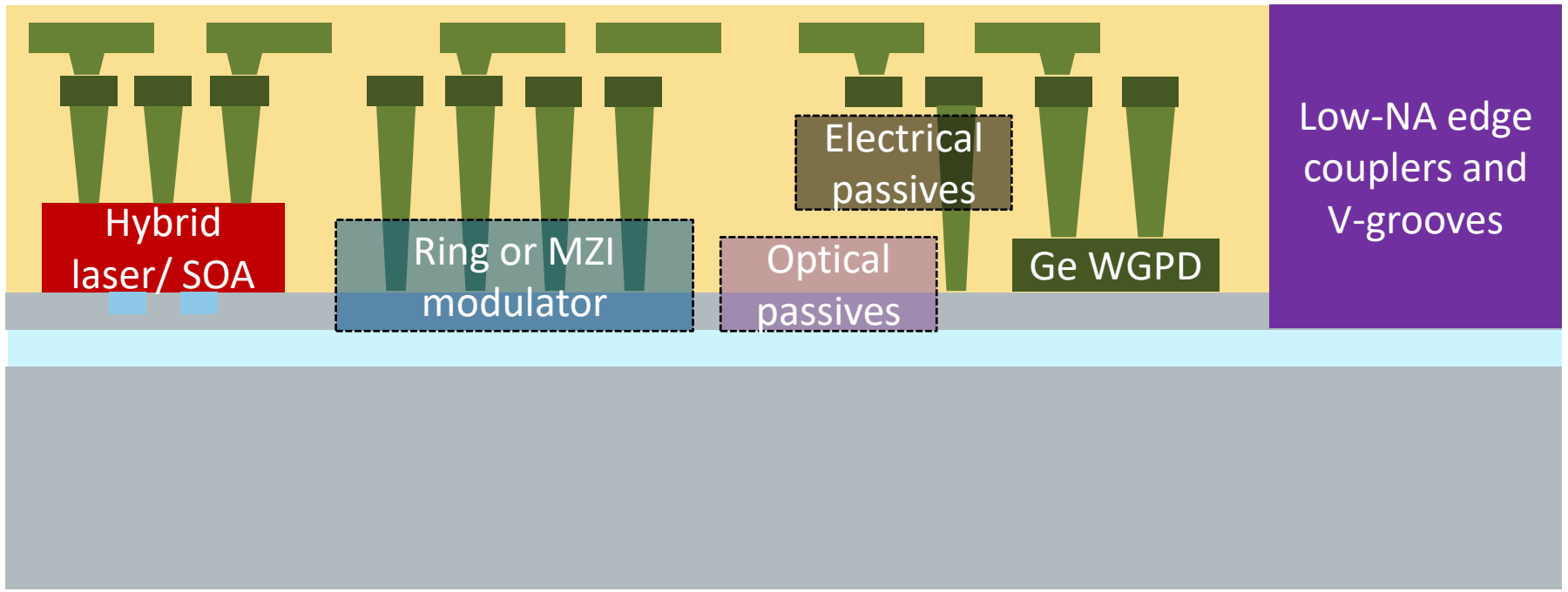
Multiple BW Scaling Vectors:

- Wavelength count: 8 →16 →32 …
- Line rate: 32 → 64 →128 Gbps …
- Fiber count: 8 → 16 …
- Polarization: TE → TE&TM

Application and product requirements will drive order and timing of scaling vectors

Directional Intel estimates

Most Integrated Silicon Photonics Process



Additional process features:

- High efficiency phase modulation
- Wafer-level trimming technology
- Avalanche waveguide photodetectors (optional)
- Electrical passives (resistor and capacitor)
- Optical passives (MMI, Polarization splitting & rotation, MUX/DEMUX, etc.)
- V-grooves for fiber alignment (optional)
- Compatible with flip-chip Tx/Rx IC assembly

Components in Silicon Photonic Integrated Circuits

Active Optics

Hybrid DFB Lasers
Electrons generate photons

On-chip SOAs
Optical Power Amplification

On-chip SLED
High-power, low-coherence

SiGe Photodetectors
Photons generate electrons

- NI PD
- Waveguide PD
- Avalanche PD

Si Modulators
Electrons control photons

- Mach Zehnder Modulators
- Micro-ring Modulators

Passive Optics

MUX/ Demux

Coupling I/O

Optical Filter

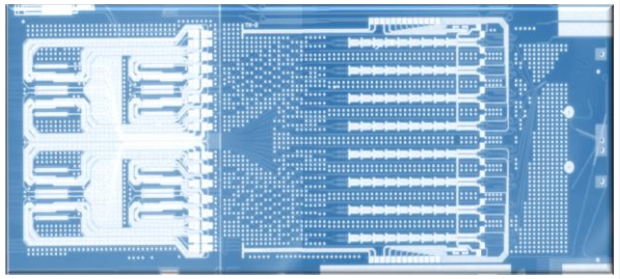
Interferometer/Switch

Splitter/Combiner

Polarization Diversity

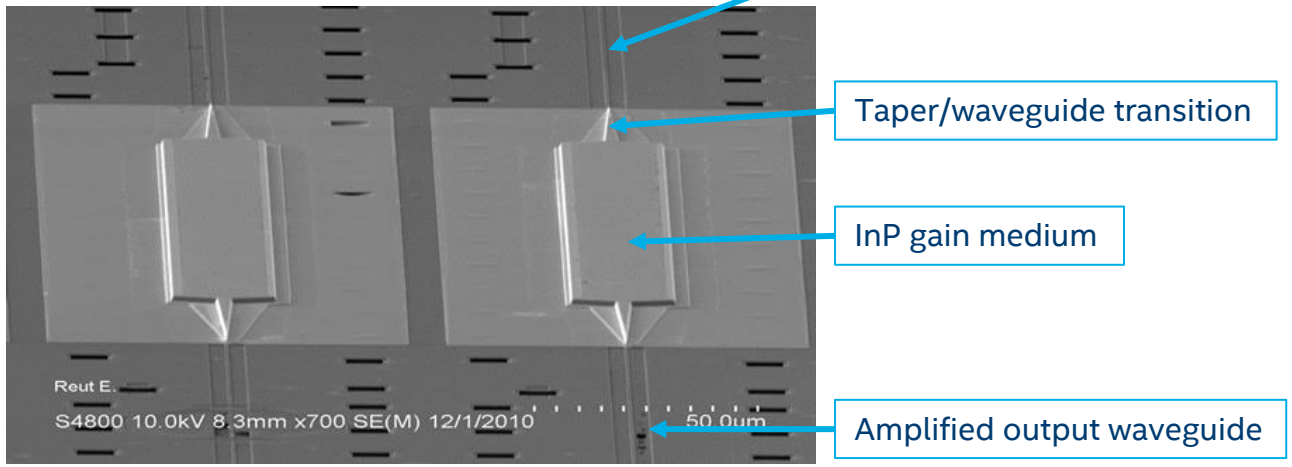
Electronic Circuits

- Resistors/ Capacitors
- Modulator Driver
- TIA
- CDR
- µ–Controller
- Serdes
- etc

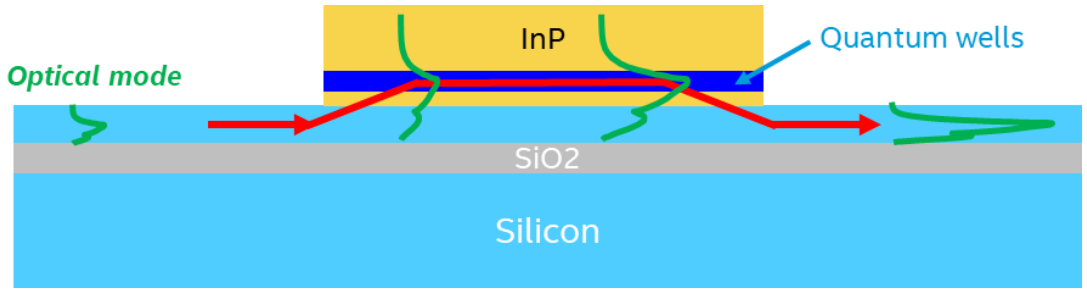


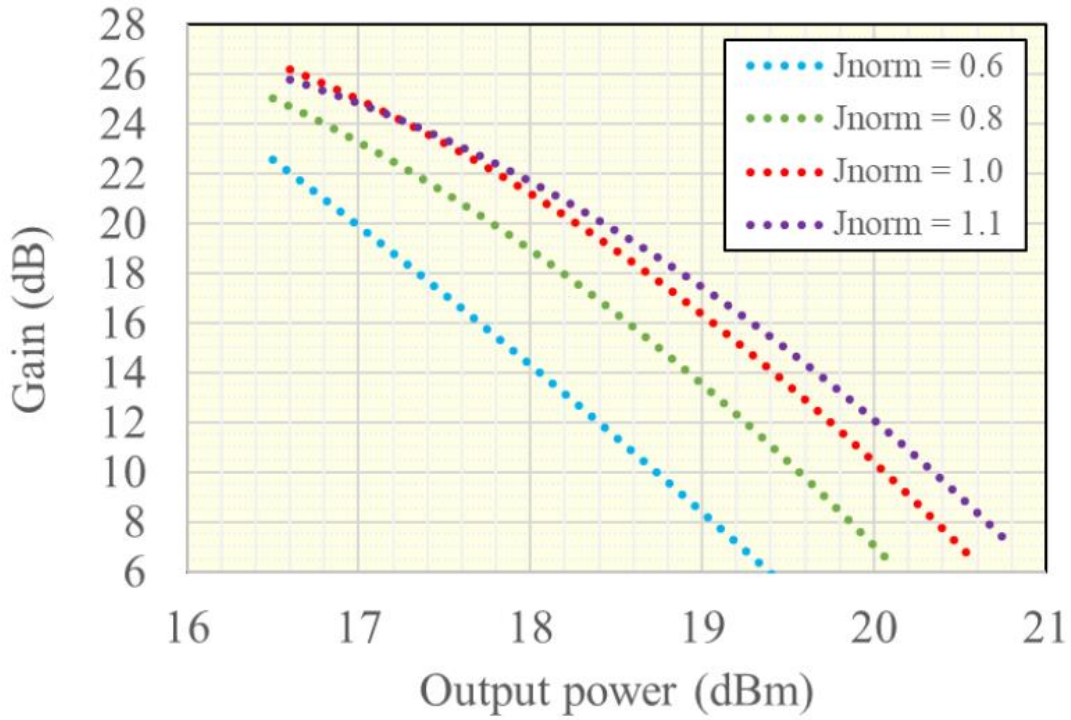
Optical On-Chip Amplifiers Enable High Output Power

Top view (concept)



Side view

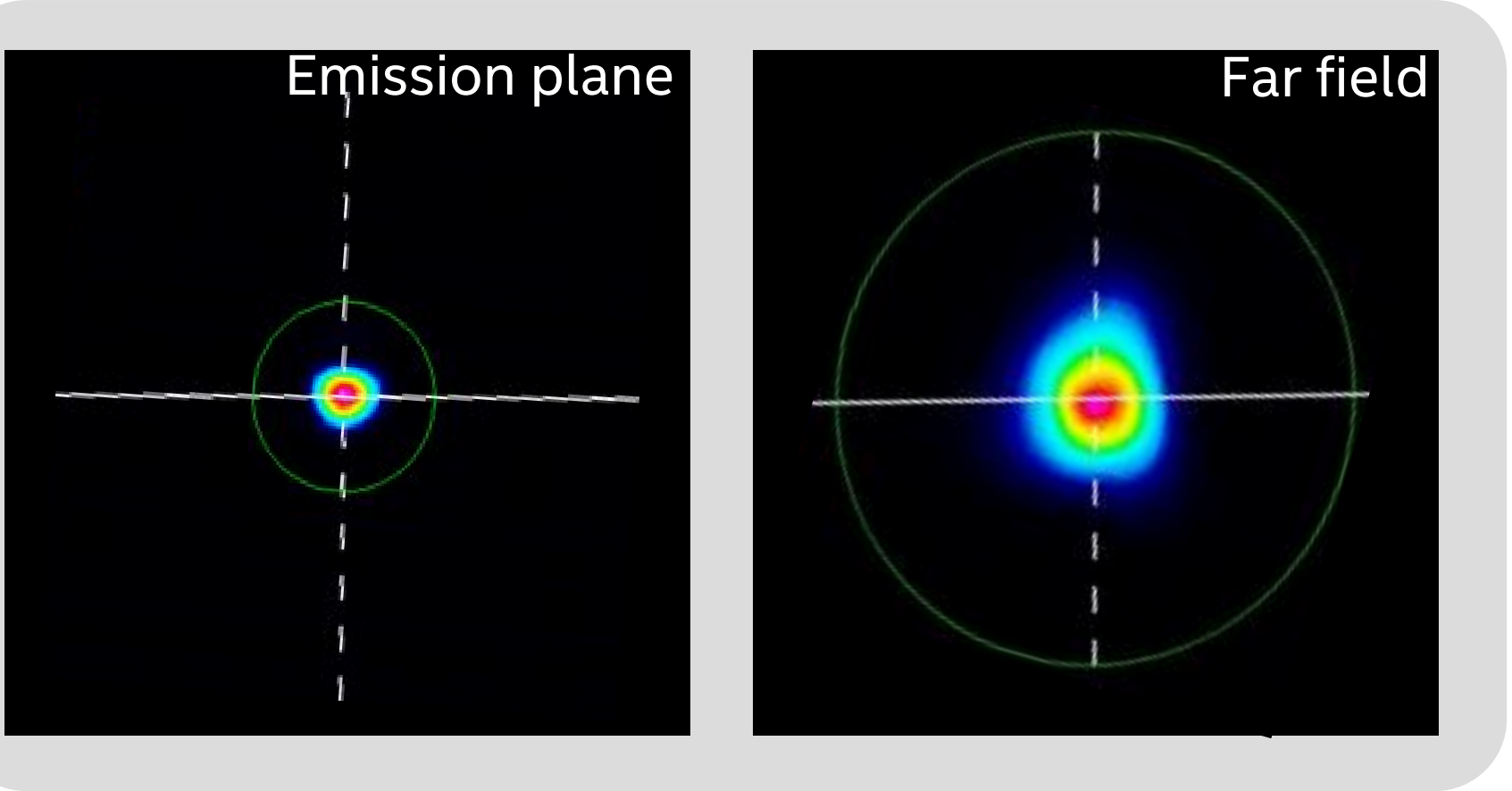




- 100mW (20dBm) output power from semiconductor optical amplifiers (SOAs)
- On-chip SOAs are unique differentiation for Intel hybrid integration platform

J. K. Doylend, S. Gupta, "An overview of silicon photonics for LIDAR," Proc. SPIE 11285, Silicon Photonics XV, (SPIE OPTO/Photonics West 2020)

Optical output to free space

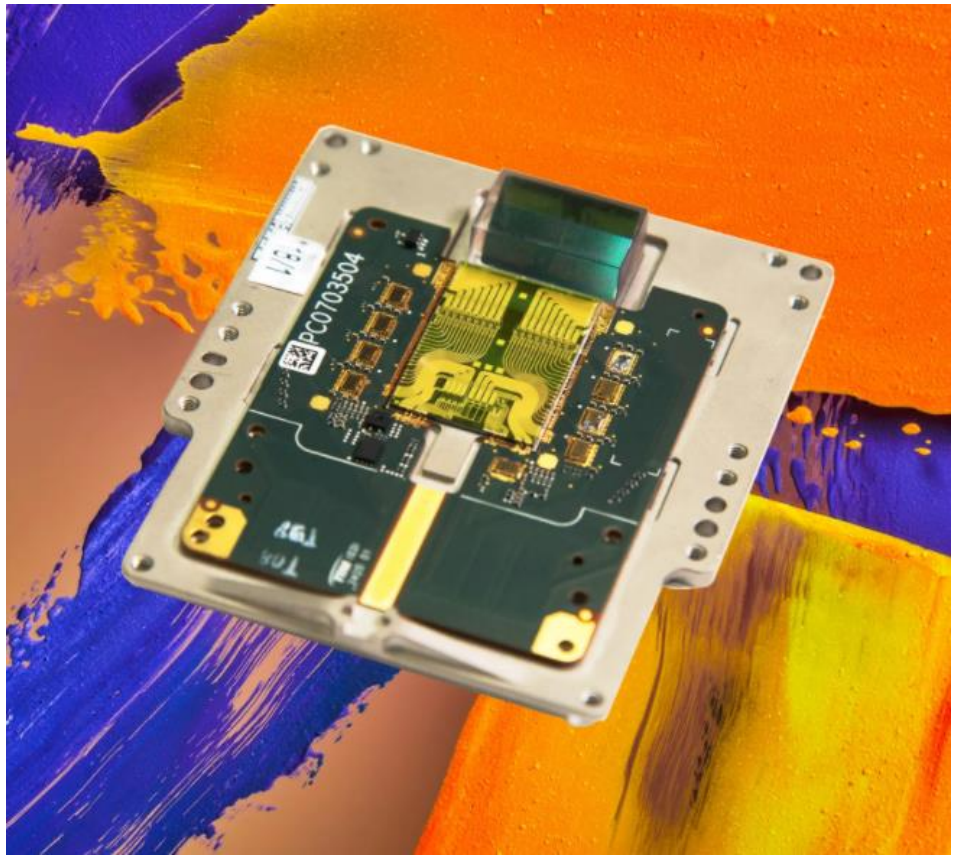


Optical output from chip with $M^2 < 1.2$

J. Doylend, "Silicon Photonics for LiDAR", SPIE Defense and Commercial Sensing 2021

FMCW “LiDAR on a chip”

Integrating 6000+ active and passive components on chip for high volume manufacturing



Mobileye CEO Amnon Shashua shows of the company's new lidar SoC prototype.
PHOTOGRAPH: MOBILEYE

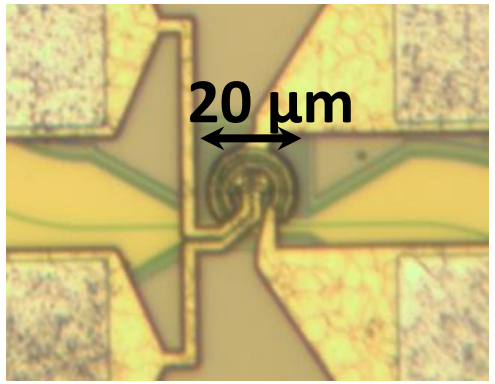
https://www.wired.com/story/mobileye-lidar-on-a-chip-intel/

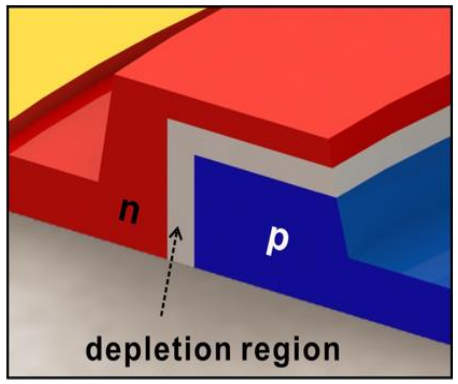
https://www.intc.com/news-events/press-releases/detail/1435/ces-2021-mobileye-innovation-will-bring-avs-to-everyone

https://newsroom.intel.com/wp-content/uploads/sites/11/2021/01/Under-the-hood-deck.pdf

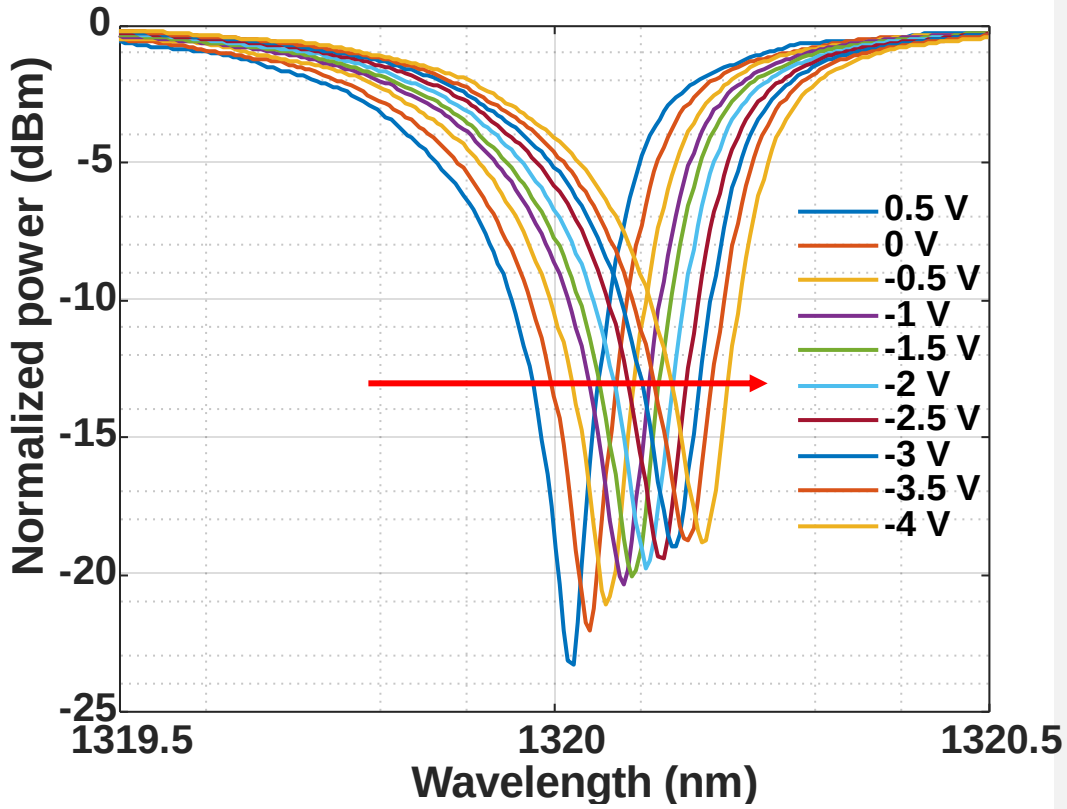
Micro Ring Modulators – A key Component for Sensing

- **PN junction design**
  - High phase efficiency (overlap & optimized doping)→<0.55 V.cm@1310 nm
  - Low resistance and capacitance (high RC bandwidth)→50 GHz EO BW



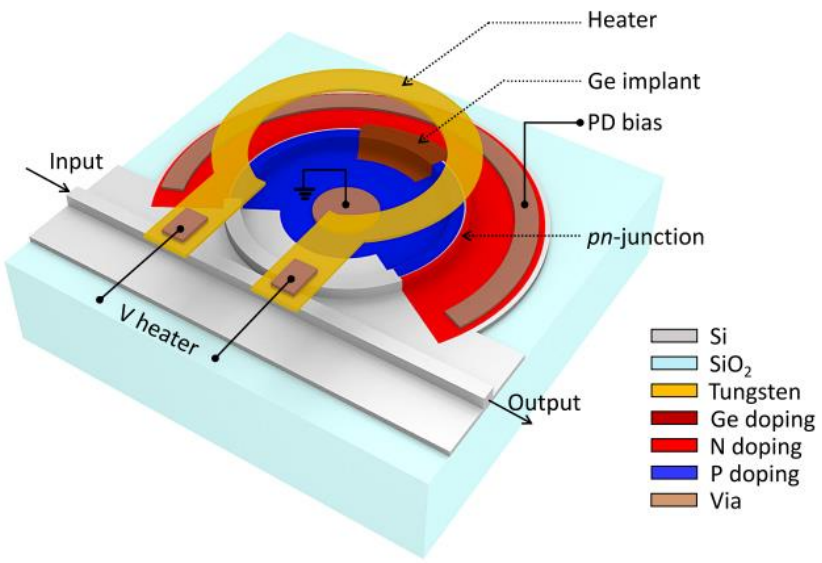


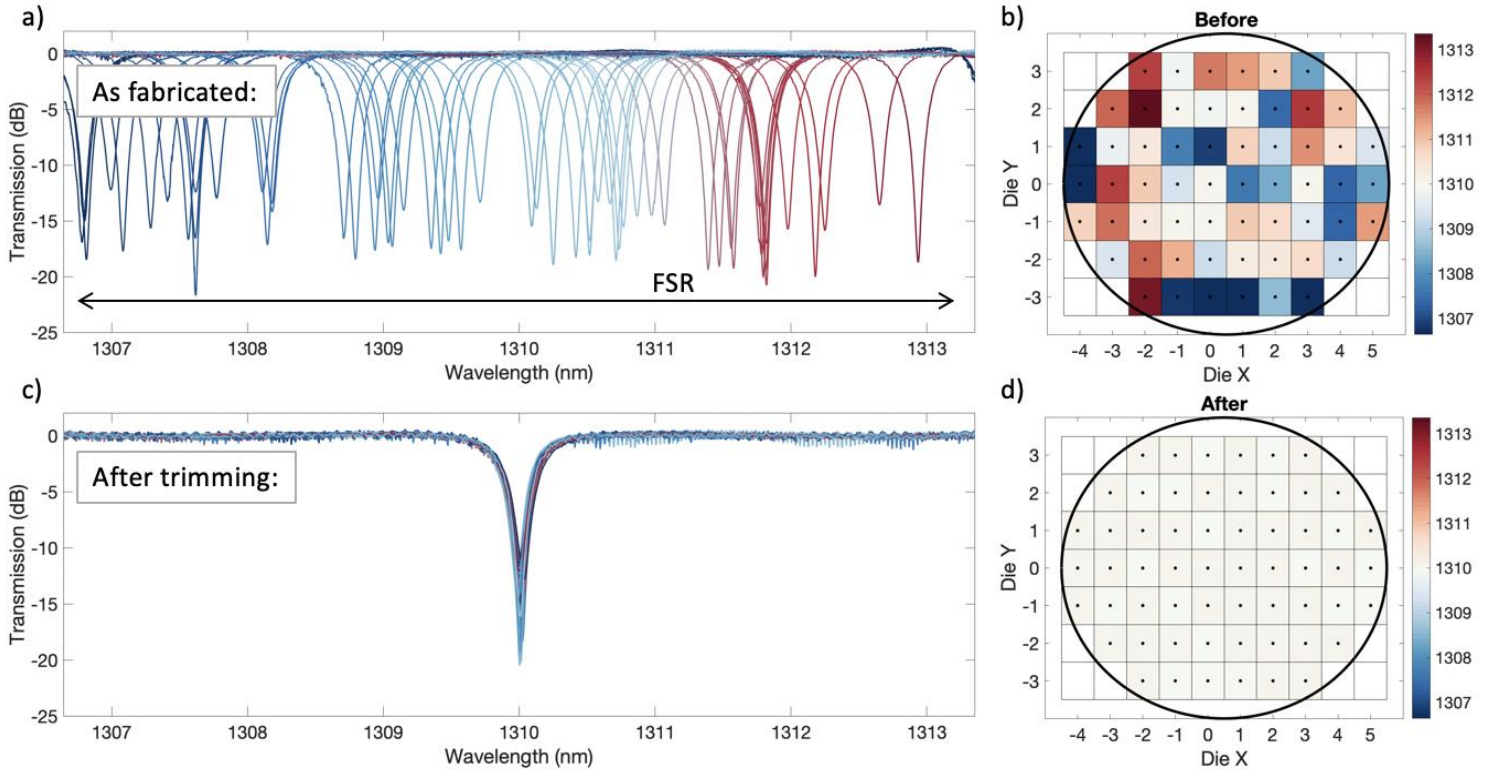
DC bias vs WL shift



Meer Sakib et al., "260 Gb/s/λ PDM Link with Silicon Photonic Dual-Polarization Transmitter and Polarization Demultiplexer", Tu4D.1, ECOC 2021

Micro-Ring Trimming at Wafer Level

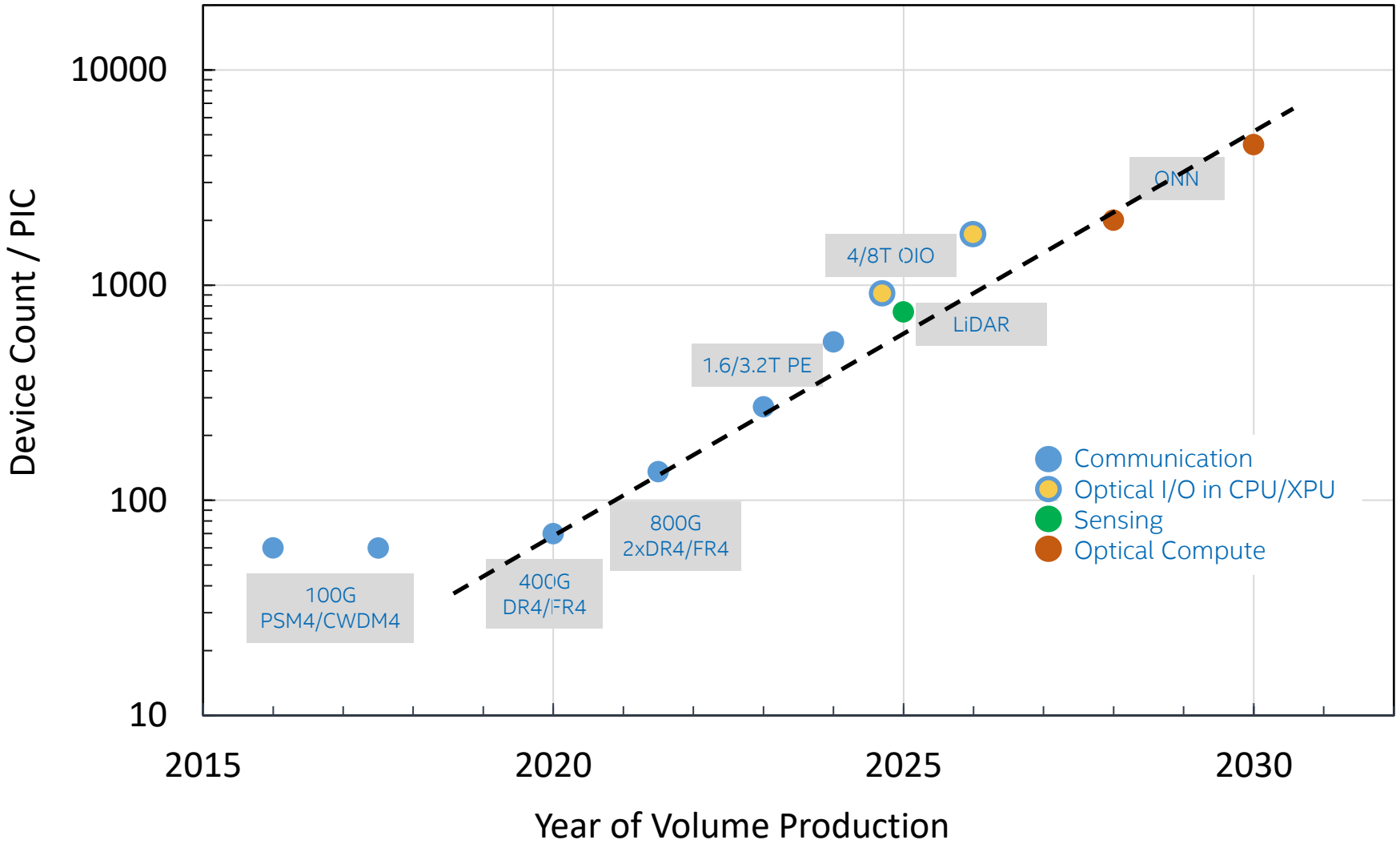




- Automated trimming of resonance wavelength at wafer-scale
- Trimming within ±32pm through Ge implantation on to Si waveguide
- Applicable to other components as well

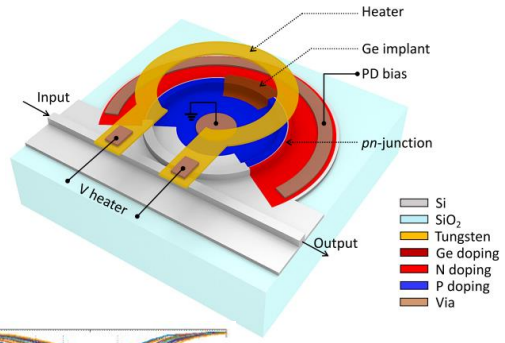
H. Jayatilleka et al., "Post-Fabrication Trimming of Silicon Photonic Ring Resonators at Wafer-Scale", J. Lightwave Tech., 39(5), 5083, 2021

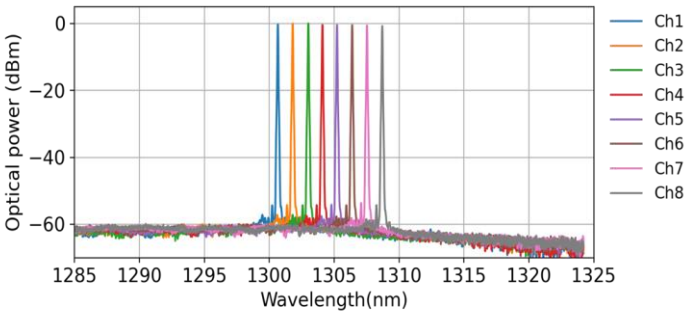
Silicon Photonics "Moore's Law" Scaling

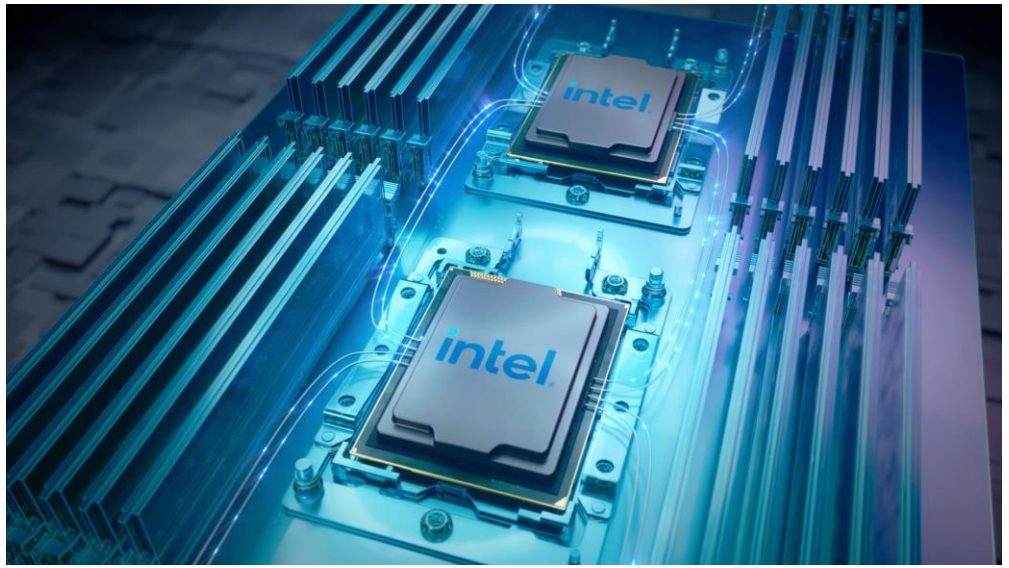


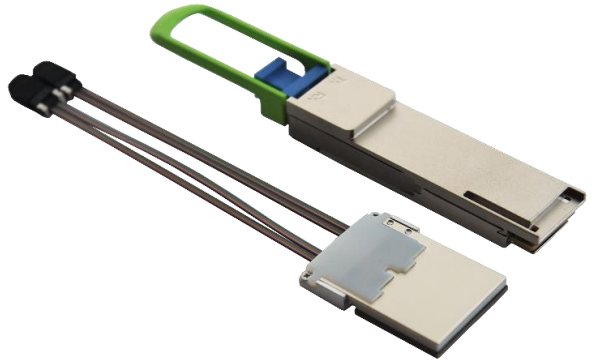
Directional Intel estimates

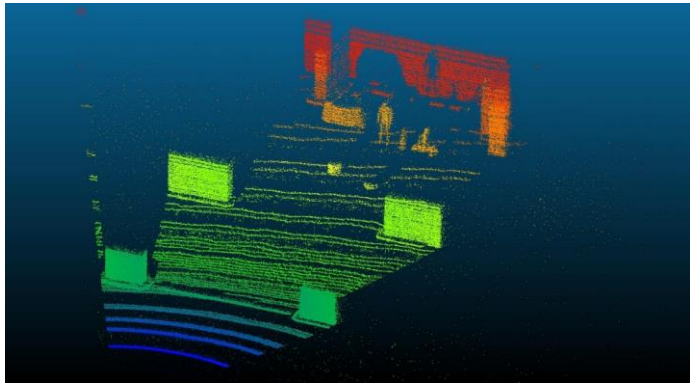
Silicon Photonics: An Ideal Platform for Optical I/O and Many Other High-Volume Applications

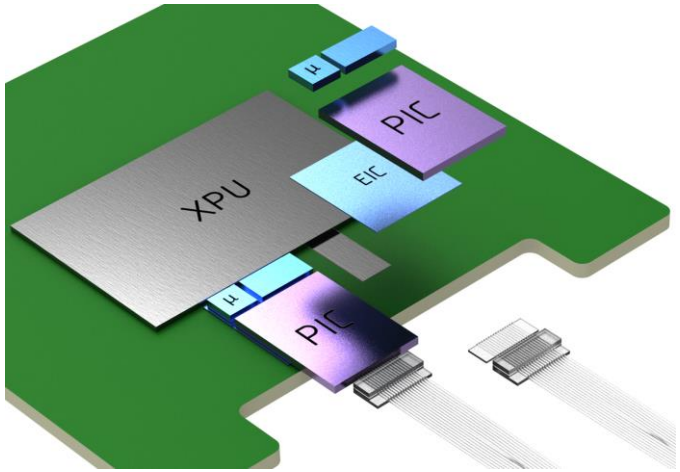












Thank You!

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