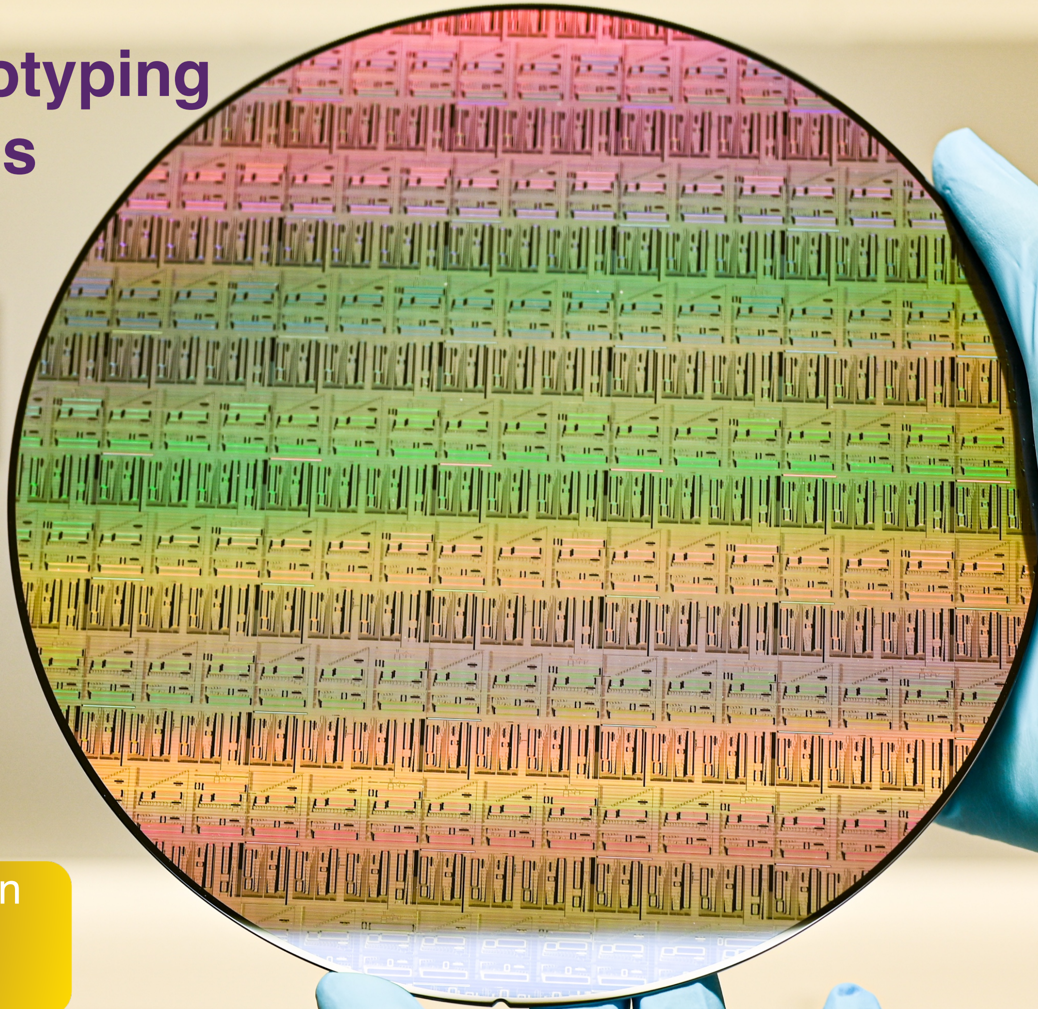
Low loss PICs: From fast prototyping to high volumes



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Leader in low loss Silicon Nitride Integrated Photonics

EPFL

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European PIC Company

Headquarters in Lausanne (CH)

Originating from EPFL (Kippenberg Lab)

LIGENTEC Snapshot

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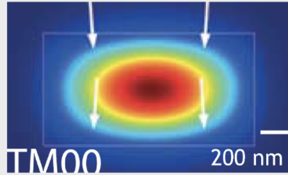
Thick SiN – the game changer



90% of the light is confined
- Low propagation loss
- Small chip size
- Non-linear optics
- High Power, VIS to IR

All Nitride Core Technology: combining the benefits of
- **Silicon Nitride** (VIS-IR, low loss, high power) with
- **Silicon Photonics** (small chip size, scalability)

Versatile PIC Platform

3+ thicknesses
- 800 nm
- 400 nm
- 150 nm
- custom

10 process modules

SiO2, Heater, SiN, waveguides, Si
2nd layer, LoCA, Rib, Si

- Modular
- CMOS compatible
- Scalable

Extensive PDK

- Design rules
- Design Rule Checks
- Layout files
- Primitives
- Building Blocks
- IP Cores

Components
- Waveguides, delay lines
- Couplers / MMIs
- Crossings
- Filters (RRs, AWGs)
- Switches
- Polarization mgt

Optical I/O
- Grating couplers
- Inverted tapers
- Spot size converters

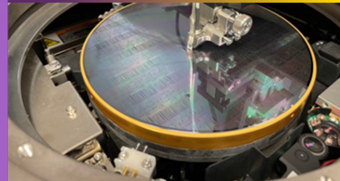
Design flows: VLC Photonics, Mentor (A Siemens Business), Synopsys (Silicon to Software), Luceda Photonics, VPIphotonics, Ansys / Lumerical

Simulations
- Component and circuit simulation
- Technology files
- Cross section

Commercial Offering

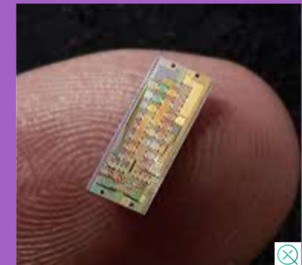
R&D and Prototyping
Open access, low barrier

Custom PIC Developments
High flexibility & competence



Manufacturing
Niche to high volumes

We deliver PICs



One base – many options:

SiN – The platform for monolithic & heterogeneous integration

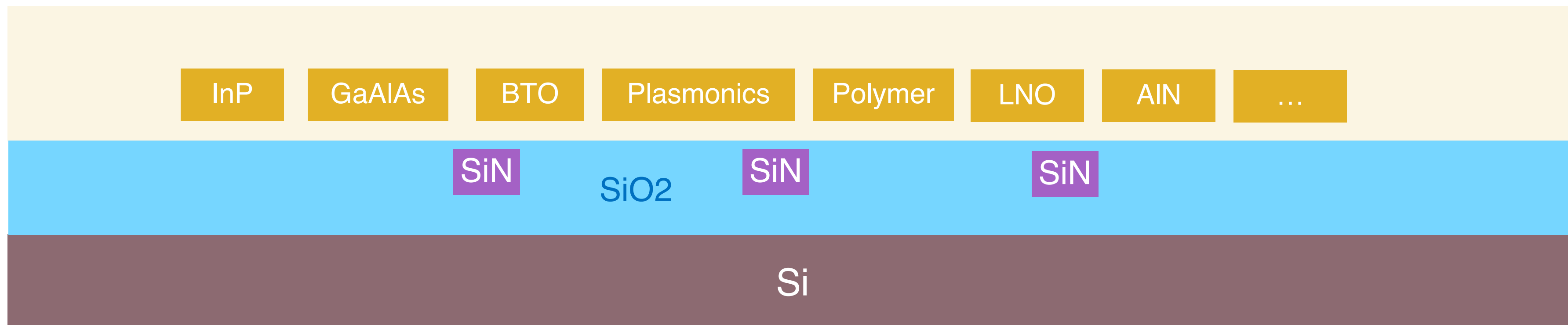
Use SiN as base platform for general circuitry

- Comprehensive PDK
- Standard I/Os
- Scalable to volume

Add materials as required by application

Focus on wafer level integration e.g.:

- Monolithic integration
- Wafer bonding
- Micro Transfer Printing



Integration Technologies

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Monolithic Integration

Deposited *or grown on the wafer*

- Best cost option potential
- Performance trade-off
- Limited material choice
- Mature for same platform materials

Heterogeneous Integration

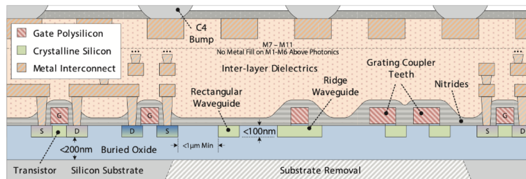
Transferred */ bonded on the wafer*

- High material integration flexibility
- Best material per application
- Low cost potential
- Emerging technology

Hybrid Integration

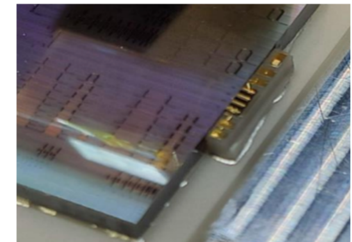
Assembled in the package

- High flexibility
- KGD integration
- Packaging complexity
- Costly in volumes



Sun *et al.*, JSSC. **50**, 893 (2016)

Source: EVG



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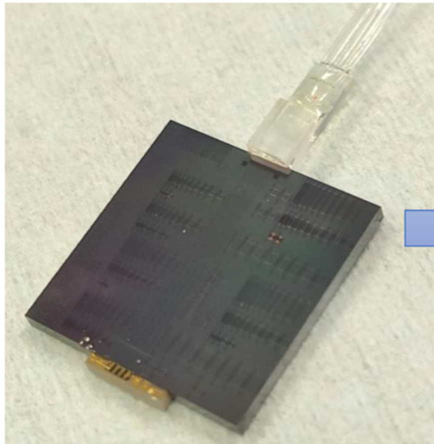
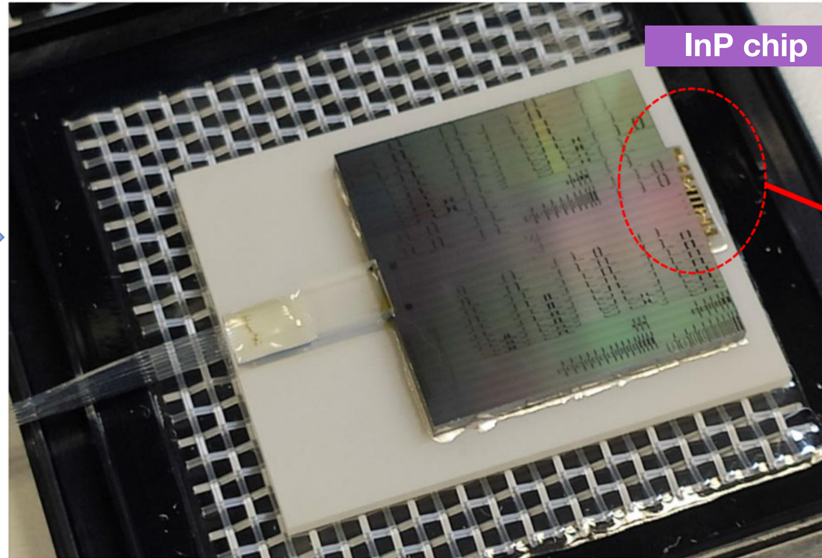
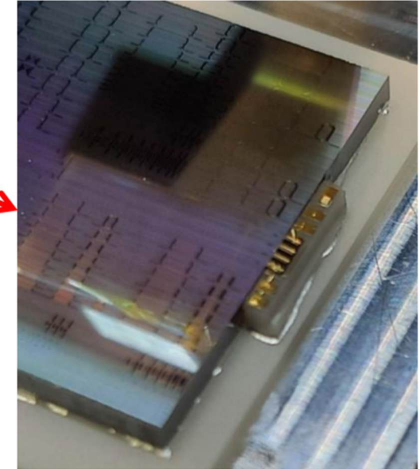
Hybrid Integration example

InP Chip to passive SiN PIC







- SiN chip with FAU and SOA attached to it
- Assembly is glued on a ceramic carrier
- **Requires flat and smooth chip facets**

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Heterogeneous Integration

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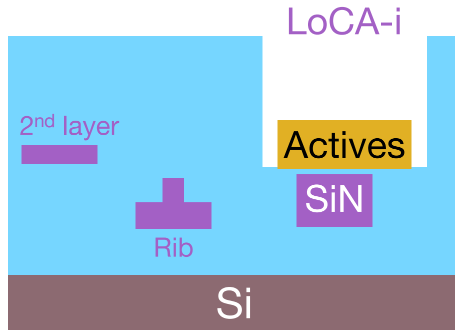
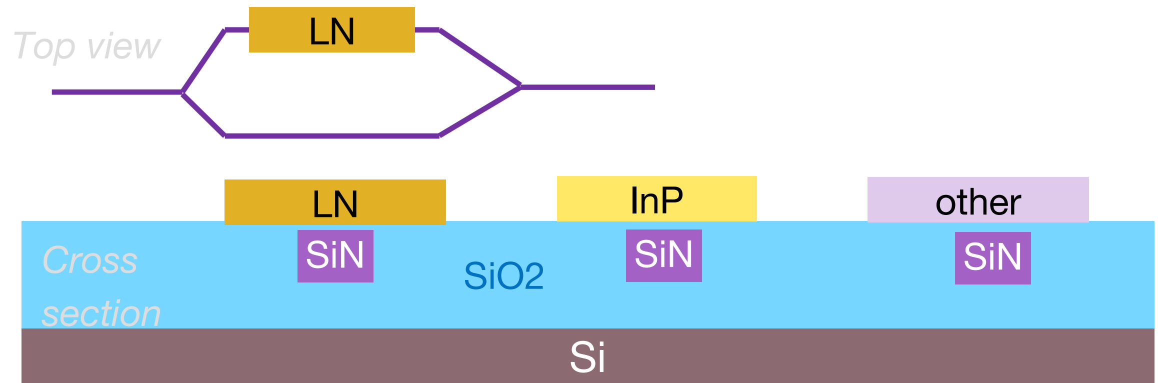
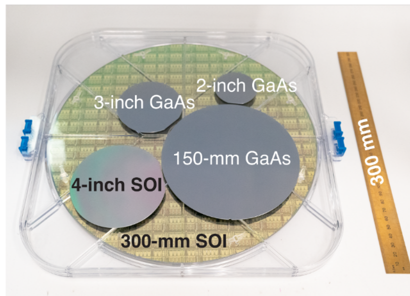
Chip to Wafer

Wafer to Wafer







- Thermal budget, after material transfer, is reduced → increased propagation losses or new material
- Yield of combined stack is reduced ($Yield_{SiN}$* $Yield_{active}$* $Yield_{integration}$) → preference to test both active and SiN
- Wafer size not always available for W2W integration in photonics

Heterogeneous Integration examples

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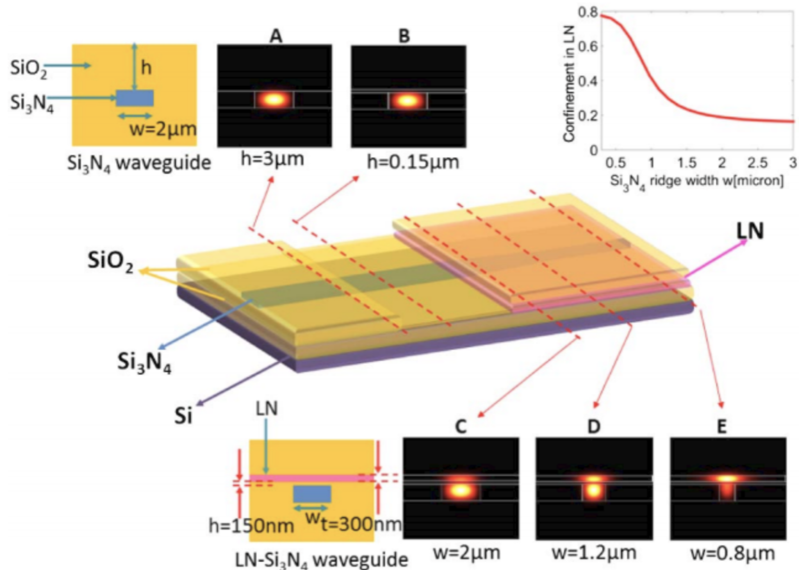
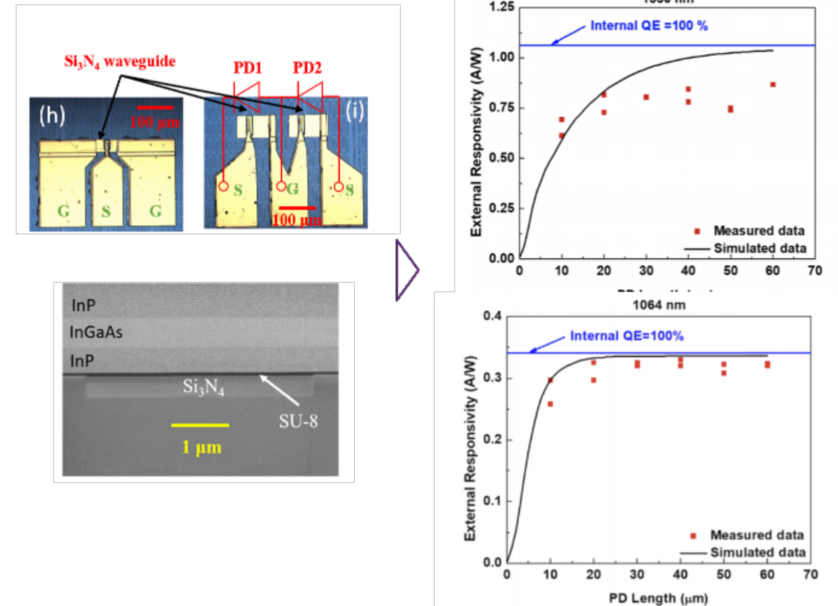
LiNbO3



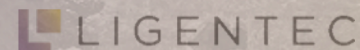
Heterogeneous integration of lithium niobate,
Chang et al., Optics Letters (2017)

InGaAs Photodiodes



Heterogeneous photodiodes on SiN,
Yu, Optics Express 28 (2020)

Thanks to all Ligentec Team



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