PsiQuantum

Electro-Optics MCM Packaging for Quantum Computing

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Agenda

- Company Profile
- Quantum Computing Architecture – Packaging Requirements
- Conventional packaging – The Building Block
- Datacenter optics – Leading Infrastructure Development
- Recent packaging Trends – High Performance Computing (HPC)
- Summary

About Psi Quantum

A silicon wafer containing thousands of quantum devices designed by PsiQuantum and fabricated by GlobalFoundries

PsiQuantum Closes $450 Million Funding Round to Build the World's First Commercially Viable Quantum Computer

Jul 27 2021 · PsiQuantum Press Release

About PsiQuantum

Powered by breakthroughs in silicon photonics and quantum architecture, PsiQuantum is on course to build the world's first commercially useful quantum computer to solve some of the world's most important challenges. PsiQuantum believes silicon photonics is the only way to achieve the necessary scale required for error correction and deliver a fault-tolerant, general-purpose quantum computer. With quantum chips now being manufactured in a world-leading semiconductor fab, PsiQuantum is uniquely positioned to deliver quantum capabilities that will drive advances in climate, healthcare, finance, energy, agriculture, transportation, communications, and beyond. To learn more, visit www.psiquantum.com

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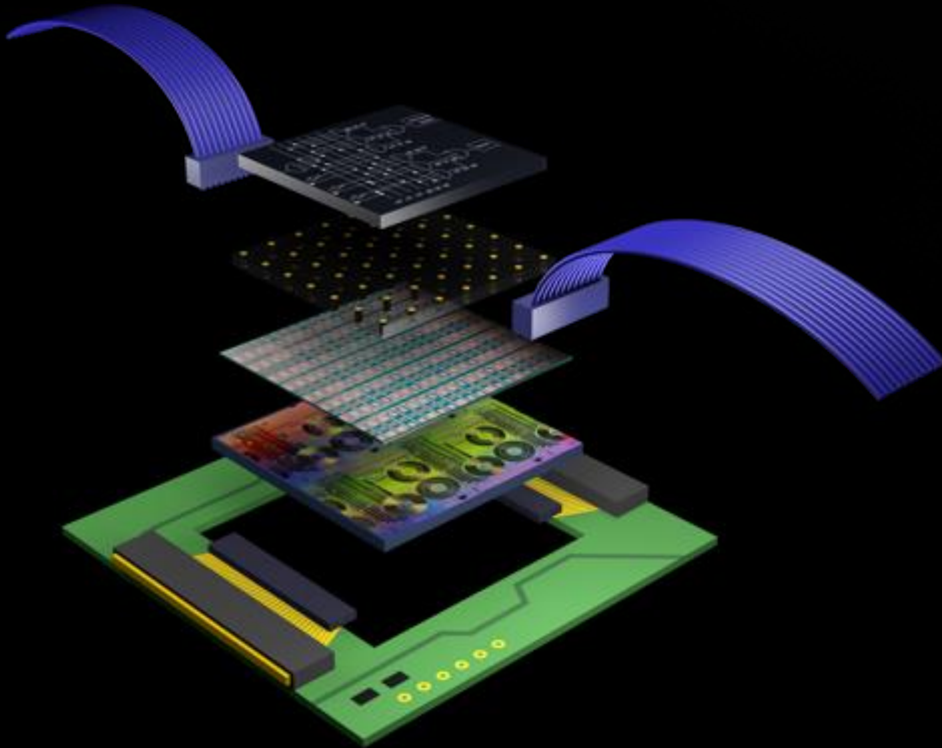
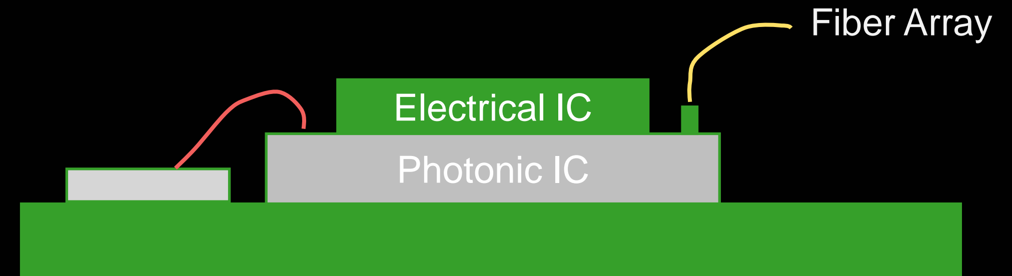
40 years of IC Packaging Interconnect Development

- From Mainframe computing to now Quantum Computing
- From pluggable connector to now face to face connect

Quantum Computing Packaging

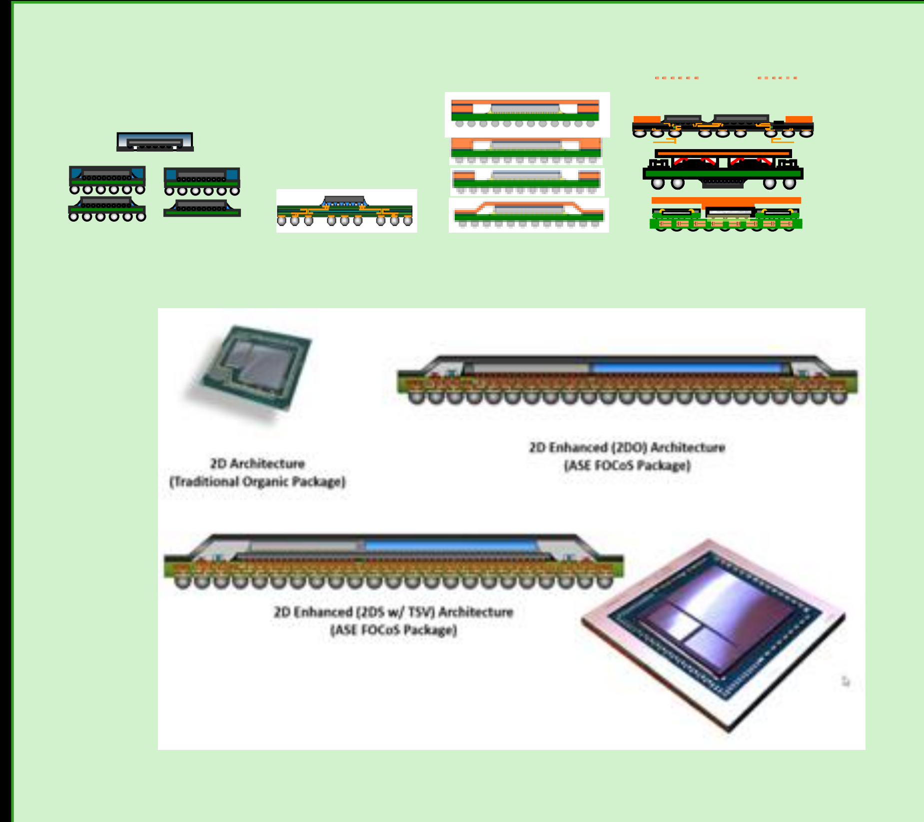


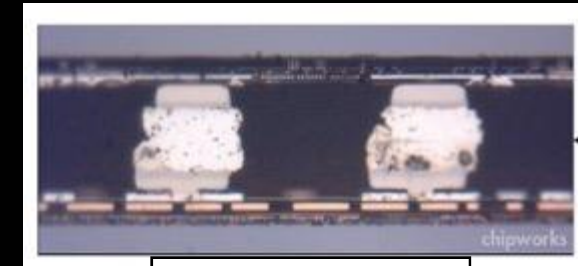


- 3D Integration of EIC and PIC IC
- Fiber coupling of Optical IO
- Reliability Performance at Cryogenic Temperature
- Validation of Packaging Assembly Processes & Materials

Flip chip Interconnect – A Building Block for the Advanced Packaging

- Interconnect
  - Wire bonding
  - Flip chip
- Substrate/Interposer
  - Ceramic, Laminate, Silicon/Glass
- Integration Processes
  - Bumping
  - Reflow/Thermo Compression Bonding
  - Face to Face Bonding
  - 2.5D Interposer
  - Wafer level Fan – Out



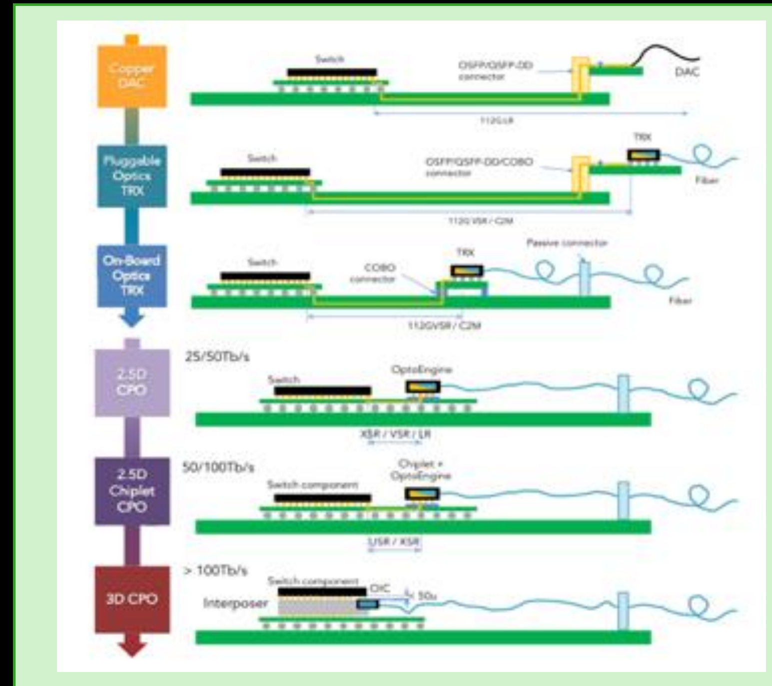


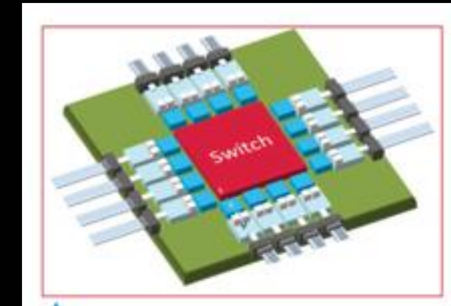
Bump Interconnect

Package Substrate
IO Density & Performance

Source: ASE, TechSearch

Datacenter Optics – Evolution to Co-Packaged Optics

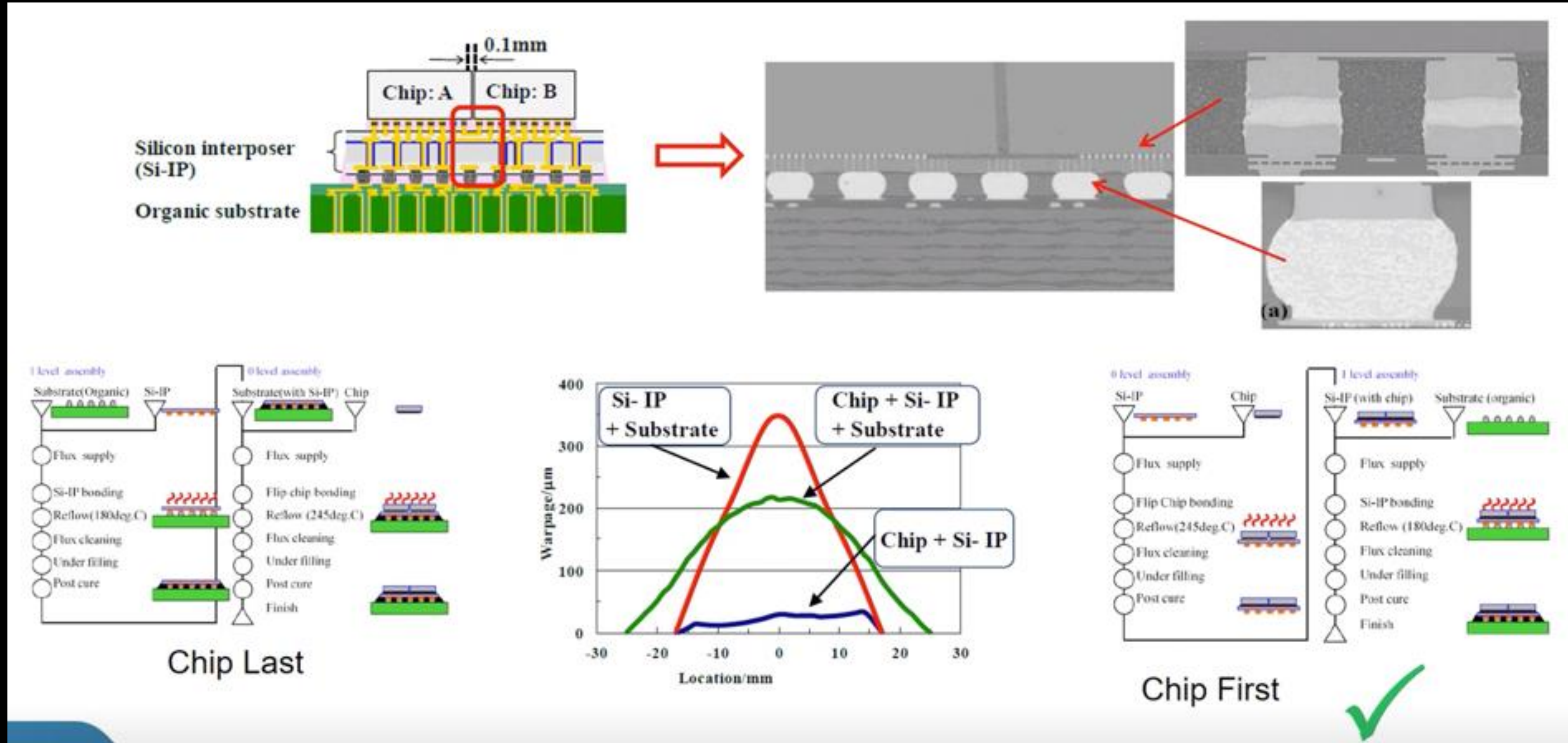




- On-board to achieve proximity to the main switch ASIC
  - Co-packaged optics is the most attractive solution
  - Can realize cost and power reductions of up to 50%.

Source: IET

Electro-Photonic Multi-Chip Module- 2.5D Interposer



Source: A Star/IEEE 2021

2.5D Assembly process flow

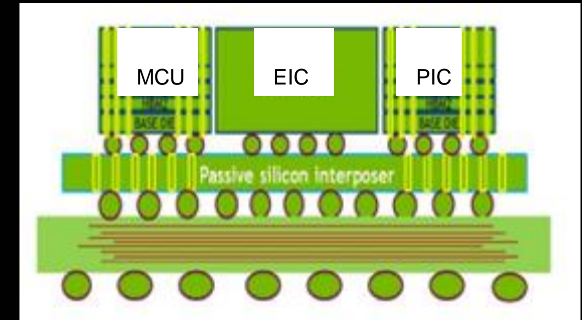
SiPH → Wafer level probe/test → UBM/Bump → Wafer saw

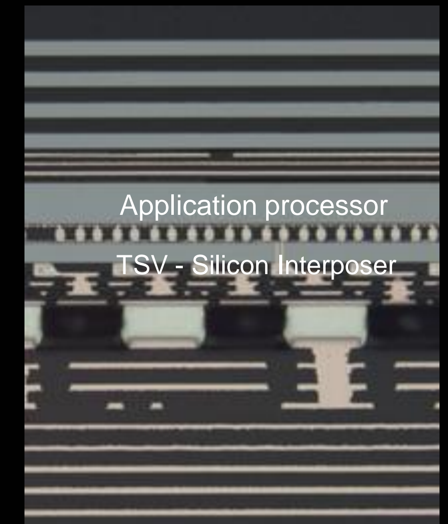
Interposer Fabrication → Interposer Test → Interposer Assembly → Wafer level probe/test → Dicing

EIC → Test → Singulation

HDI Substrate → Passive Attach → Interposer Attach

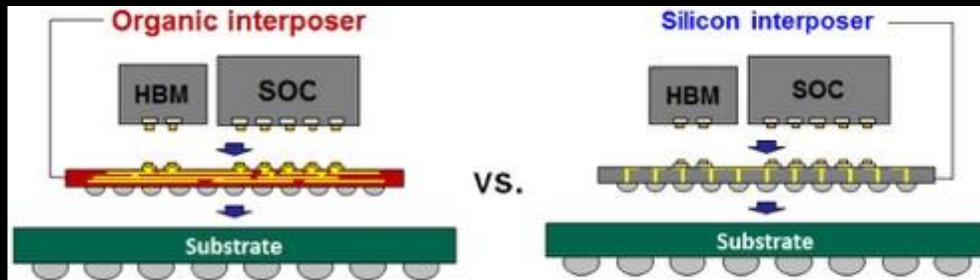
MCM Test → Fiber Attach/Test/ Ship





Source: Yole
Samsung Galaxy

Electro-Photonic Multi-Chip Module –Interposer



Source: TSMC

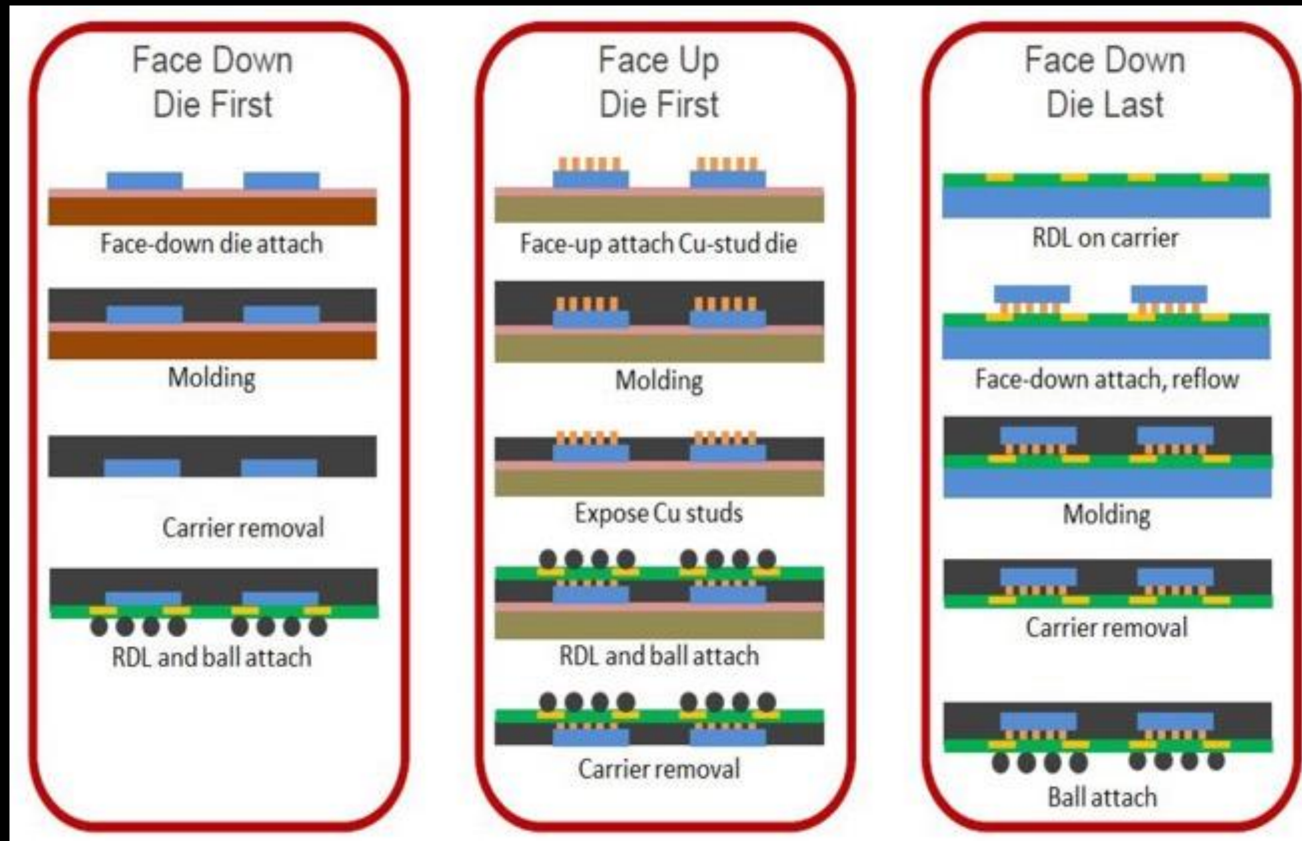
Silicon versus Glass 3D interposers

Excellent
Fair
Difficult

	Silicon interposers	Glass interposers
hermeticity	Difficult to achieve	Full-Hermeticity is possible
optical transparency	Only to IR	Key for optical applications
via pitch	10-500µm	50-500µm
Substrate thickness	20-700µm	100-700µm
RF dielectric constant	~11,8	~4,6
Electric isolation	various possible resistances (25mΩ.cm to 5kΩ.cm)	perfect isolator → no barrier / isolation layers in via
embedded components	→ Passives: R,L,C, diodes → Active: transistors !	Limited to R,L,C in the back-end-of-line
wafer sizes	6",8",12"	6",8", 12", PANEL size
via filling materials	Cu, W, Au, Poly-Si, Doped-Si	W, Cu, Au
cost of substrate+via	relative high cost of dry etching+isolation+seed layer	Some low cost "embedding" processes available for TGV
cost of redistribution layers	Wide available WLP and CMOS infrastructure on any wafer size	limited infrastructure today
CTE for assembly	~ 3ppm *(issue with Cu via and plastic BGA)*	~ 3 to 10ppm *(depending on glass)*

High density Silicon Interposer widely used- eg. GPU/HBM Packaging

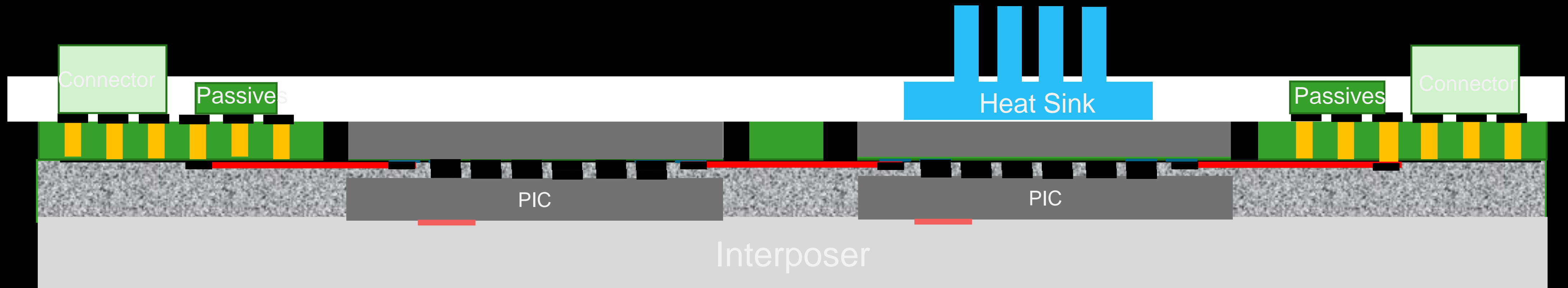
Electro-Photonic Multi-Chip Module – Wafer Level Fan-Out



Wafer level fan-out integration is another approach providing high density interconnect for heterogeneous integration of Electronics and Photonics IC

Source: Innocentrix

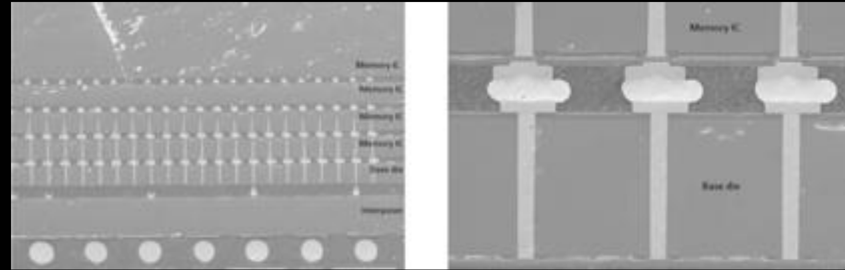
Electro-Photonic Multi-Chip Module – Wafer Level Fan-Out



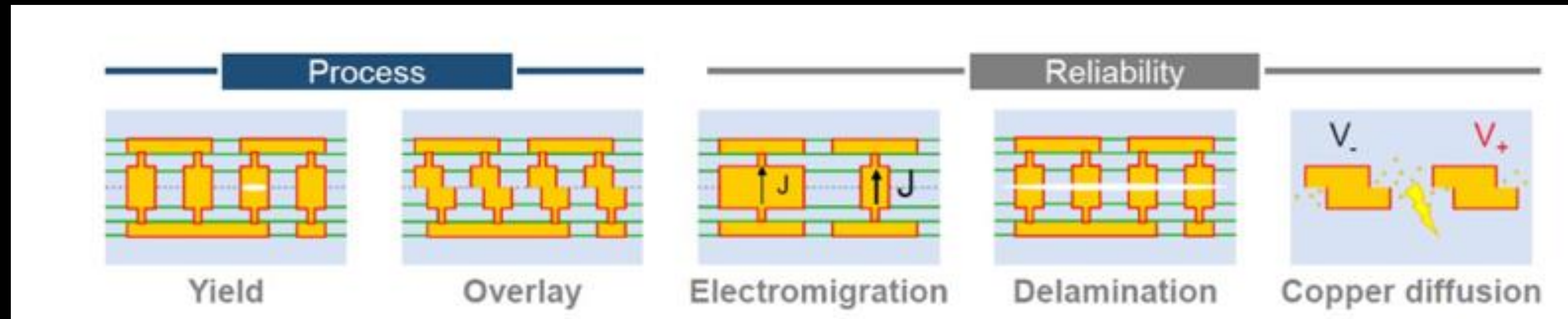
- KGI for C2C interconnect using Fan Out Wafer level RDL process
- Silicon interposer with TSV/RDL connections for Passives, Connectors
- Face to Face bonding
- Molding/Underfilling coupling EIC & PIC assembly
- Manufacturing processes – Leveraging Industry Infrastructure; Scalable

Electro-Photonic Multi-Chip Module – 3D

F2F bonding - Solder



Hybrid Bonding



- EIC & PIC – Face to Face bonding
- Process selection – Higher Performance, Higher Yield and Lower cost
- Well established process for CIS and ISP

Source: 3DInCites
ST Micro

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Summary

- Integration of PICs and EICs while meeting key metrics in terms of performance, power density, cost, and thermals requires advanced packaging solutions
- Advanced packaging process that scales with the increase in interconnect density
- Extensive TM modeling is required to down select packaging processes and materials
- Thermal challenges will require solution with the requirements of cooling both the sides of the Package structure
- Packaging interconnect and Material performance in Cryogenic environment needs to be demonstrated working across the suppliers/partners

Solution Through Collaborative Partnerships with the Industry Infrastructure