Fostering a Thriving Ecosystem Around Virtuoso Technology

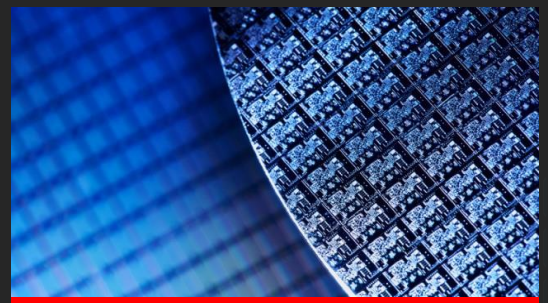
EPIC World Photonics Technology Summit – January 24, 2022

Gilles S.C. Lamant, Distinguished Engineer

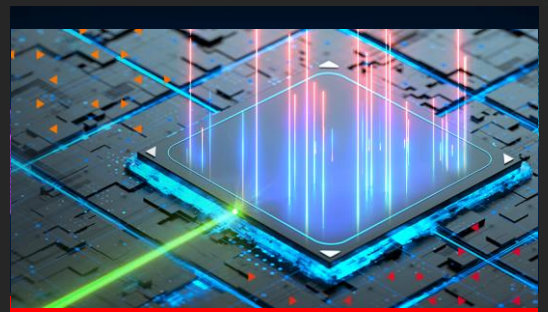
cadence®

Silicon and System First-Pass Success

Advanced-node mixed-signal IC to complex 5G solutions



Advanced FinFET Processes



Integrated Photonics

Custom IC, IC Packaging, PCB, and System Analysis

IC/CHIP	PACKAGE	BOARD	SYSTEM
Mixed Signal, Analog/RF, and Photonics			
Advanced Node (16nm to 3nm)			
Machine Learning			
System Analysis/Verification			
	Complex PCB Enablement		
	Advanced 2.5D/3D Packaging		

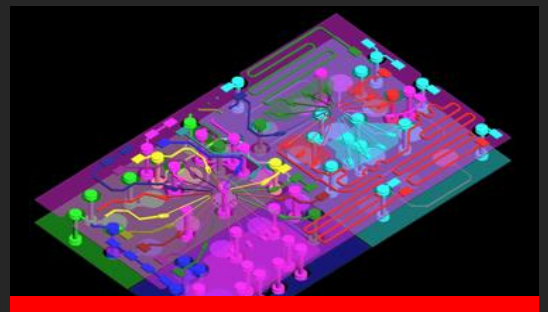
Mobile · IoT · Auto · Medical · Aero · Cloud

Vast ecosystem, +70 partners

tsmc · National Instruments · MathWorks · Ansys Lumerical · arm · Dassault Systèmes · …

Innovation Leader for 30+ Years

System Design



System Analysis

Automotive

ML/AI

Design Excellence

5G, RF, and Edge

Data Center and Cloud

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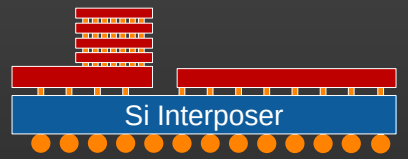
From the Chip Through to the System
Multi-Physics Analysis Portfolio

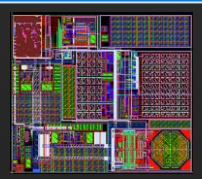
Packaging Design

2.5/3DIC



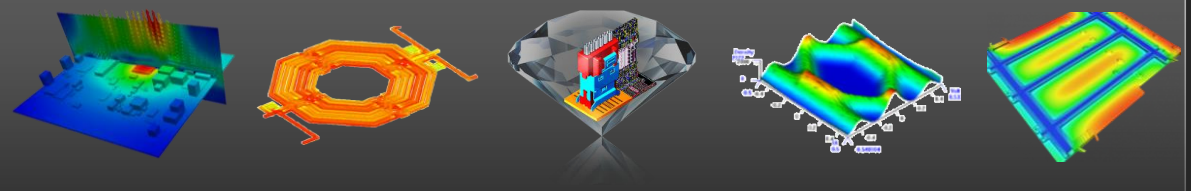
2.5D-IC (CoWoS)

IC Design

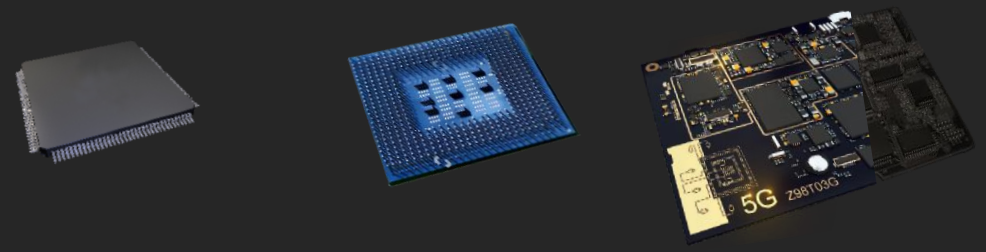


IC

Multi-Physics Analysis



Celsius **EMX** **Clarity** **Sigrity** **CFD**



System Design

Automotive

Communications

Aerospace

Electronic-Photonic Design Automation (EPDA) IC Flow

Ansys / LUMERICAL

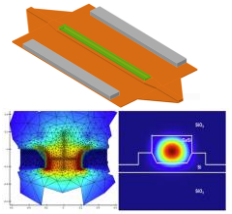
Photonic Integrated Circuit Simulation

INTERCONNECT
Photonic Integrated Circuit Simulator

CML Compiler
Cross-simulator Photonic CML Development Platform

Photonic Multiphysics Simulation

FDTD, MODE, FEEM EM Simulators
CHARGE Charge Transport Simulator
HEAT Heat Transport Simulator
MQW Multi-Quantum Well Simulator



Foundry

GDSII
Final (batch)
DRC/LVS

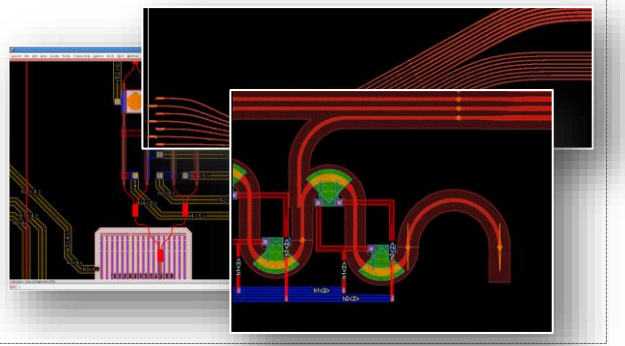
Spectre®

APS/X Simulators	AMS Designer
Electrical and Optical (Verilog-A) Simulation	Mixed-Mode Simulation

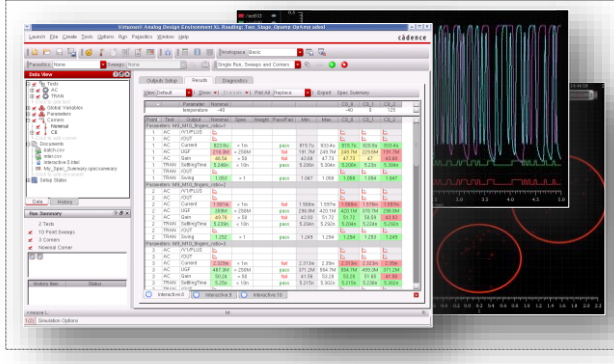
- Mask layers
- Design rules
- Symbols
- Optical and electrical simulation models
- SKILL® PCells and device-fixed layouts

PDK

Virtuoso® Layout Suite



Virtuoso Analog Design Environment



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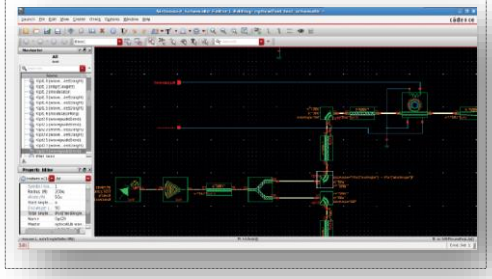
Virtuoso Schematic Editor



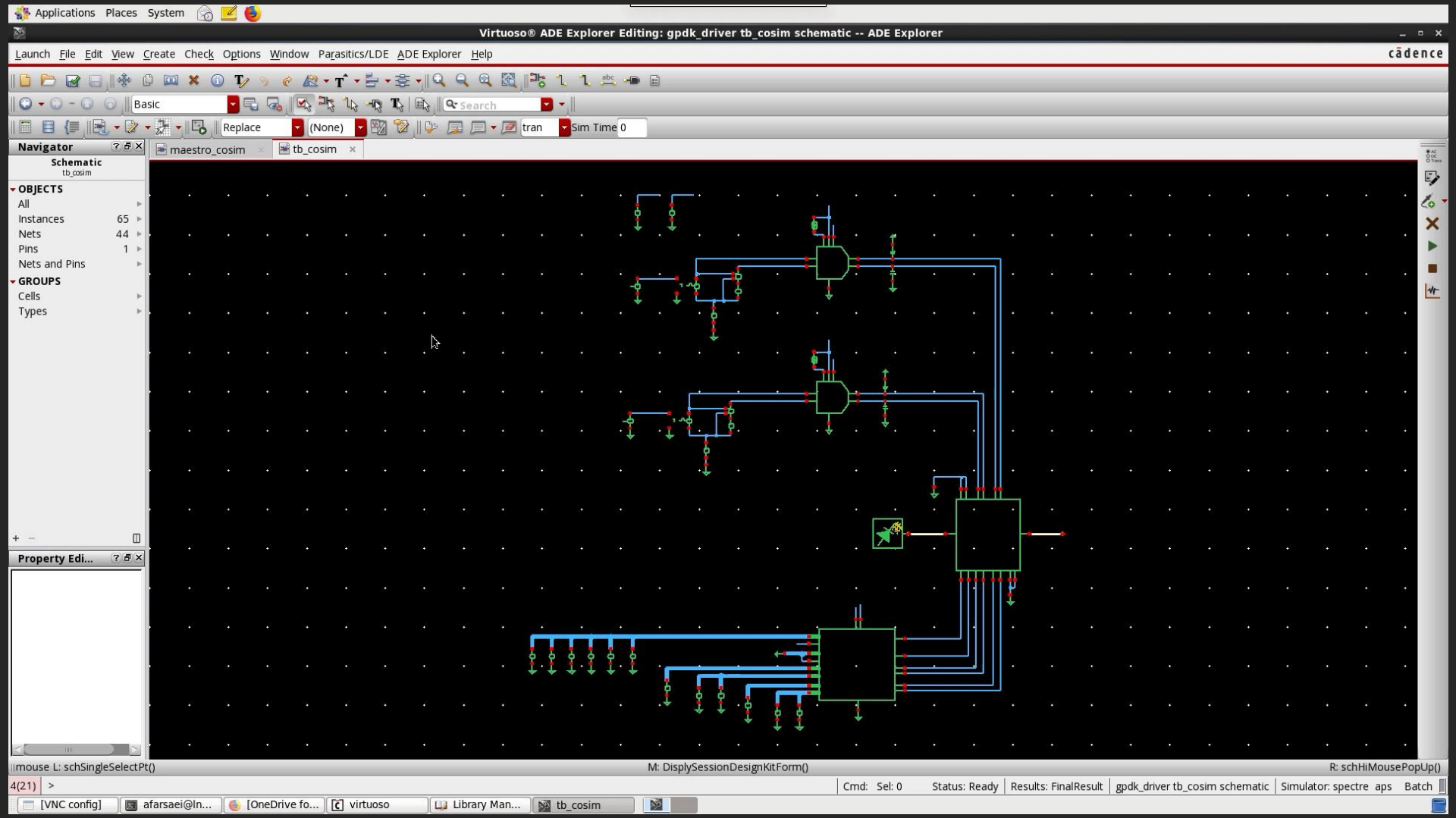
Photonics Layout Generation
SKILL or SKILL CurvyCore™ APIs

- **Symbolic curvilinear layout and discretization**
- **Waveguide creation and modal properties calculation**

Working with Foundry Partners for Wide, Accessible Enablement

- Foundries are our key partners in the past years
- They presented their PDK as well as their differentiated offering at the annual Cadence Photonics event

Collaboration to Enable Truly Unique Design Environment
(Combining the best in kind…)



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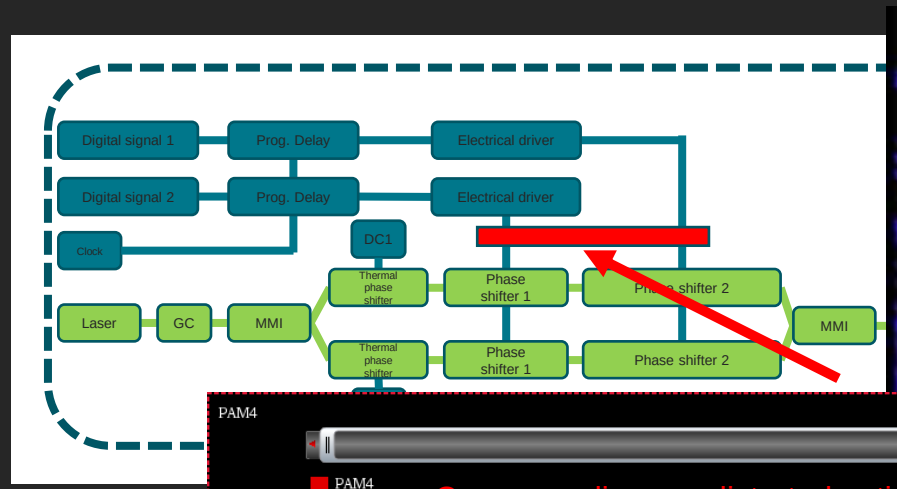
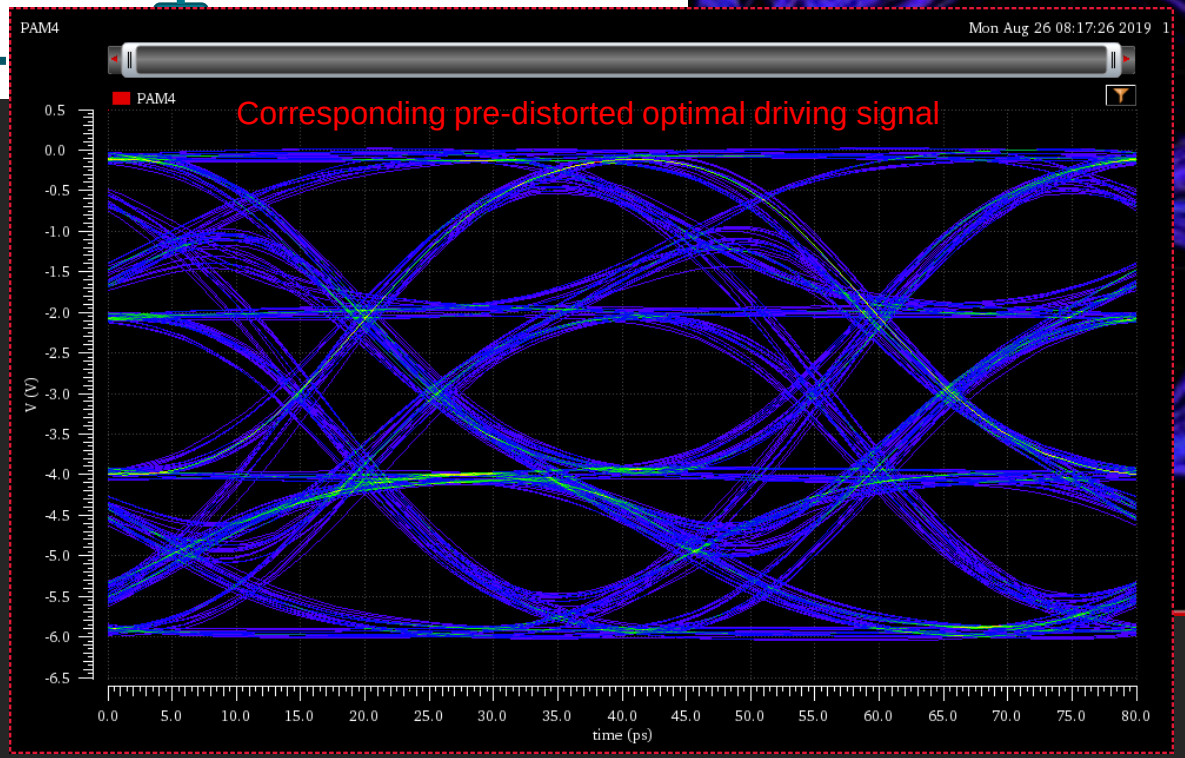
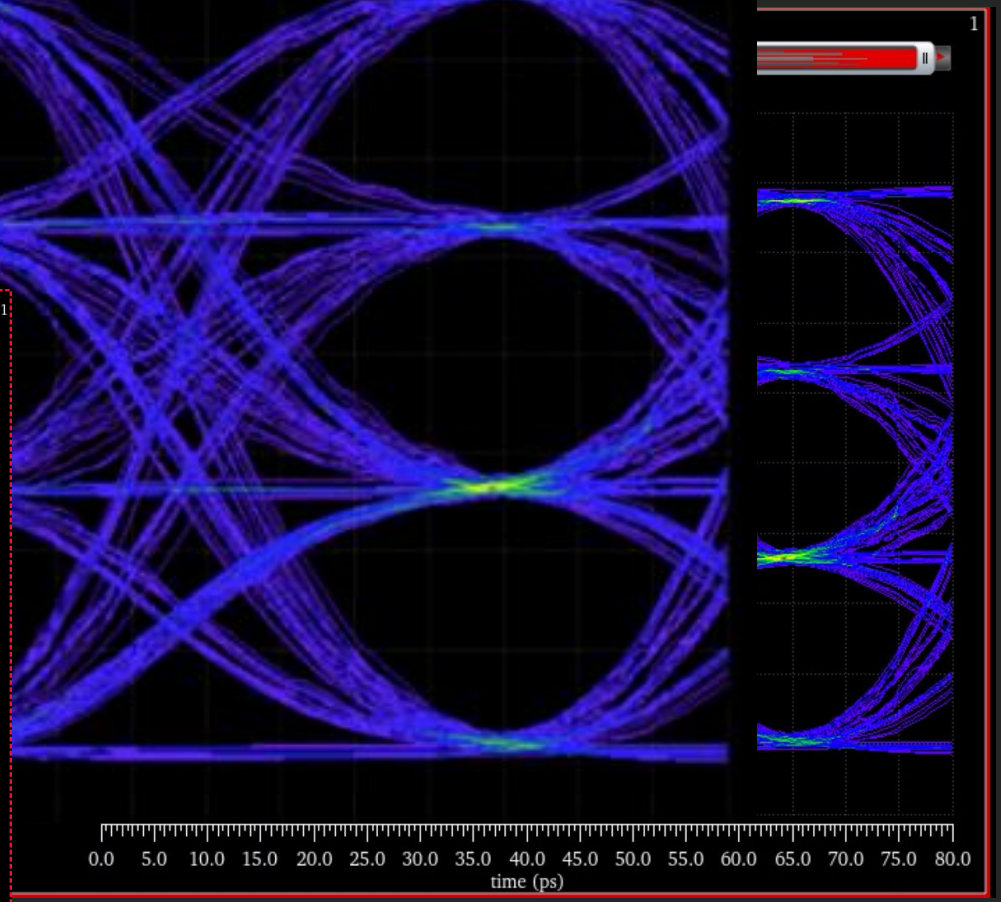
Collaboration to Enable Truly Unique Design Environment

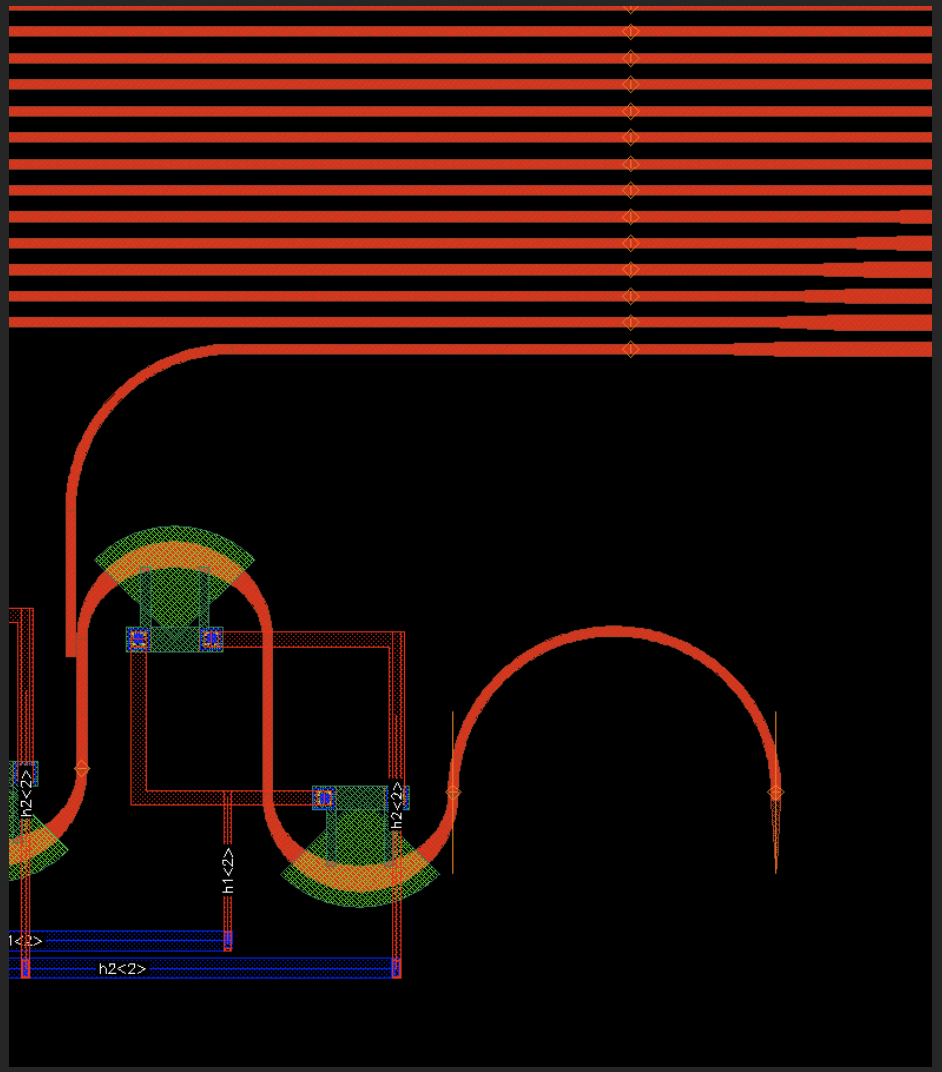






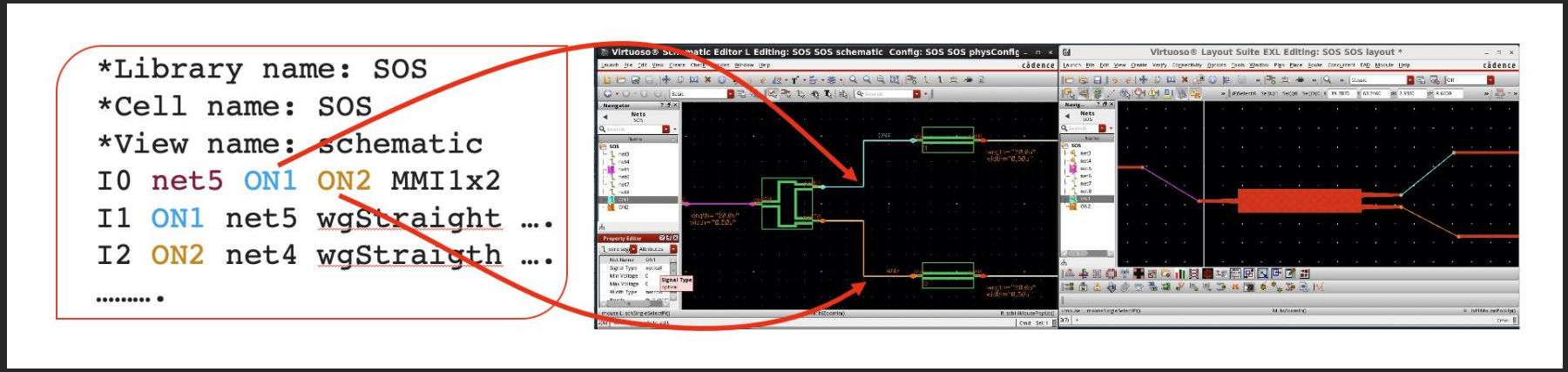
Integrated Where It Matters!

- Cadence CurvyCore™ technology is the native curvilinear engine for the Virtuoso® Design Platform (in production since 2018)
  - Tower, GF, AIM, CTek... PDKs
  - IDMs
- Supports both Interactive or API driven design flows (or a mix)
- Built above base Virtuoso platform – inherits years of flow maturity when using this known and proven environment



Continuing to Invest

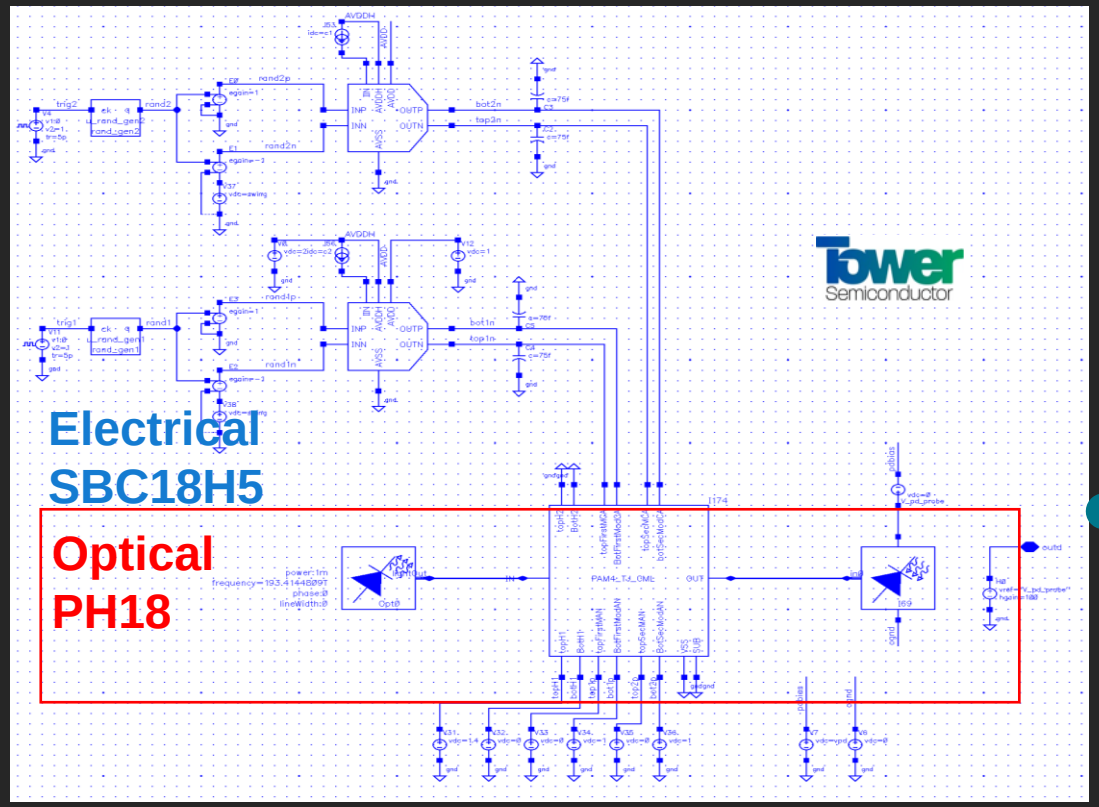
- Support for optical signal in Spectre® simulation (production end of 2019)
  - Enables matching connectivity for all representations, even though optical signals can be represented by very complex, multi-quantities (TE Img, Real, forward, backward, TM, and so on) in the model
  - Key enabler for EPDA / schematic-driven flows
  - Works with Verilog-A or Spectre models

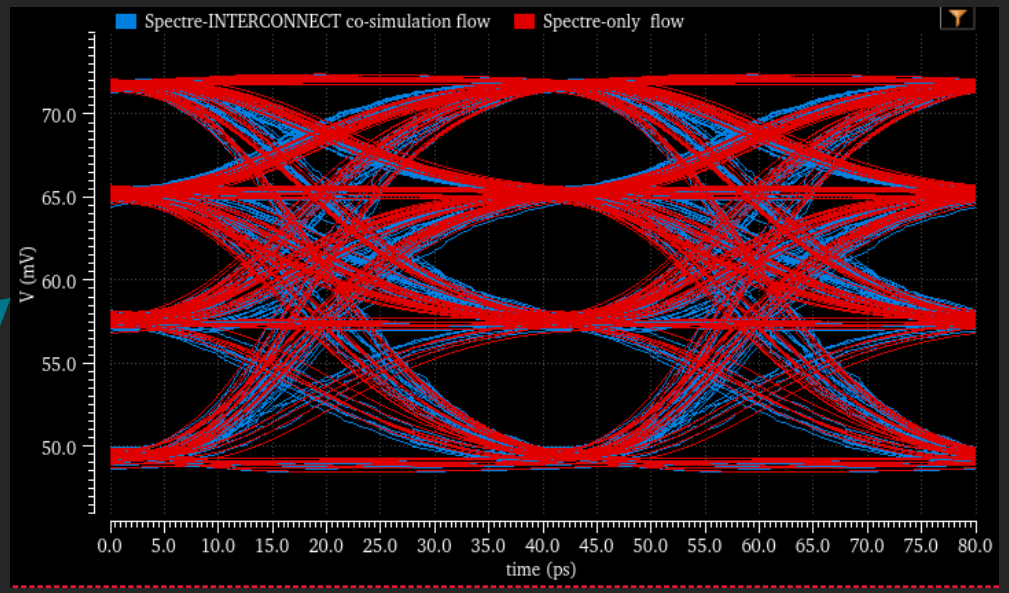


- Compatible with Lumerical CML Compiler models

Working with Foundries to Validate Models and Model Strategies

Results presented at CadenceLIVE™ Americas 2021 (ANSYS/Lumerical and Tower Semiconductor)





	Spectre®-INTERCONNECT flow	Spectre-only
Electrical element models	SPICE	SPICE
Optical element models	INTERCONNECT	Photonic Verilog-A
Simulation Time	612.4s	237.5s
Extinction Ratio	1.55dB	1.558dB
10%-90% Rise Time for level0 – level3	21.98ps	21.76ps

Continuing to Partner

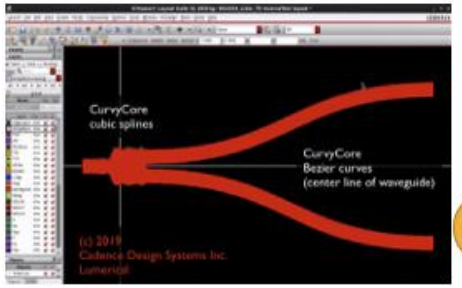
Integration for component design

Design Challenges:

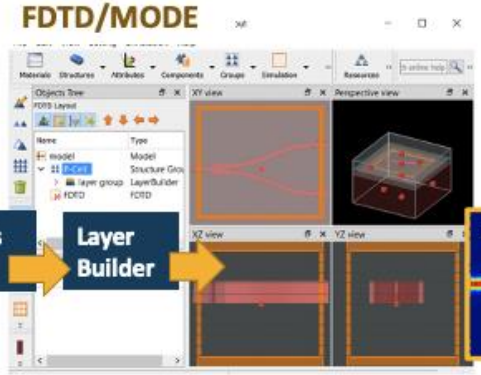
- *Users need to define layouts in both layout editor and FDTD/MODE solvers, which is time-consuming*
- *Inconsistency between two layouts is difficult to resolve*
- *Exporting GDS to FDTD/MODE does not support parametric analysis*

Goal: *Facilitate component design through direct integration with Virtuoso Layout*

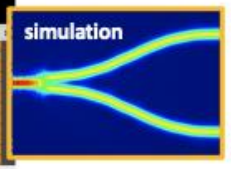
Virtuoso Layout Suite



FDTD/MODE



Analysis Group → **Layer Builder**



Direct bridge

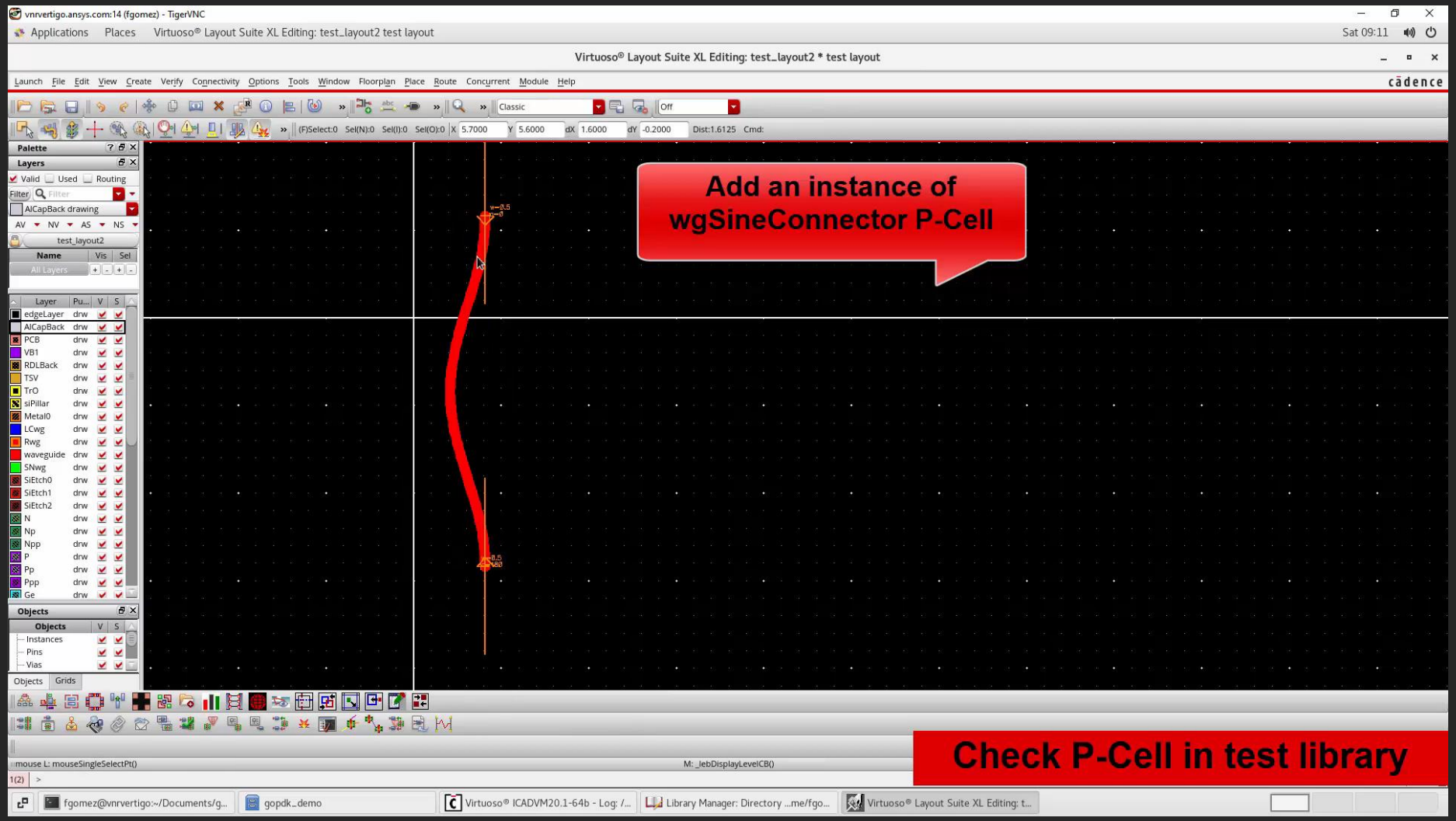
Communicate layout data between Virtuoso and FDTD/MODE

- *Query properties of fixed and parameterized cells*
- *Obtain polygon vertices for given parameter values*
- *Easy optimization of P-Cells*

Ansys

Reproduced with permission from Ansys/Lumerical

Continuing to Partner



Parting Words

- Need to include thanks to the Lumerical team, which has graciously contributed to this presentation to show a more complete picture
- Cadence is very engaged both at the system analysis level and the PIC level, driven by the requests from our customers
- José always asks how we can help each other
  - I am interested in working with a SiN foundry to enable a commercial SiN PDK
  - We work with a lot of startups (not just the big electronic firms) – talk to us