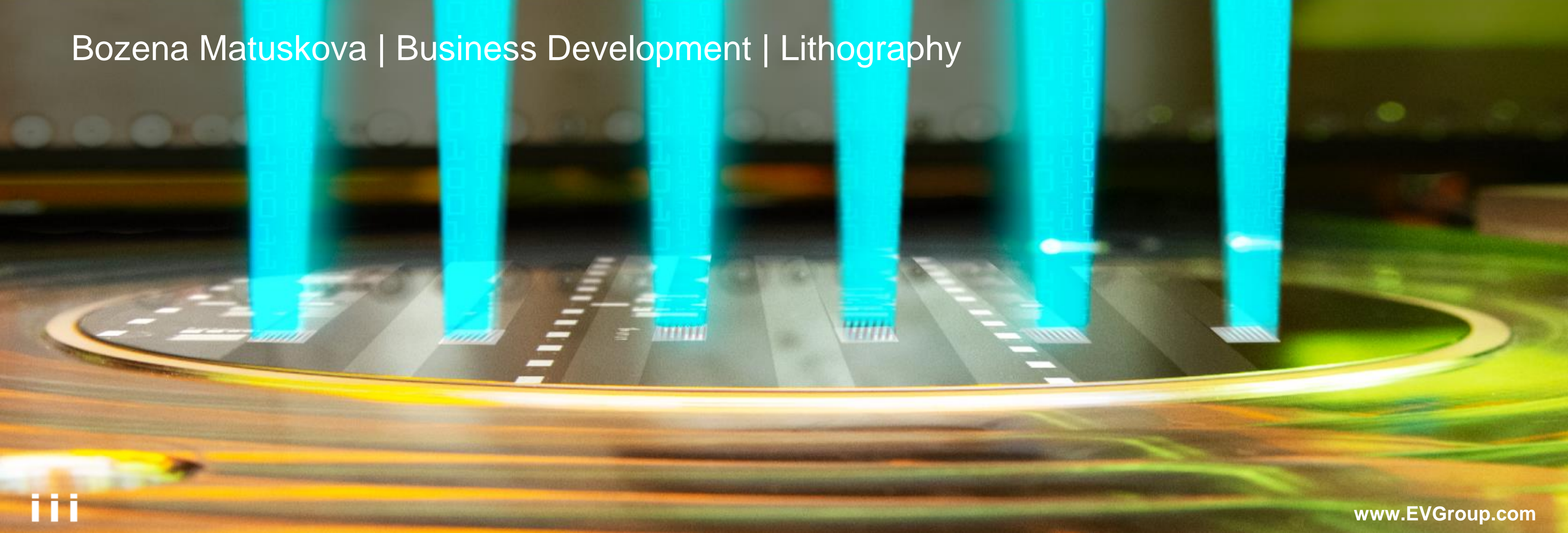
EPIC Members New Product Release

EVG

LITHOSCALE®

A milestone towards digital lithography in high volume manufacturing



EV Group | At A Glance

EVG

Leading supplier of wafer processing equipment for the MEMS, nanotechnology and semiconductor markets

Founded in 1980 by DI Erich and Aya Maria Thallner. More than 1000 employees worldwide

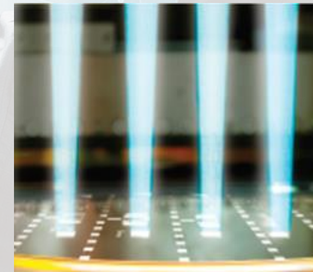
Headquarters in Austria, with fully owned subsidiaries in the USA, Japan, South Korea, China and Taiwan

Recent Developments

GEMINI® FB
Hybrid Bonding

EVG®850 DB
Laser Debonding

BONDSCALE™
Fusion Bonding



EVG® MLE™
Maskless Exposure Technology

EVG® HERCULES® NIL
SmartNIL® UV-NIL
Up to 300 mm

Motivation | Future Challenges for Backend Lithography

Flexibility

- **Fast innovation and design tape out** for improved time to market
- **Short development cycles** and immediate ramp up from R&D to HVM
- High **product mix** demands mix and match with minimal retooling time
- **Flexible dynamic patterning solution** with high depth of focus and high resolution
- **Confidentiality** of new designs

Scalability

- Patterning of **various substrate sizes and materials** such as mold, silicon or laminates
- **Adaptability to high substrate stress**, bow and warp

Cost of ownership

- High throughput with low resolution
- Low consumable cost
- High mask cost for different chip designs and mask inventory management

MLE™ Maskless Exposure Technology | Transforming Idea to Reality

EVG

Concept

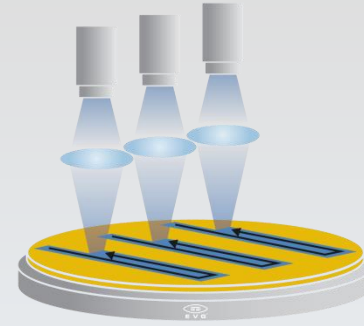
- Real-time layout processing & patterning
- Exposure of individual stripes
- Fine sub-grid address for smooth edges
- Scalability by adding/ removing exposure heads in substrate sizes from wafers to panels

Advanced Alignment Capabilities

- VIS top-side alignment & backside alignment for enhanced compensation features
- Individual alignment capabilities throughout the wafer surface

Mask-less flexibility & agility

- High product-mix variation improving CoO values
- Agile smart processing & design mix
- Consumables-free technology



Parameter	Specification
Exposure Source	HP UV - Laser Diode (LD)
Exposure Spectrum [nm] (single or mixed)	375 nm 405 nm
DoF [µm]	24 µm
Substrate Sizes [round/ square]	up to 12“
Wafer layouts [formats]	GDS II (standard) Gerber, OASIS, ODB++ (optional)

MLE™ | Highlights & Unique Values

Compensates

- Mechanical die placement and stress induced inaccuracies via adaptive registration
- High order substrate deformations, e.g. thick wafers glasses and organic substrates

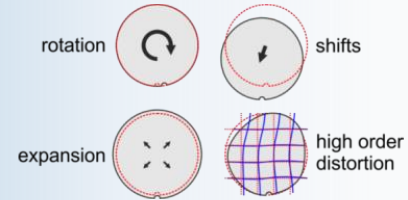
Enables

- Individual die layouts (serial numbers, encryption keys)
- Die & wafer level design patterns
- Mix & match with minimal switch-over
- Seamless stitching
- Contactless WEC and surface scan

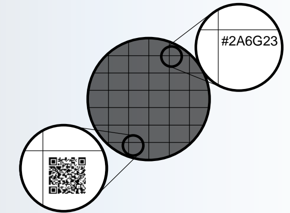
Delivers

- In-line capability, long lifetime, cost-efficient light sources
- Mask-less flexibility
- Large, small, non-standard, multiple wafers or rectangular substrates (panels) for a multitude of processes

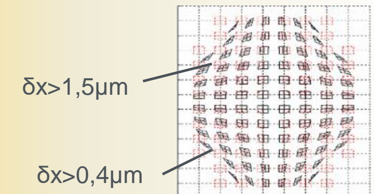
High-order, placement, scaling error corrections



Die-level annotation, serial numbers

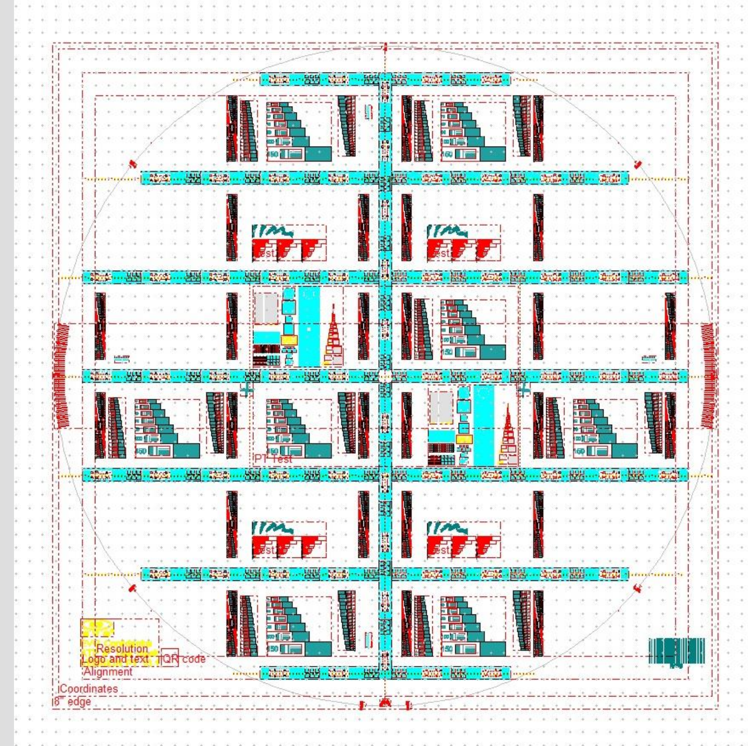


Bow substrates, surface in-variations



LITHOSCALE® | Wavelength vs Dosis vs Focus Exposure Matrix

- **Numerous process conditions tested at once & in real environment**
- **User defined & can vary for each material**
  - **dose steps vs wavelengths**
    - **Dose** range variation:
      - 50mJ – 4000mJ
    - **Exposure wavelength** range variation:
      - 375 nm
      - 405 nm
      - 375 + 405nm (broadband: 100% / 100%)
      - or any kind of mixture (20% / 80%, ..)
  - **dose steps vs focus position steps**
    - Dose range variation:
      - depends on first matrix result
    - Focus position range variation:
      - -12 .. 12µm



EVG test layout example

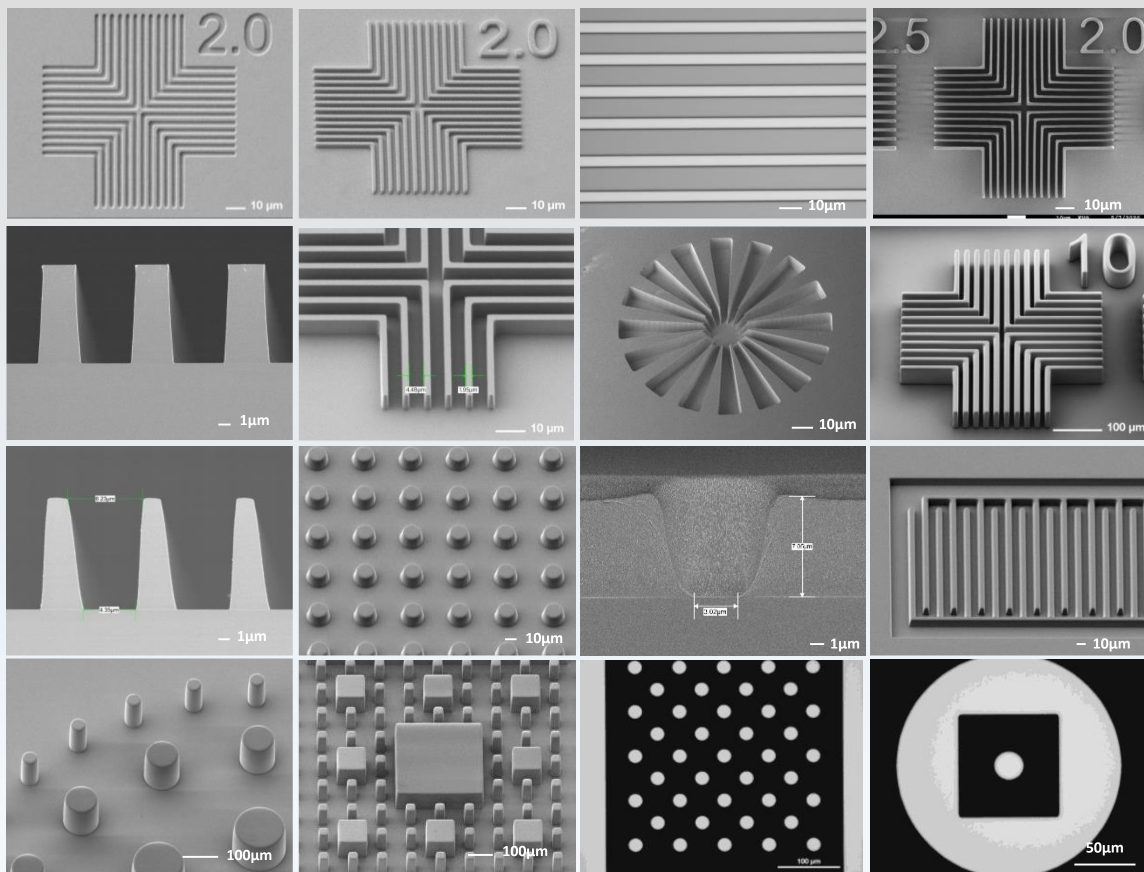
→ Alignment pattern

→ Test structures: *round, square vias*

→ Standard L/S variation test pattern

→ Various additional test patterns: *siemens star, taper*

LITHOSCALE® | Applications & Process Results



Thin Resists

→ Fine-line RDL structuring, Lift-off applications

- Pos. AZ MIR 701, LT: 1µm
- Neg. AZ nLOF, LT: 2µm
- Pos. AZ 12XT, LT: 10µm
- Pos. Sumitomo, AR 3.5:1, 7:1

Thick Resists

→ Bumping, core-line RDL structuring, high AR

- Pos. TOK P-W1000T, LT 8µm, AR: 4:1 sidewall angle: 87°
- Neg. JSR THB 151N, LT 50µm, AR 5:1

Dielectrics

→ Buffer layer for stress & thermal optimisation

- Pos. JSR WPR5100, LT 7µm, AR 2:1 sidewall angle: 82°
- Neg. FUJIFILM LTC Series, LT 7µm, AR: 2:1

ORDL, Photonics, MEMS Applications

→ Photonics packaging, MEMS, coloured resists

- Neg. SU-8 GM1075, LT 100 – 600µm
- Neg. Black resist (FFEM), LT 1 – 6µm

LITHOSCALE® | Executive Summary

E V G®

Mask-Free Manufacturing

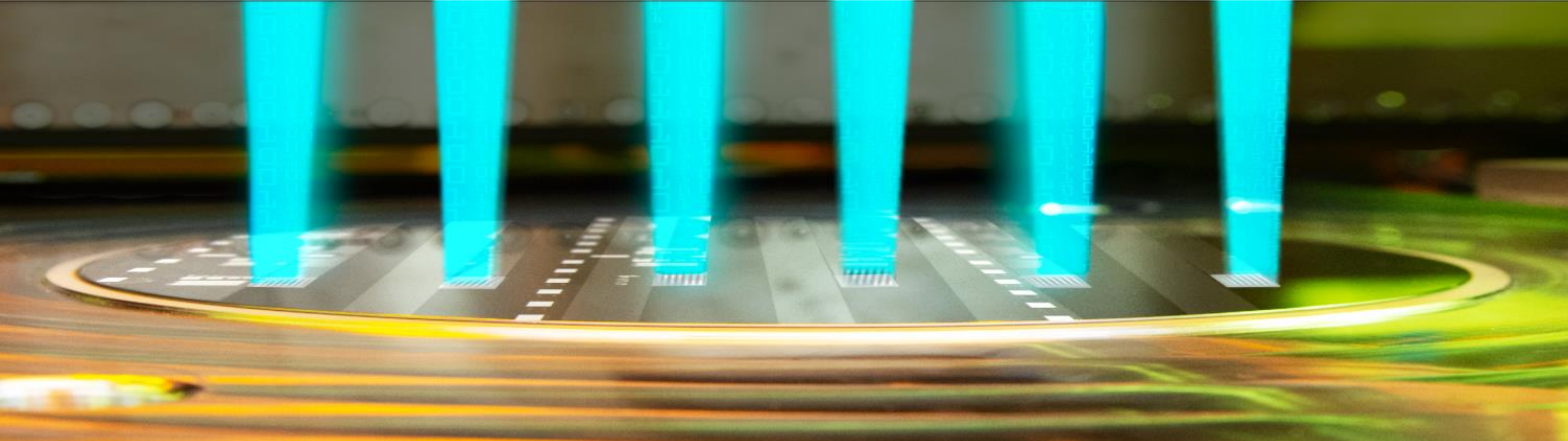
- High product variation
- Agile processing & design mix
- Digital infrastructure
- Low cost multi design logistics
- Consumables-free technology

Individual Die Processing

- Exposure of individual stripes
- Small raster size for smooth edges
- Grayscale intensity modulation
- Dynamic die annotation

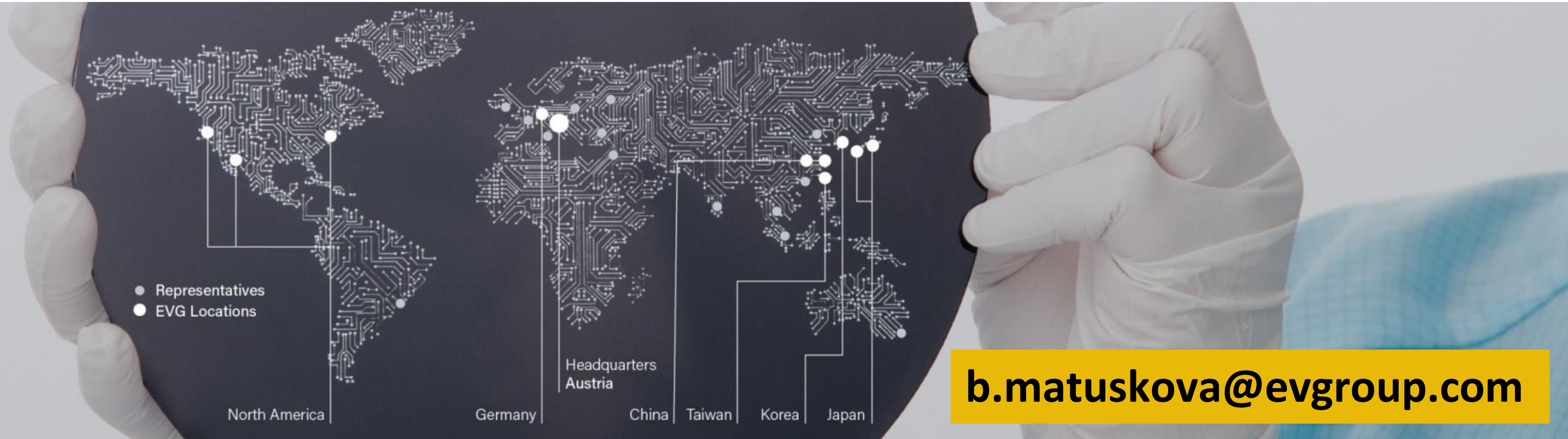
Fast Full-Field Positioning

- VIS, top-side alignment, nIR backside alignment for interposer, advanced packaging and MEMS processing
- Scalability in substrate sizes from wafers to panels



Thank you for your attention.

Bozena Matuskova | Business Development | Lithography



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