



Assembly & Test

ALEXANDER JANTA-POLCZYNSKI

SENIOR ADVANCED PACKAGING ENGINEER

ajantapo@ca.ibm.com



North American Assembly and Test Provider

Packaging & test solutions

- Advanced Flip Chip & Photonics
- Any wafer source
- “Masters of Complexity”
- Outstanding characterization
- Design for manufacturing/Test
- OSAT > 40 yrs of experience



850K square feet **manufacturing facility**

Certified “Trusted Source”


Market Segments



HPC



Aerospace
Defense



Networking



Medical

Advanced & Complex Package

- Design → prototypes → HVM

Efficient & Effective Production

- Low/High Volume
- High mix environment

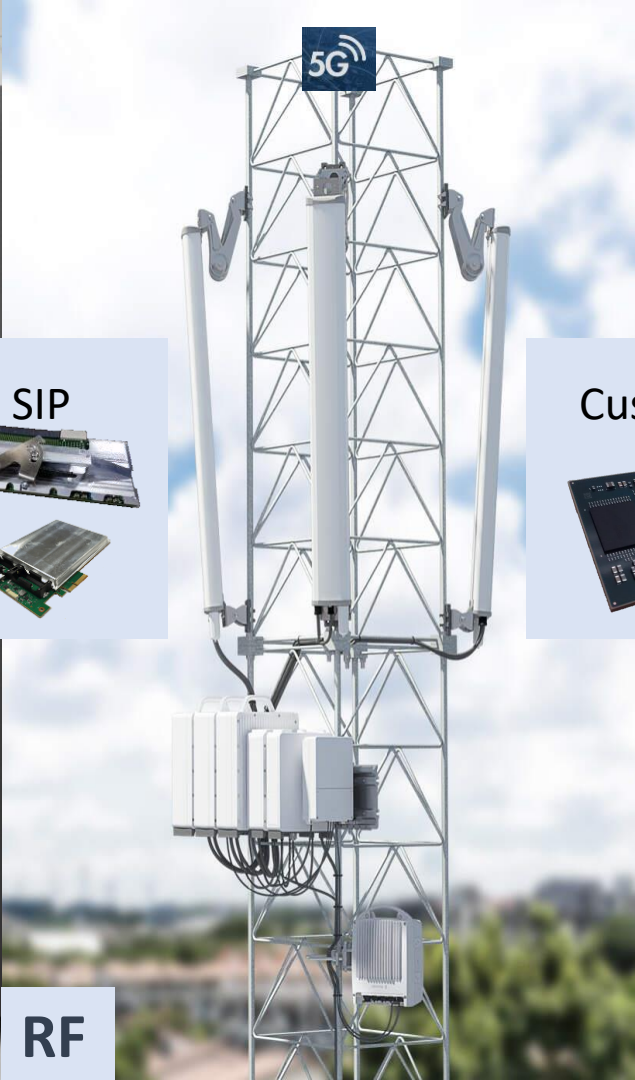
Better Time to market



161K square feet dedicated **development facility (C2MI)**



Mainframes



RF



SIP



Datacom

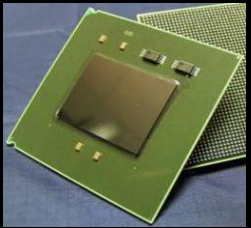


Custom

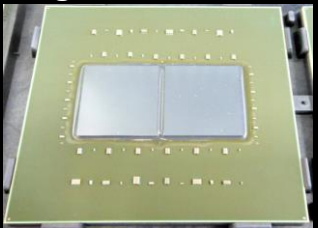
IBM Bromont – Advanced Packaging

Heterogenous integration of various node function in SiP

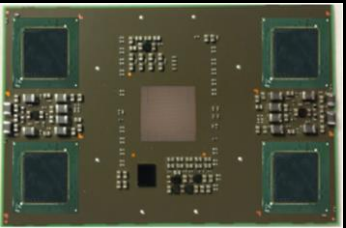
Large MCM



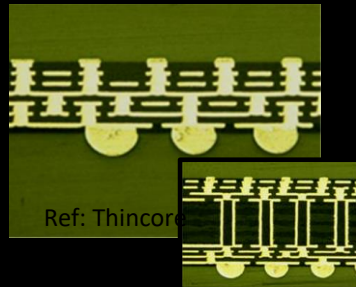
Large SCM/DCM



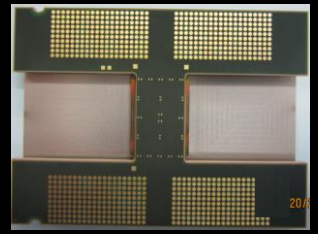
MCM - HI / SiP



Coreless



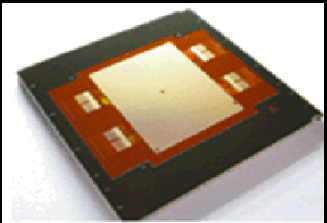
Custom



CSP



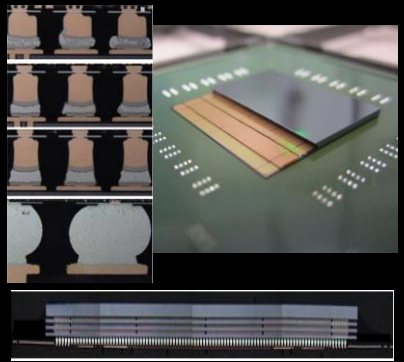
2.1D/2.3D



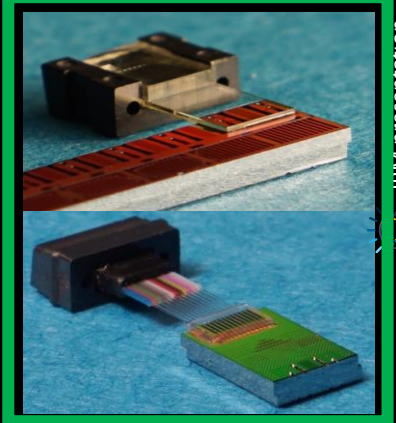
2.5D



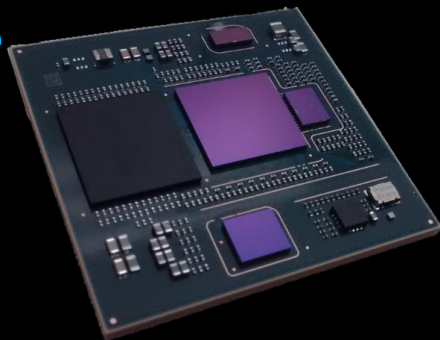
3D



Photonics



System in Package



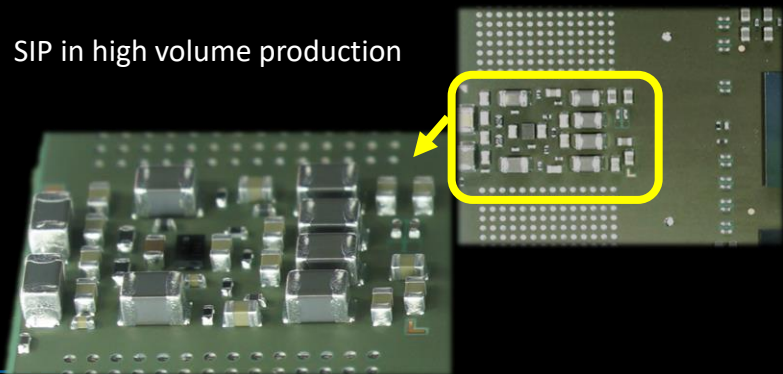
FC-PBGA SIP solutions

Board level integration
→ Cost reduction

Mixing device technologies at package level provides:

- Very close die & components positioning
 - Higher bandwidth and lower power
 - Better signal integrity
 - Smaller system level footprint
 - Modularity for cost savings
- Next generation component drop-in

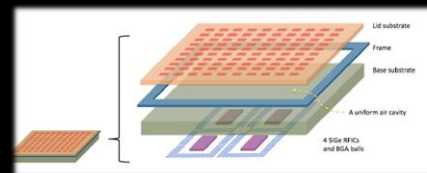
SIP in high volume production



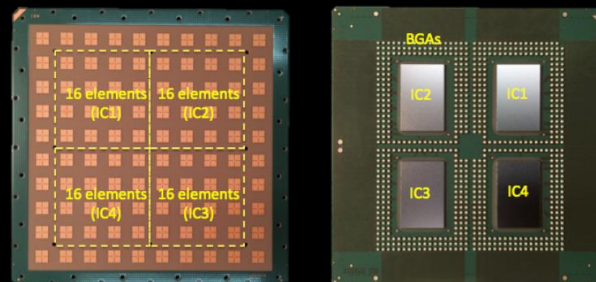
Antenna on Package

5G radio access application AoP SIP

- phased-array antenna-in-package module
- 64 dual-polarized elements
- Package size 70 x 70 mm
- Tight spacing control in assembly
- over 50dBm EIRP in TX mode
- ±40 degrees scanning range



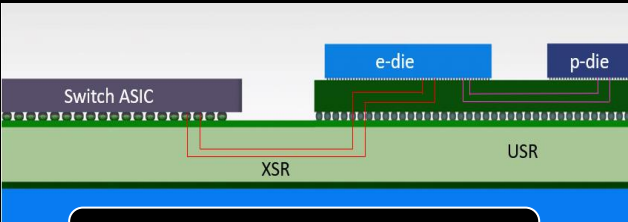
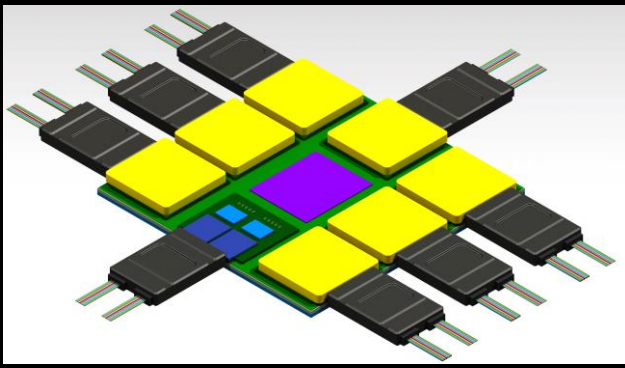
Assembled phased array with four transceiver ICs showed



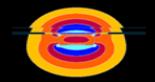
Co-Packaging – Advanced integration

Design for manufacturing & Test

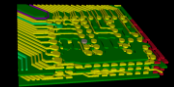
Disaggregation → Package integration
Heterogenous integration of various node function in SiP



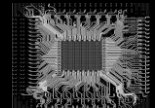
Packaging is critical for success
Co-design with packaging in mind



Simulation



Design



Substrate



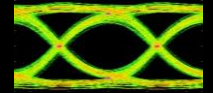
Manufacturability



Miniaturization



Optical Performance



Electrical Performance



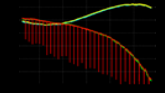
Reliability



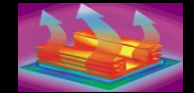
Industry 4.0



Modeling



Measure & Test



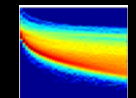
Thermal Management



CPI



Cost / yield



Predictive manufacturing



Silicon Photonic Packaging Vision

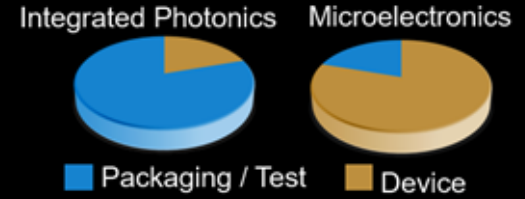
Lowering packaging cost → Increased scalability

Manual / Low volume → Automated / High volume

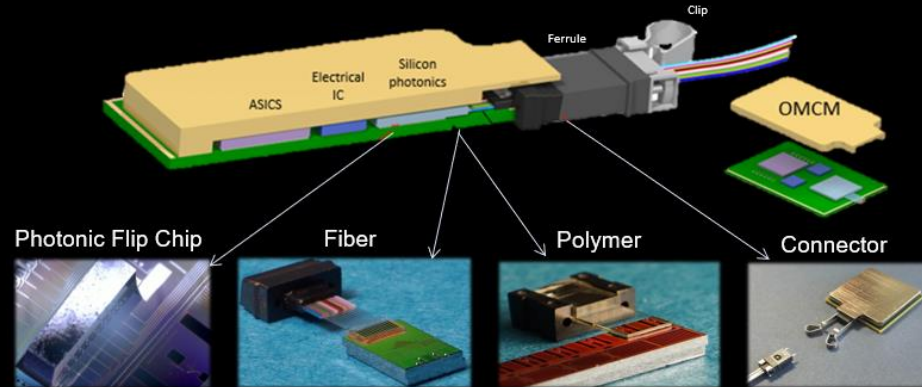
- Active alignment
- One connection at a time
- Custom design

- Self alignment
- Multiple connections at a time
- Standard design

Cost Structure

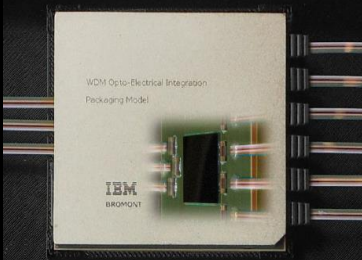


Typical 2D Multi-Chip Module package with integrated optics

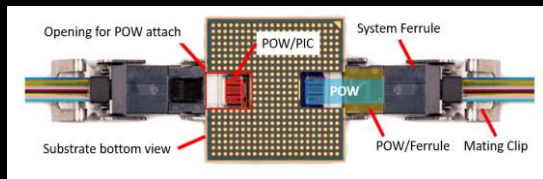


Photonic co-packaging demonstrator

High Fiber Counts Application



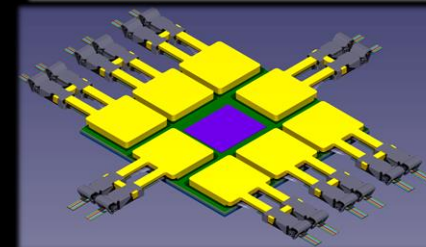
High Density Optical Port Counts Application



Integrated Connector

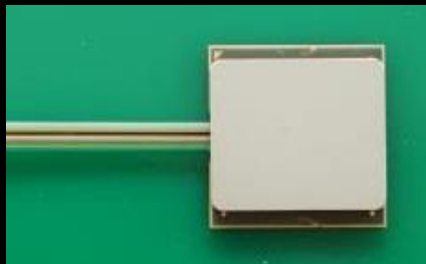


MT ferrule attached to CSOP lid
MT ferrule part of fiber cable to be plugged in

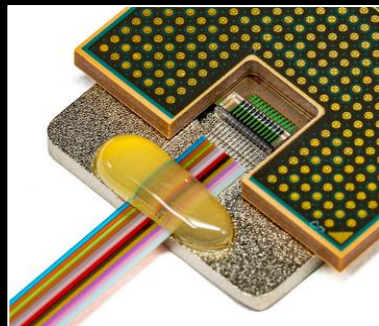


Clip installed during fiber cable plug in

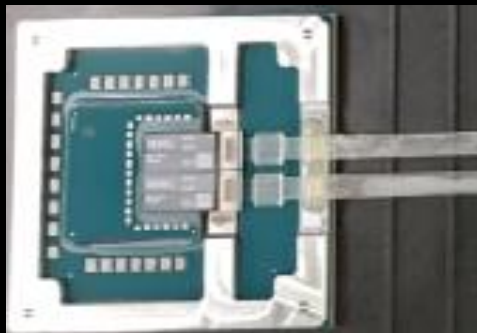
Solder Reflowable Silicon Photonics Fiber assembly



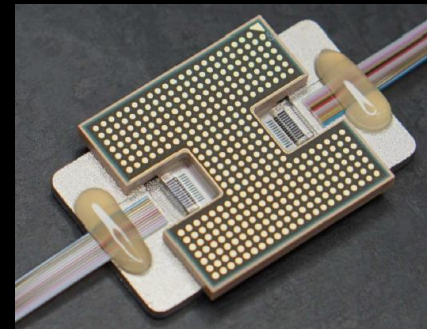
Strain Relief of fiber assembly pigtail



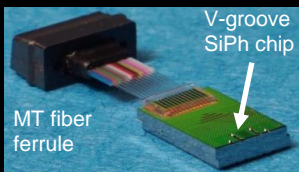
PIPES Transceiver



Full Optical Switch



Fiber Array – Single mode solder reflowable coupler

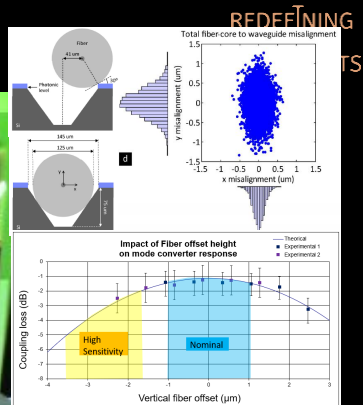
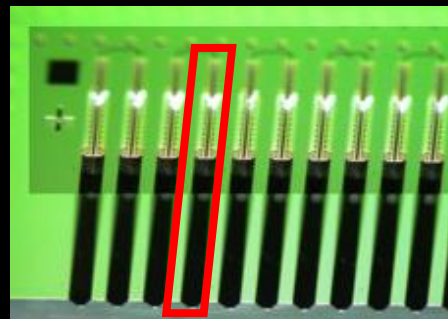


IBM design chip build at GF



Parallel channel array (12ch TV)
O, S, C, L bands compatible
Couples both polarizations (TE / TM)
High throughput pick n place tools
Solder reflow compatible (260 C)

Key to Success:
Adhesive partitioning



Integrated Metamaterial Interfaces for Self-Aligned Fiber-to-Chip Coupling in Volume Manufacturing

IEEE Journal of Selected Topics in Quantum Electronics
 Volume: 25, Issue: 3, May-June 2019

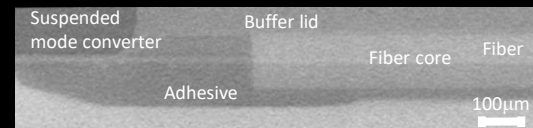
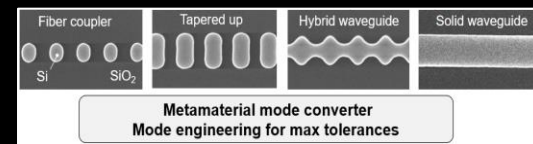
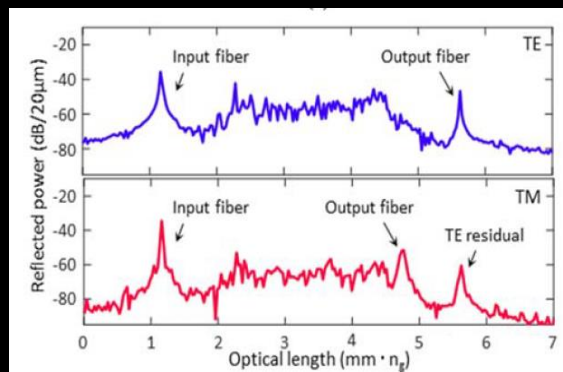
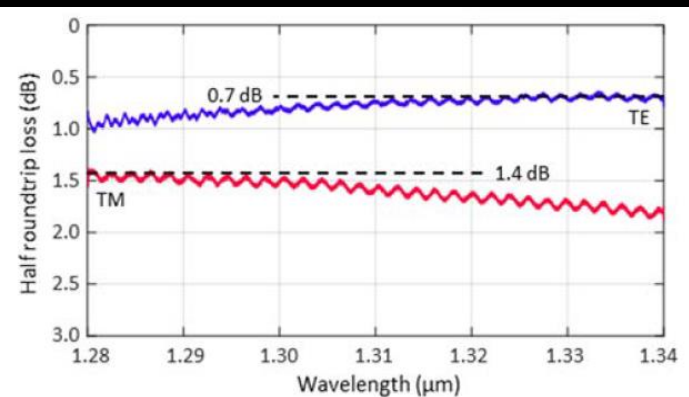


Structural adhesive for fiber

- Mechanical stability/robustness
- Fast UV tack (< 5 sec)

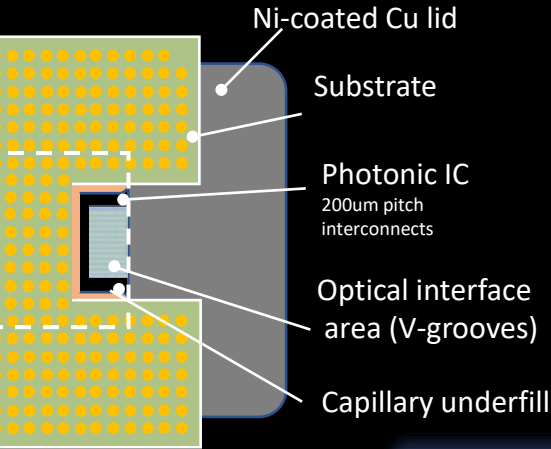
Optical adhesive for suspended region:

- Optical performance
- Reduce stress on fragile membrane

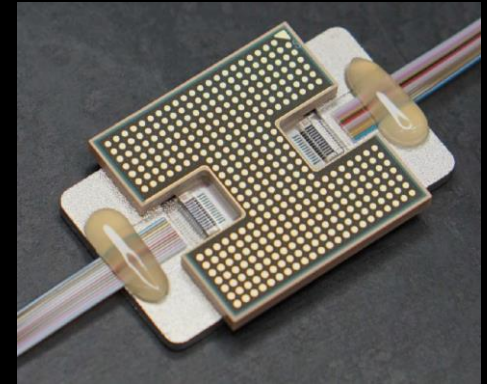
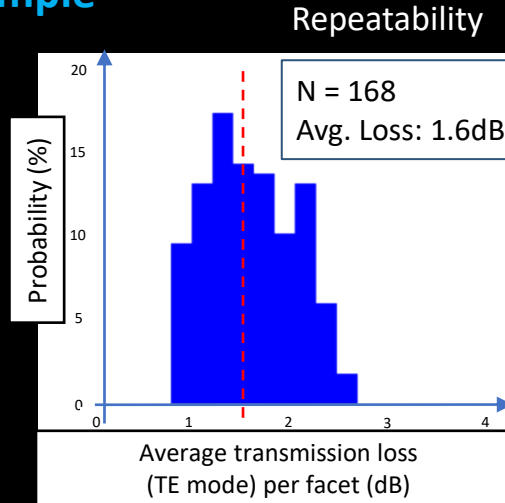


Fiber ribbon assembly in V-grooves (X-ray tomo)

Photonic Flip-Chip assembly example



Bottom view substrate side of the module



10

Formic acid flip-chip bonding

Fluxless solution required to maintain grooves/facet cleanliness and SWG integrity

Fluxless formic acid reflow with temporary adhesive material (tacking fluid)

No voiding / cracking of the IMC & solder

Formic acid reflow available at IBM Bromont



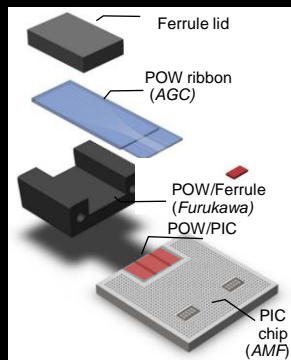
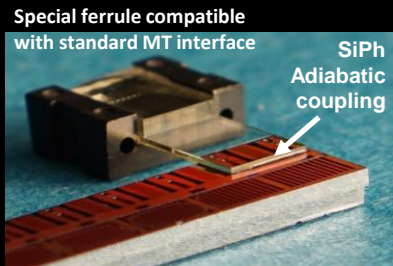
Formic acid furnace

R&D formic acid oven also available

IBM presentation



Compliant Polymer interface – Dense Single mode coupler

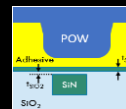
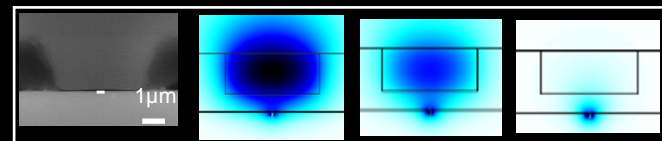
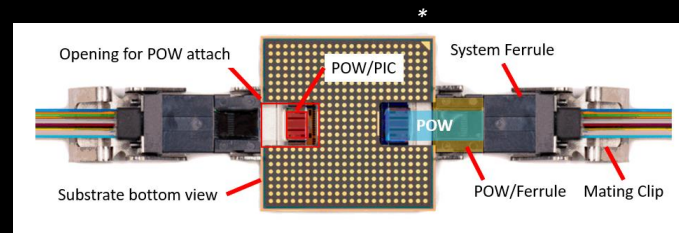
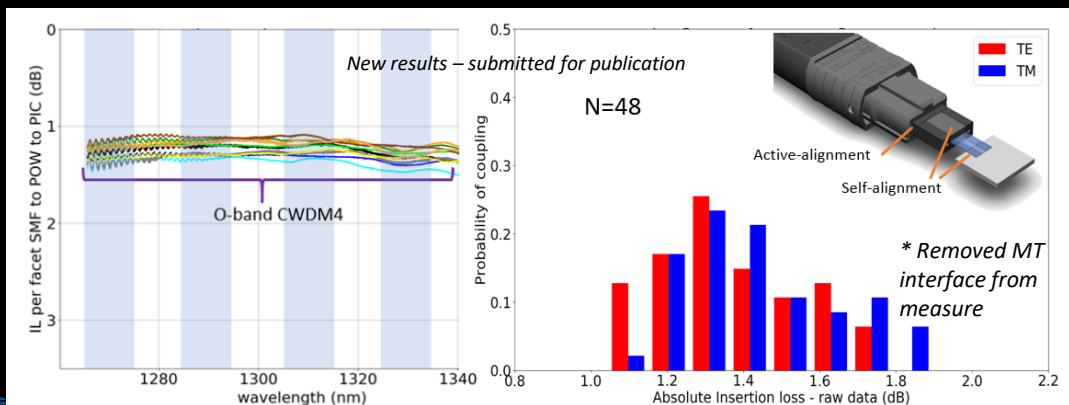


Parallel channel array (dense 50μm pitch – 12ch TV)
O, S, C, L bands compatible
Couples both polarizations (TE / TM)
Assembly using high throughput pick n place tools

- Denser pitch (up to 25μm) at chip interface
- No need for deep grooves (wet etch process)
- Mode converter structure is simple
- Compliant material for CPI risk mitigation



Advances in Interfacing Optical Fibers to Nanophotonic waveguides via Mechanically Compliant Polymer Waveguides
 IEEE Journal of Selected Topics in Quantum Electronics - 06 January 2020



Adiabatic coupling polymer/nanowaveguide



Offer

Expertise

- 7nm
- Proven material sets for high performance
- Prototyping to high volume manufacturing

Time to market

- Benefit from existing models and designs to accelerate MCM implementation
- Beyond groundrules:
 - ✓ Customization
 - ✓ Characterization

Business Model

- Co design partners
- Streamlined manufacturing flow
- Integrated supply chain

We put our packaging know how at your service
Focusing on your application and performance



IBM Packaging and Test
www.ibm.com/assembly

Thank You

We are here for you!

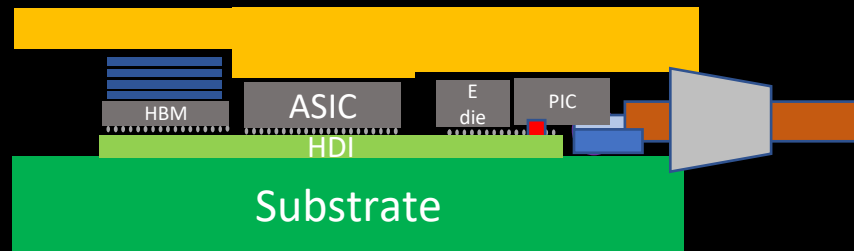


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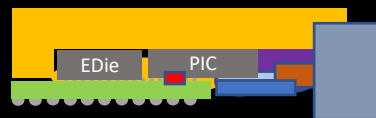


Co-packaged Optics Configuration examples

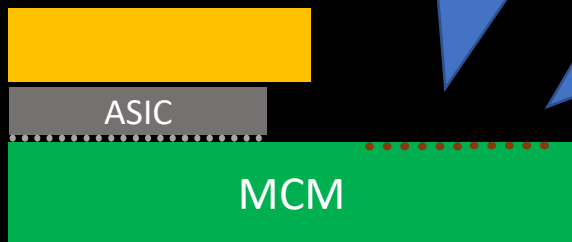
HDI with Photonics



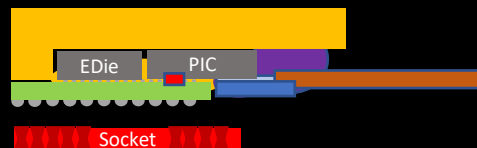
SMT / BGA reflow



CPO engine

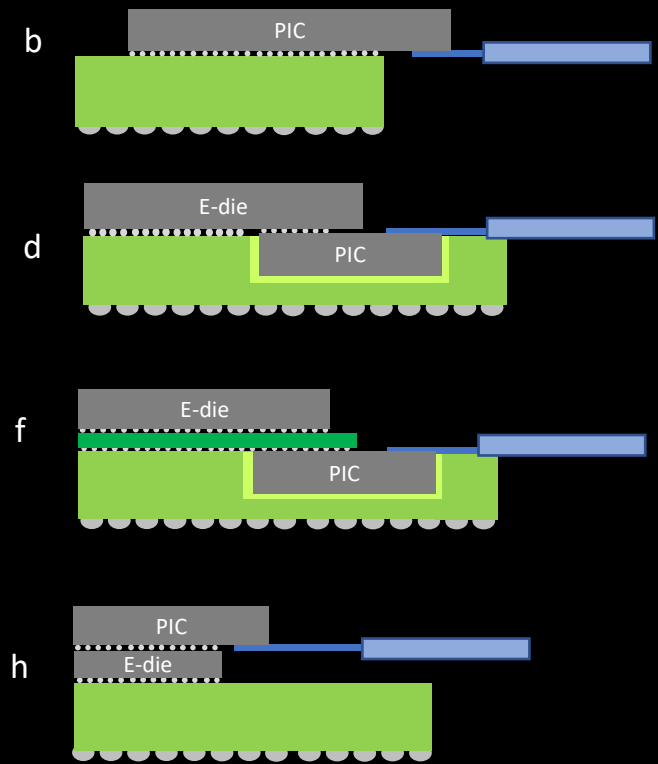
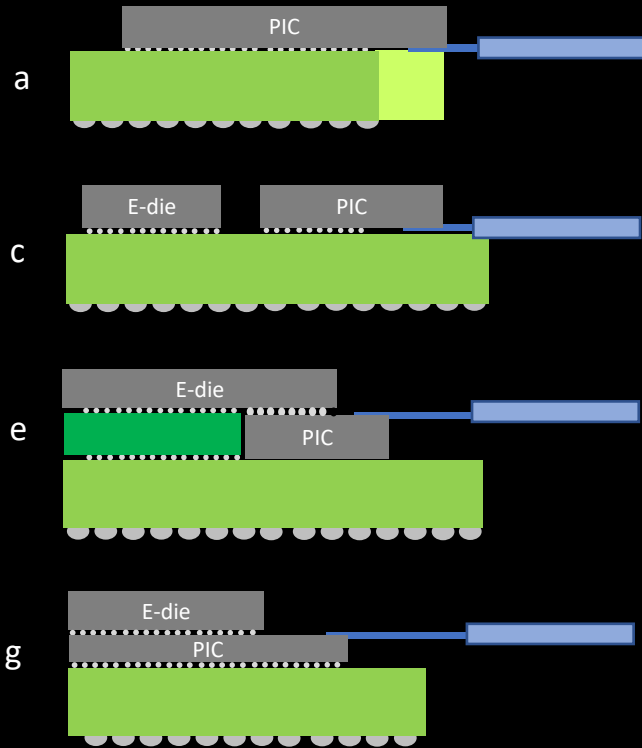


MCM with
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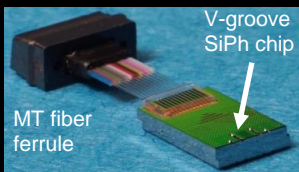


Socket / Retaining HW

Co-Packaging in Advanced integration



Fiber Array – Single mode solder reflowable coupler

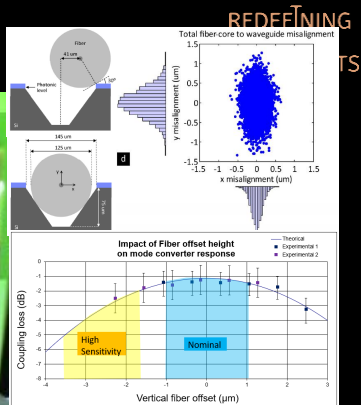
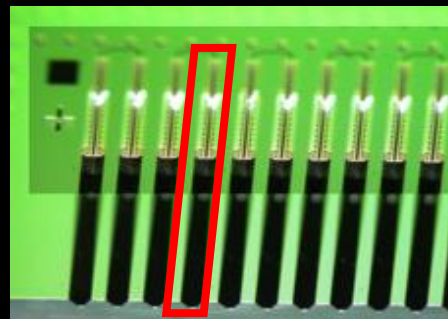


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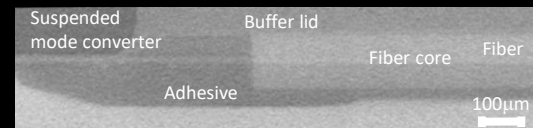
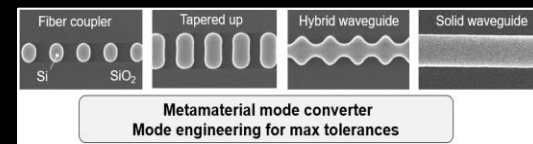
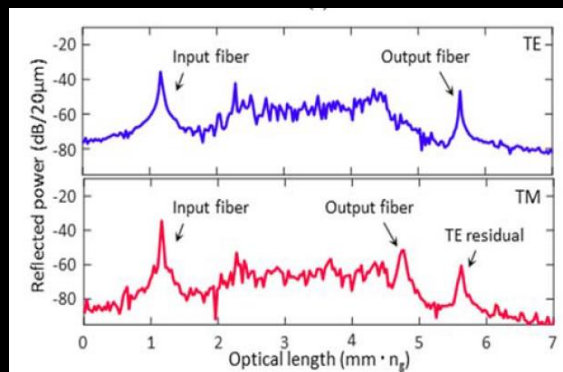
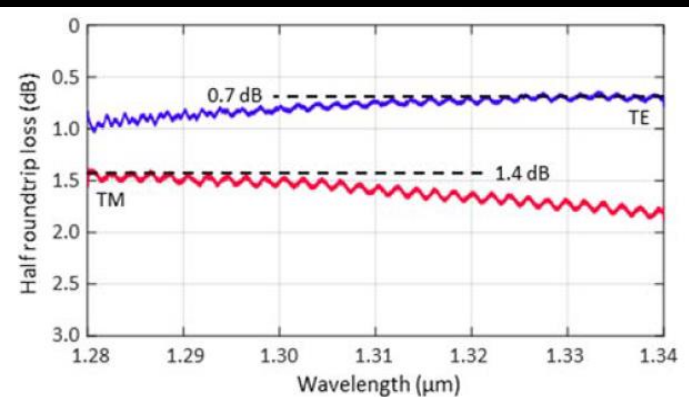


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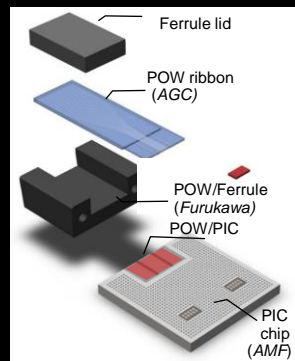
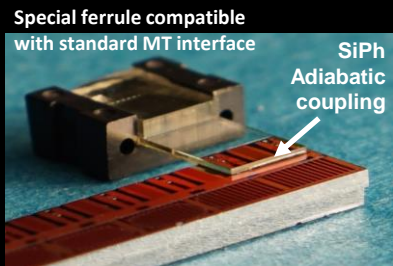
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Fiber ribbon assembly in V-grooves (X-ray tomo)

Compliant Polymer interface – Dense Single mode coupler

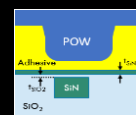
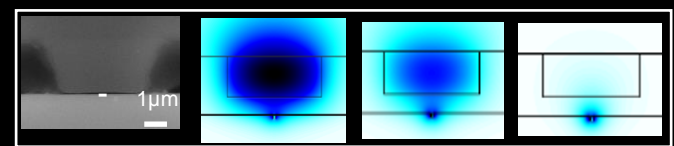
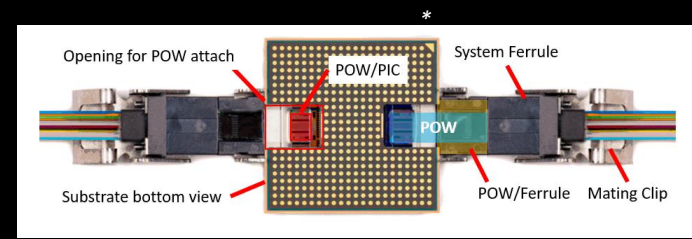
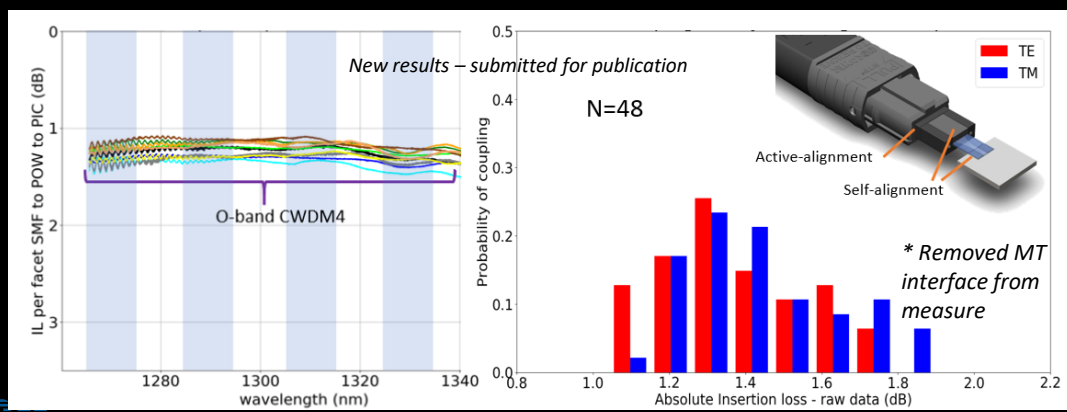


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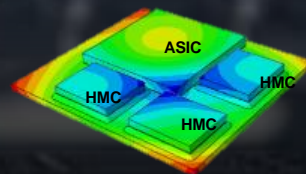
Adiabatic coupling polymer/nanowaveguide



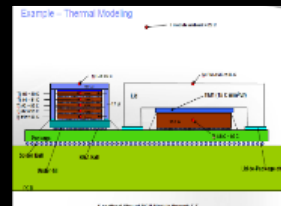
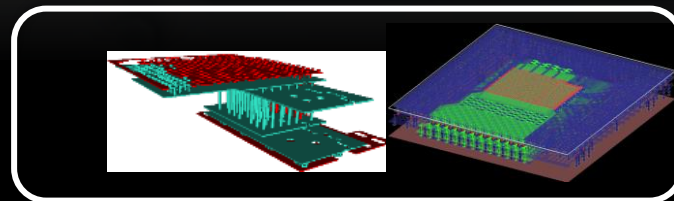
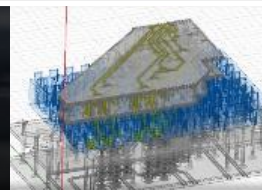
Deep capability in design, modeling, failure analysis and qualification

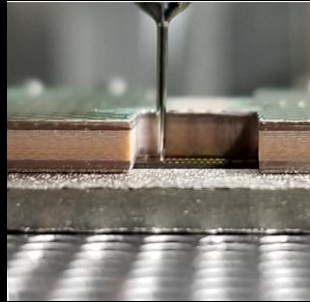
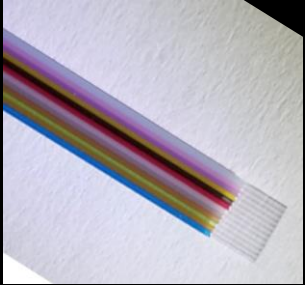
“First time right results”

- ✓ Predictive and validated [mechanical modeling](#)
- ✓ Proven [electrical modeling](#), simulation, analysis and characterization refined through empirical authentication
- ✓ Demonstrated [thermal modeling](#) capabilities confirmed through HVM products
- ✓ Innovative [photonics](#) single mode packaging and certified OSAT
- ✓ Top-of-the-industry **failure analysis** skills and labs
- ✓ Package and Product qualification services complying with reliability standards

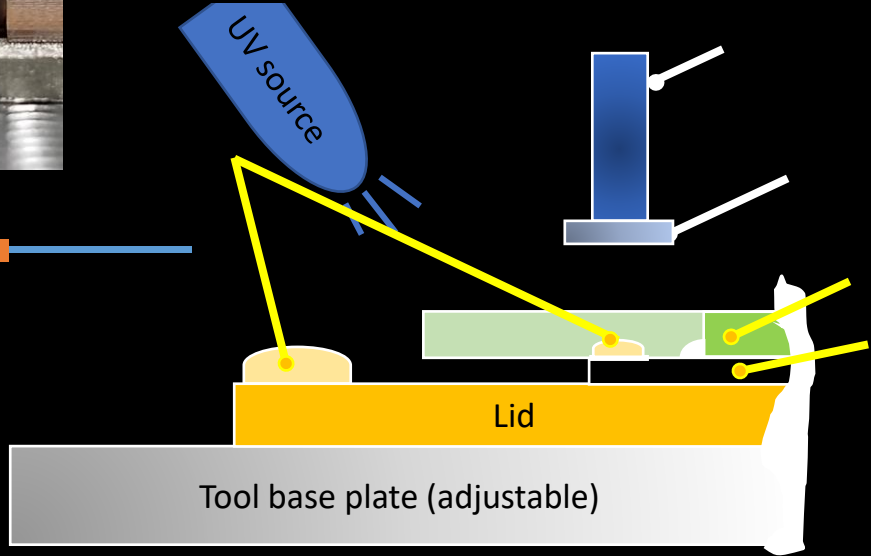


HFSS
Q3D, 2D,
SiWave
PowerSI
IBM Internal tools
Etc..

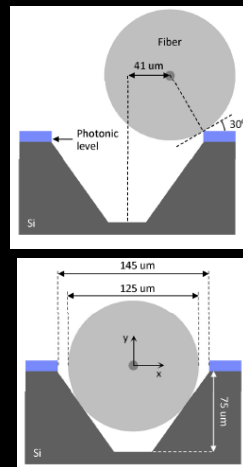
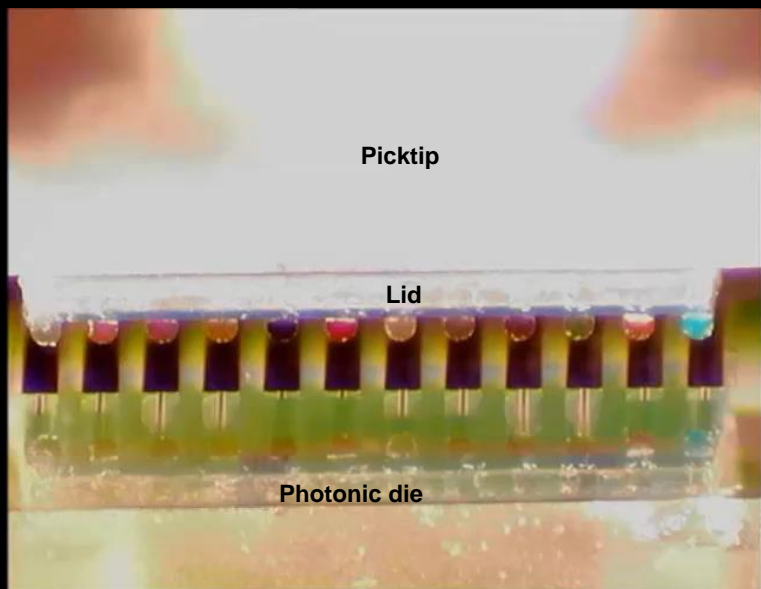




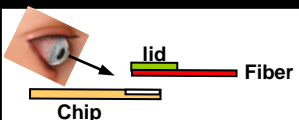
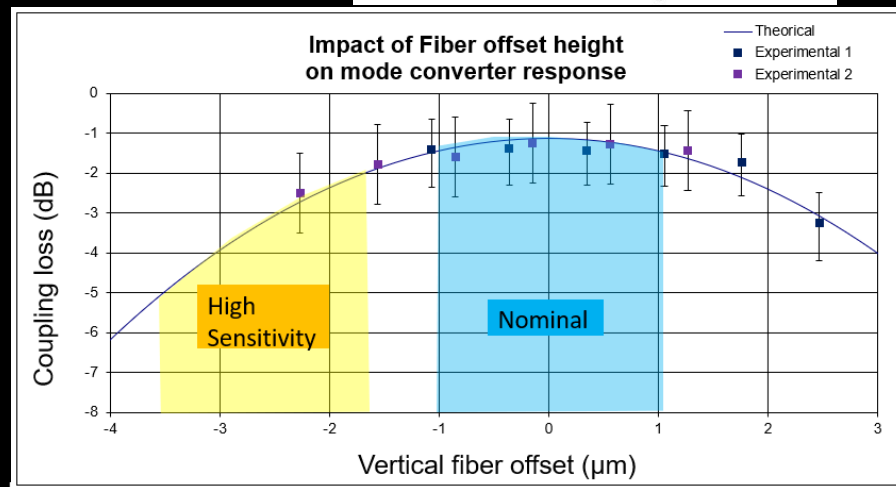
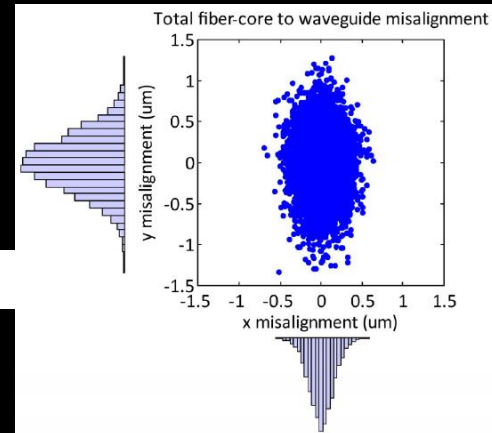
Robot handler



Fiber Array – Self-alignment

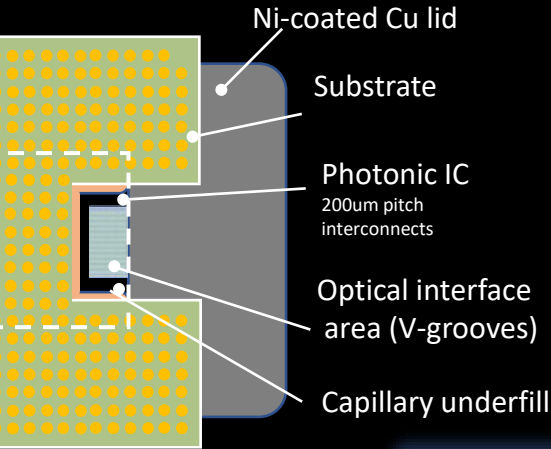


Montecarlo tolerance analysis

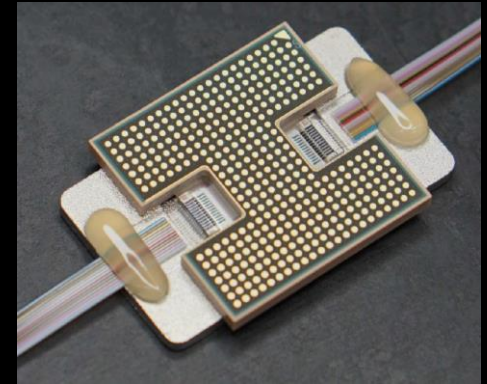
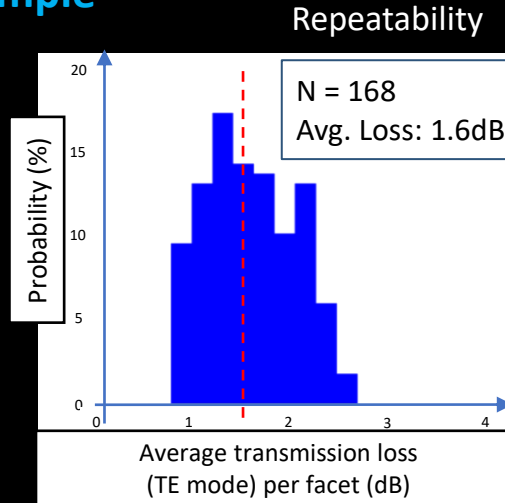


**10 μm pick and place
Self alignment to ~1 μm**

Photonic Flip-Chip assembly example



Bottom view substrate side of the module



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Formic acid flip-chip bonding

Fluxless solution required to maintain grooves/facet cleanliness and SWG integrity

Fluxless formic acid reflow with temporary adhesive material (tacking fluid)

No voiding / cracking of the IMC & solder

Formic acid reflow available at IBM Bromont



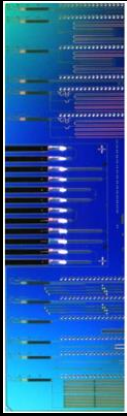
Formic acid furnace

R&D formic acid oven also available

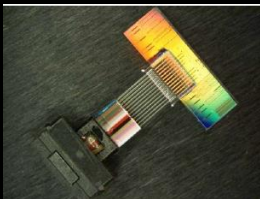
IBM presentation



Fiber Array – Reliability Demonstration

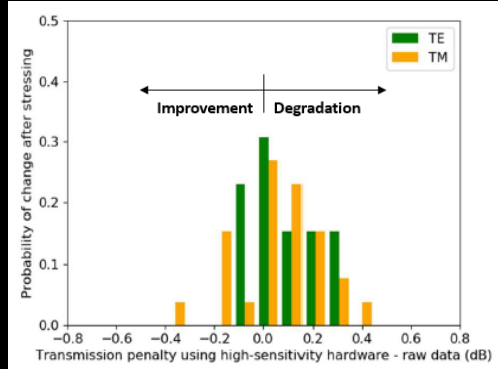


PIC



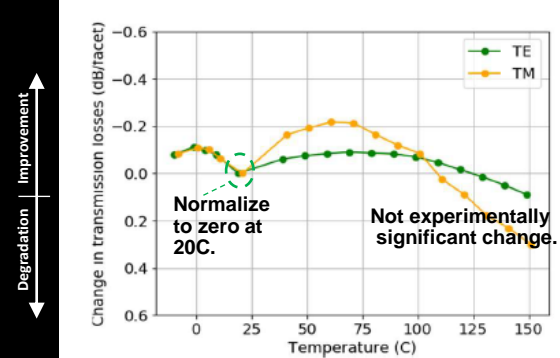
Assembly

Solder reflow (5x) 1min@250C

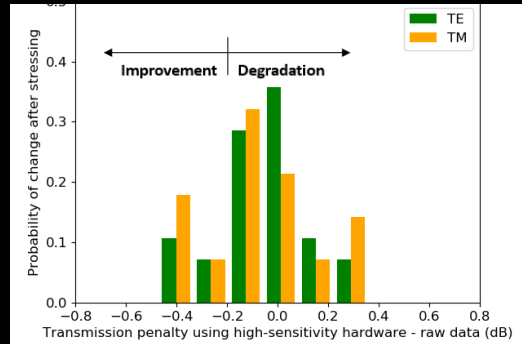


High sensitivity hardware

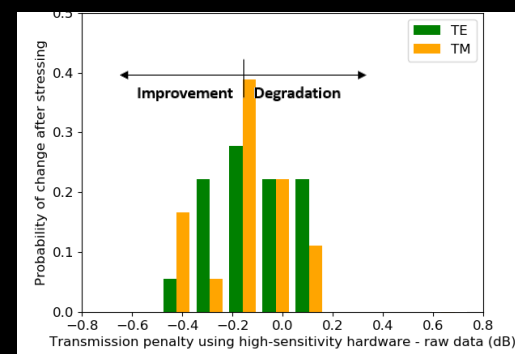
In-situ optical loss change from -10C to 150C



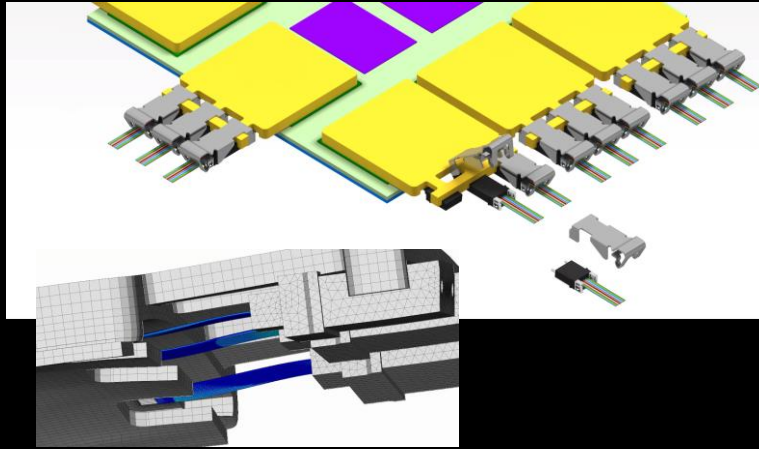
Thermal Cycling -40/85C & -40/125C : total 2000 cycles



Damped heat 85C 85%RH : 2000 hrs

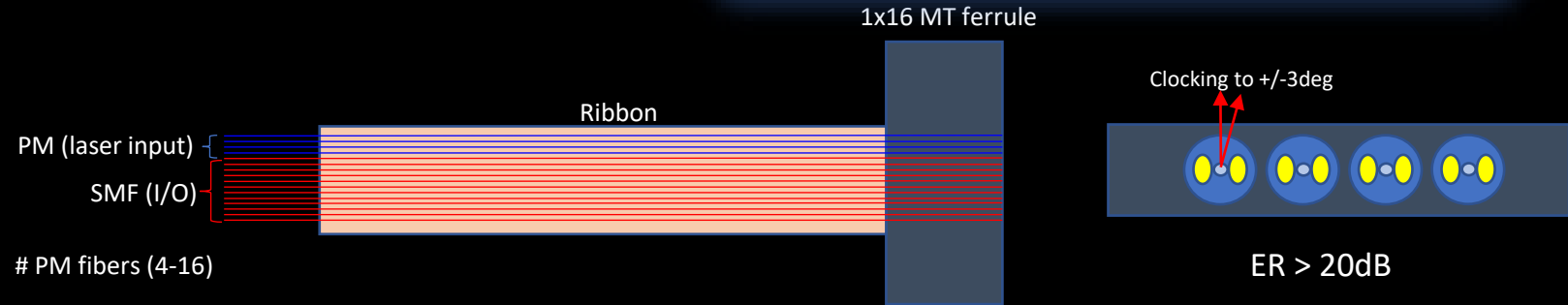


Photonic copackage – Optical connectors



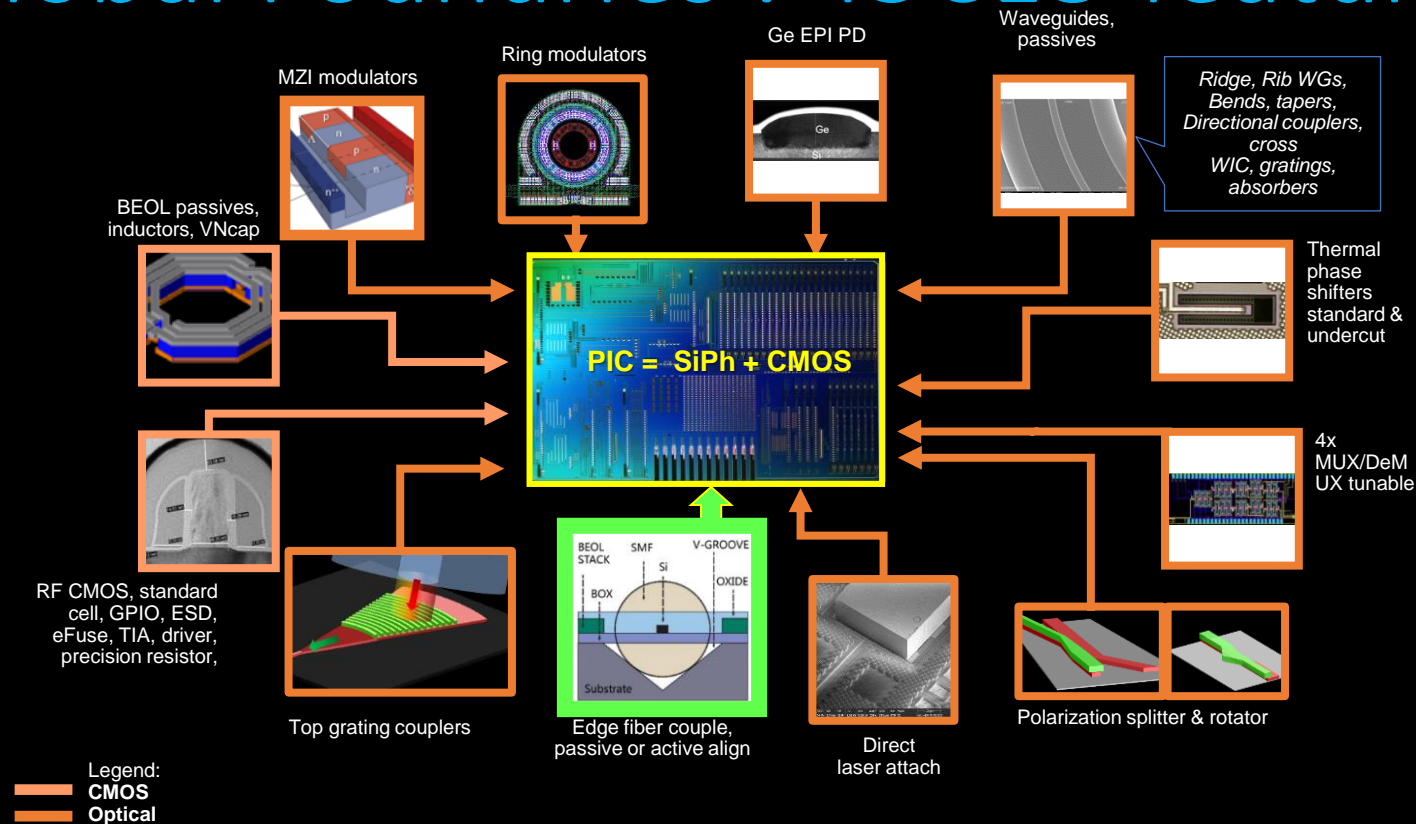
What is needed from fiber component suppliers

- Disruptive innovation to reduce connector size (integrated version)
- Solder reflow compatible ferrules
- Low loss SM 1x16 .. 2x16 ? 1x24?
- SM with 80µm fiber on reduced pitch
- PM arrays and Combination of PM / SMF fibers
- Efficient shipping and expedition of fiber component and photonic module



* Ideally Integrated connector to be solder reflow compatible

Global Foundries : 45CLO feature set



courtesy of GF
source IBM-GF :
CPO Webinar Sept16,2020

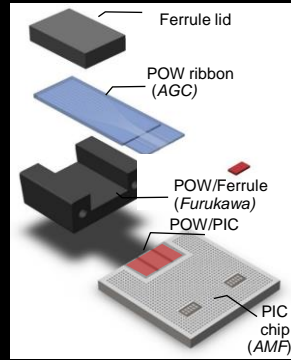
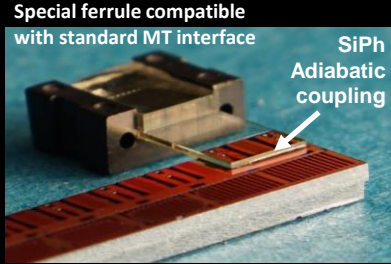
Global Foundries – Chips for co-packaged photonics

	Electronic technology for hybrid integration			GF monolithic CMOS - SiPh	
	14FF	22FDX®	BiCMOS	90WG	45CLO
nMOS Ft	270GHz	350GHz	500GHz	150GHz	280GHz
Supply V	0.8V	0.8V	3.3V	1.2V	1.0V-1.1V
Substrate	BULK	SOI	SiGe HBT	SOI	SOI
Mx res & rap	High	Low	Very low	Very low	Very low
Parasitic load	5-30fF	5-30fF	5-30fF	2-3fF	2-3fF
ESD cap	~50fF	~50fF	~50fF	0	0
Estimated TIA 3dB BW @1kΩ gain	24 GHz *(70fF)	28 GHz *(70fF)	33 GHz *(70fF)	35 GHz *(20fF)	47GHz *(20fF)

- RF-grade CMOS FETs integrated with SiPh
- Dense high speed channel integration
- Reduced packaging costs
- ESD elimination further reduces input capacitance
- Significant TIA bandwidth due to low input capacitance

courtesy of GF
source IBM-GF :
CPO Webinar Sept16,2020

Compliant Polymer interface – Dense Single mode coupler

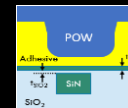
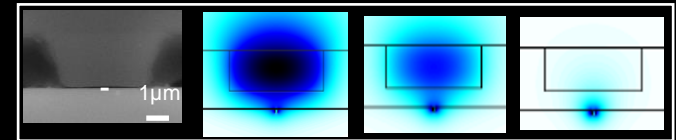
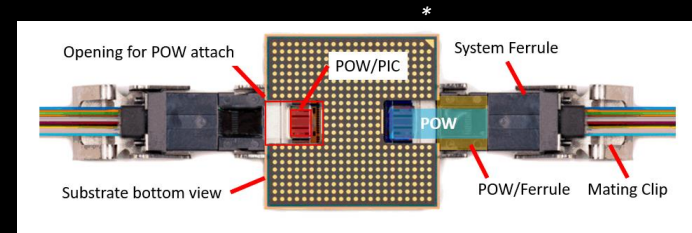
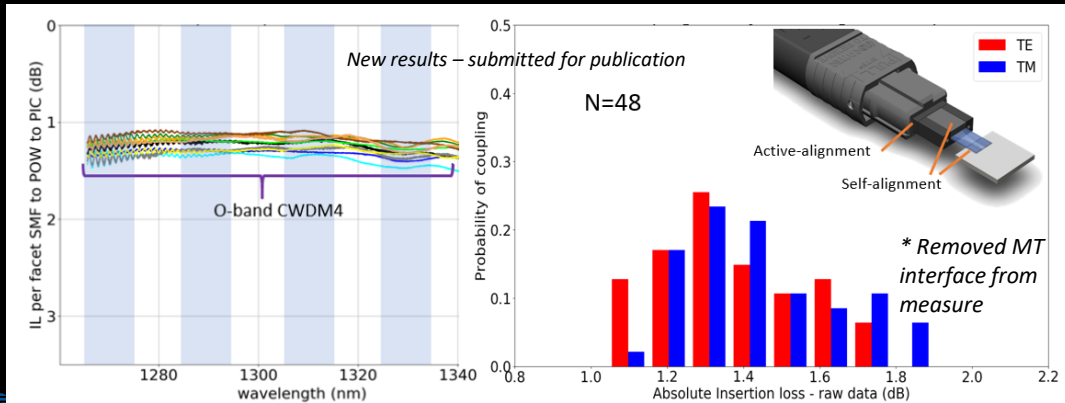


Parallel channel array (dense 50μm pitch – 12ch TV)
O, S, C, L bands compatible
Couples both polarizations (TE / TM)
Assembly using high throughput pick n place tools

- Denser pitch (up to 25μm) at chip interface
- No need for deep grooves (wet etch process)
- Mode converter structure is simple
- Compliant material for CPI risk mitigation



Advances in Interfacing Optical Fibers to Nanophotonic waveguides via Mechanically Compliant Polymer Waveguides
 IEEE Journal of Selected Topics in Quantum Electronics - 06 January 2020

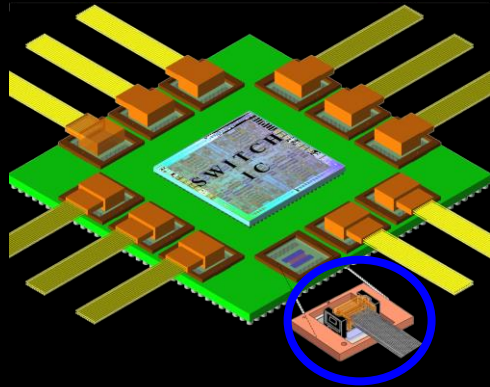


Adiabatic coupling polymer/nanowaveguide



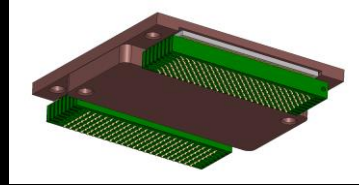
ARPA-E Enlighten: Motion – VCSEL co-packaging

Multi-wavelength Optical Transceivers Integrated On Node

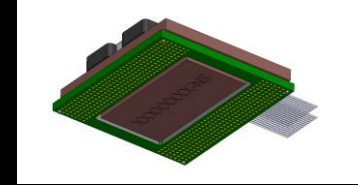


CSOP (Chip Scale Optical Package)
56Gbps NRZ (16Tx + 16Rx)

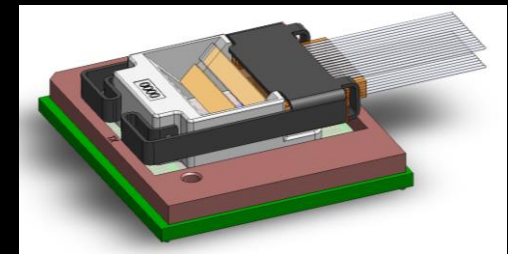
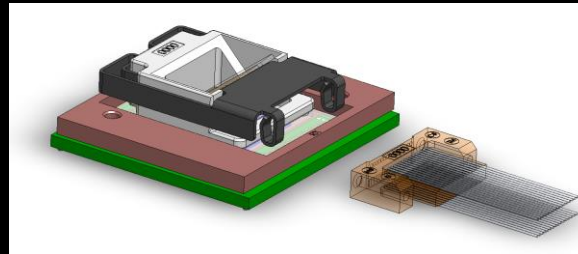
Socket version



Solderable version



Final assembly



ARPA-E Enlighten: Motion – VCSEL co-packaging

