

REDEFINING
THE
LIMITS



Assembly & Test

ALEXANDER JANTA-POLCZYNSKI

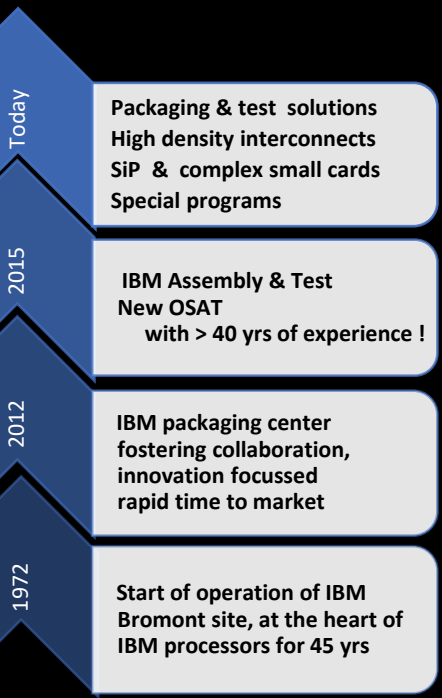
SENIOR ADVANCED PACKAGING ENGINEER

ajantapo@ca.ibm.com

www.ibm.com/assembly



North American Assembly and Test Provider



- Advanced Flip Chip Packaging & Photonics
- Any wafer source
- "Masters of Complexity"
- Outstanding characterization capabilities
- Design for manufacturing
- Better Time to market



RF

SIP

Custom

5G

400 M \$

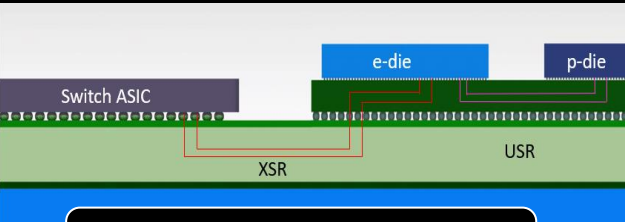
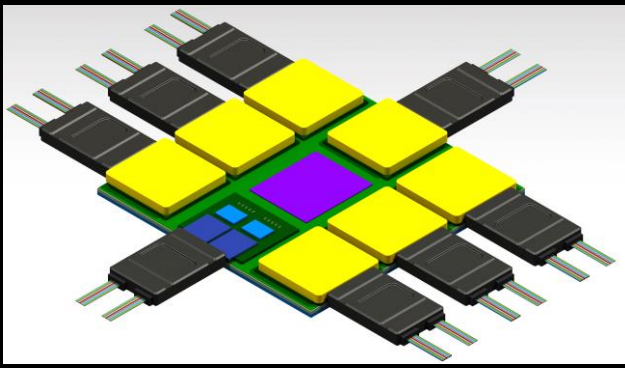
Mainframes

Datacom

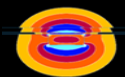
Co-Packaging – Advanced integration

Design for manufacturing & Test

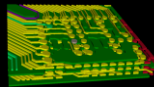
Disaggregation → Package integration
Heterogenous integration of various node function in SiP



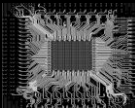
Packaging is critical for success
Co-design with packaging in mind



Simulation



Design



Substrate



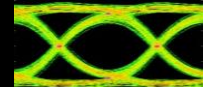
Manufacturability



Miniaturization



Optical Performance



Electrical Performance



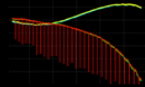
Reliability



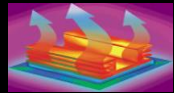
Industry 4.0



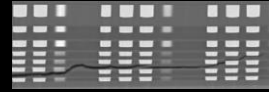
Modeling



Measure & Test



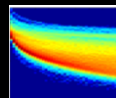
Thermal Management



CPI



Cost / yield



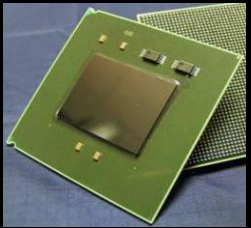
Predictive manufacturing



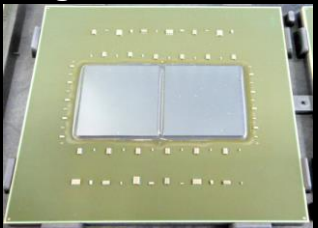
IBM Bromont – Advanced Packaging

Heterogenous integration of various node function in SiP

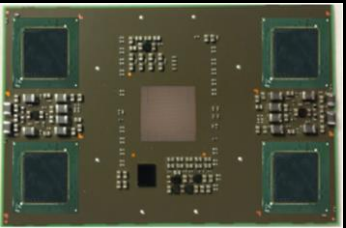
Large MCM



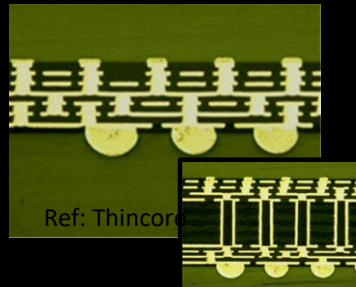
Large SCM/DCM



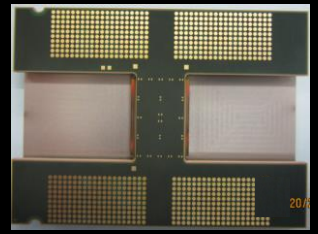
MCM - HI / SiP



Coreless



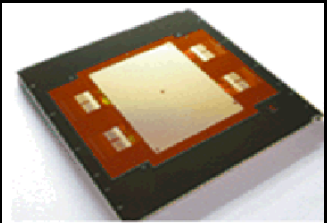
Custom



CSP



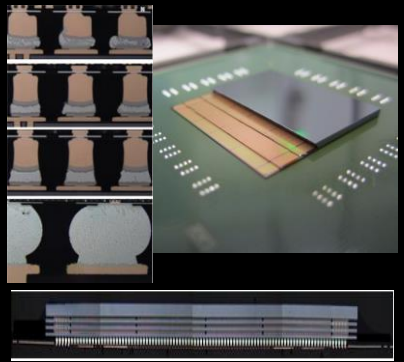
2.1D/2.3D



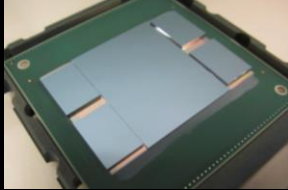
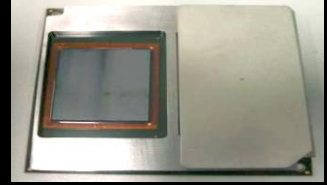
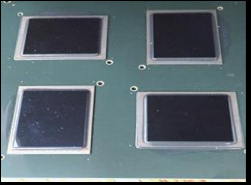
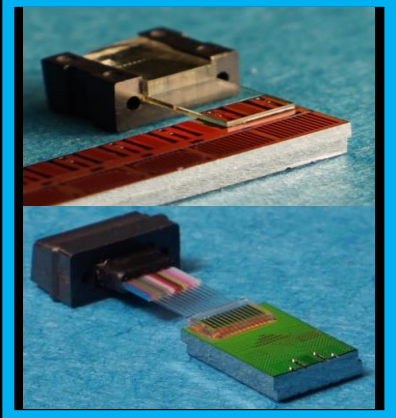
2.5D



3D



Photonics



Silicon Photonic Packaging Vision

Manual / Low volume

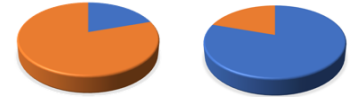
- Active alignment
- One connection at a time
- Custom design



Legacy

Cost Structure

Integrated Photonics Microelectronics



■ Packaging / Test ■ Device



Lower packaging cost increased scalability

Automated / Low volume

- Self alignment
- Multiple connections at a time
- Standard design

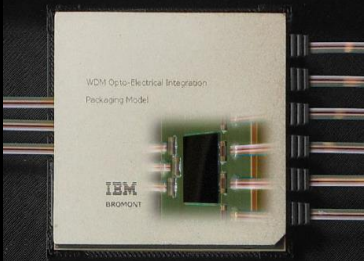


IBM Bromont

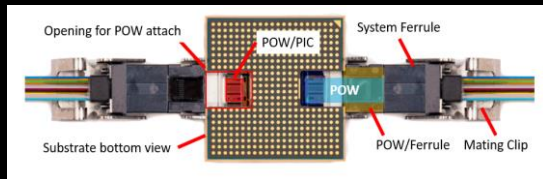
Leverage Microelectronic Packaging Infrastructure / Knowhow

Photonic co-packaging demonstrator

High Fiber Counts Application



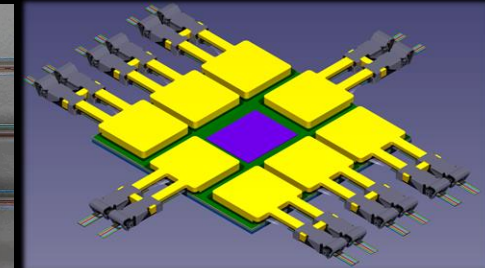
High Density Optical Port Counts Application



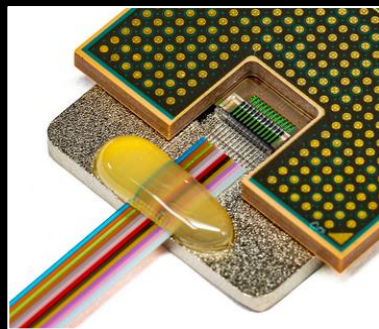
Integrated Connector



Clip installed during fiber cable plug in



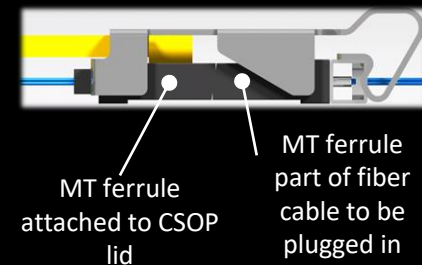
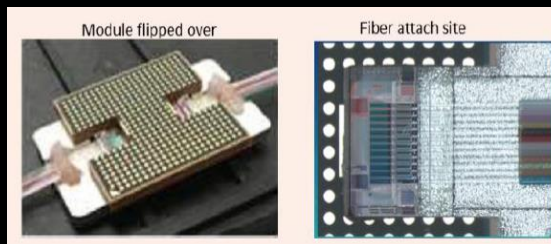
Strain Relief of fiber assembly pigtail



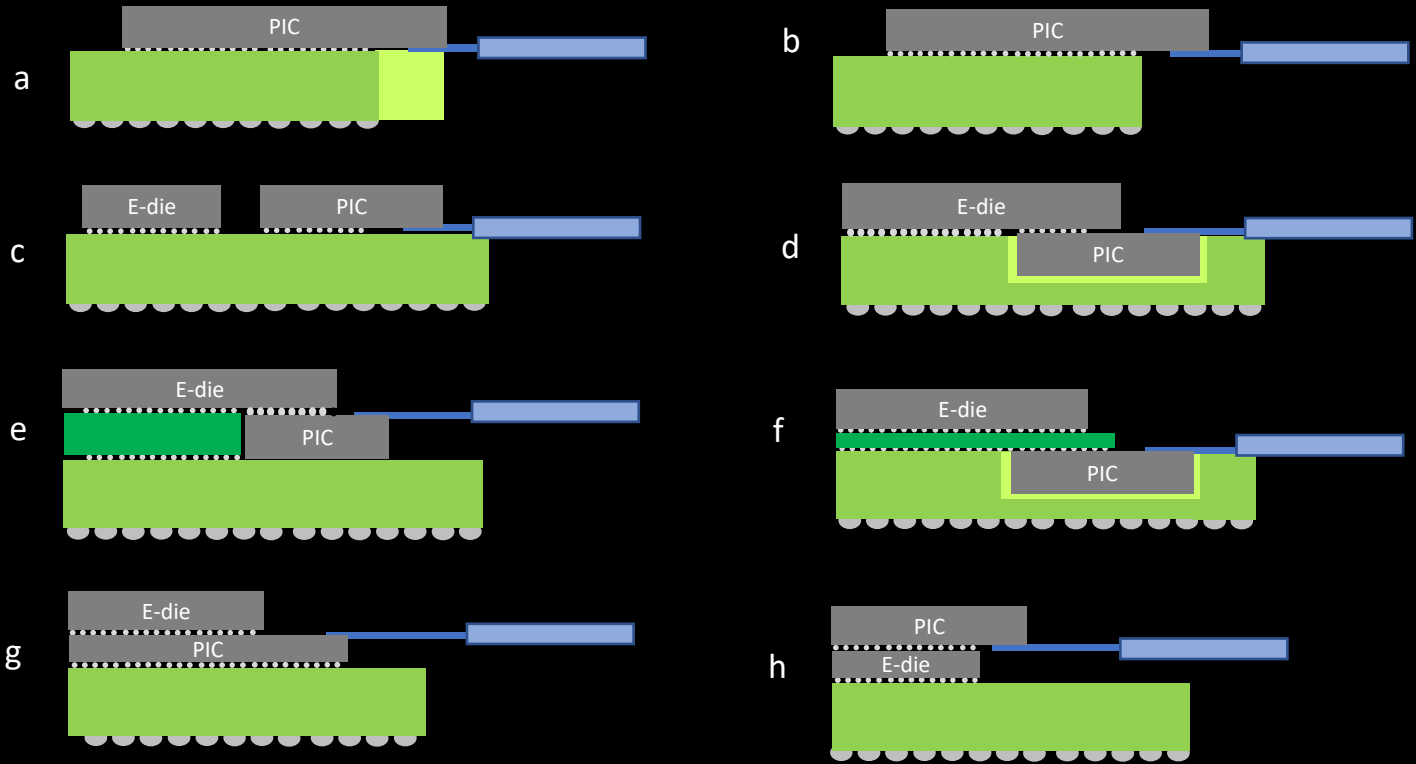
Solder Reflowable Silicon Photonics Fiber assembly



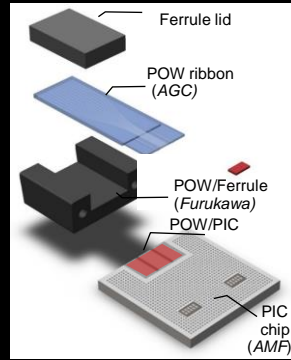
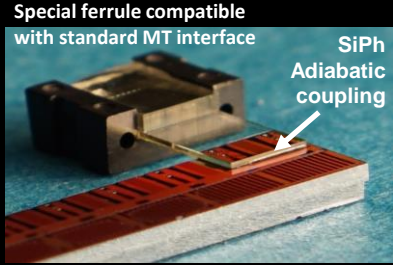
Full Optical Switch



Co-Packaging in Advanced integration



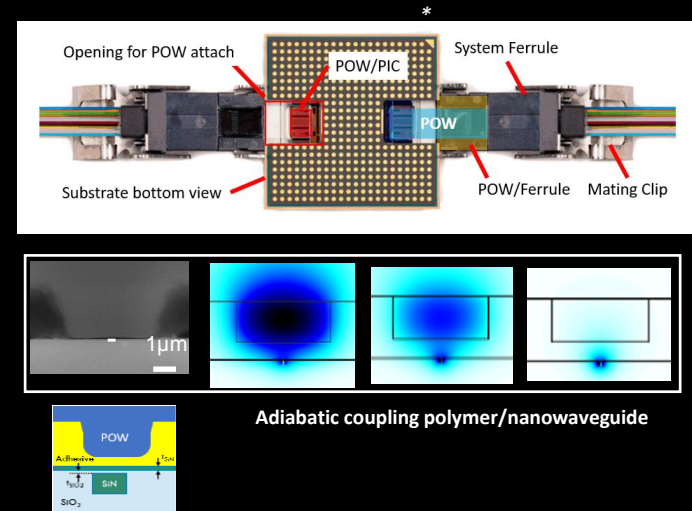
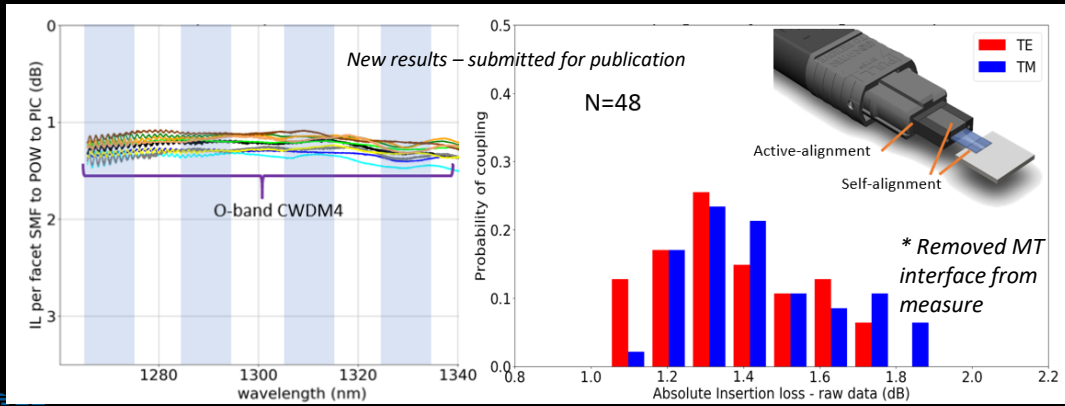
Compliant Polymer interface – Dense Single mode coupler



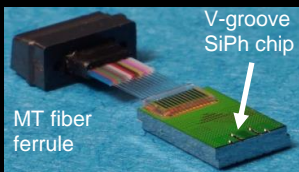
Parallel channel array (dense 50 μ m pitch – 12ch TV)
O, S, C, L bands compatible
Couples both polarizations (TE / TM)
Assembly using high throughput pick n place tools

- Denser pitch (up to 25 μ m) at chip interface
- No need for deep grooves (wet etch process)
- Mode converter structure is simple
- Compliant material for CPI risk mitigation

Advances in Interfacing Optical Fibers to Nanophotonic waveguides via Mechanically Compliant Polymer Waveguides
IEEE Journal of Selected Topics in Quantum Electronics - 06 January 2020



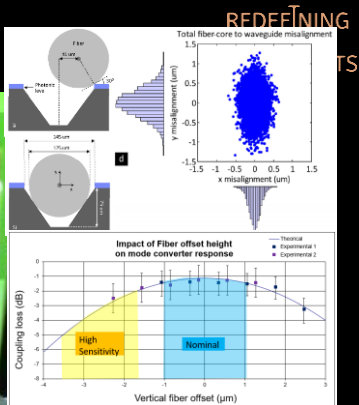
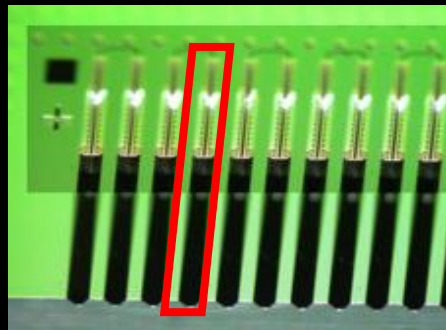
Fiber Array – Single mode solder reflowable coupler



IBM design chip build at GF

- Parallel channel array (12ch TV)
- O, S, C, L bands compatible
- Couples both polarizations (TE / TM)
- High throughput pick n place tools
- Solder reflow compatible (260 C)

Key to Success:
Adhesive partitioning



Integrated Metamaterial Interfaces for Self-Aligned Fiber-to-Chip Coupling in Volume Manufacturing

IEEE Journal of Selected Topics in Quantum Electronics
Volume: 25 , Issue: 3 , May-June 2019

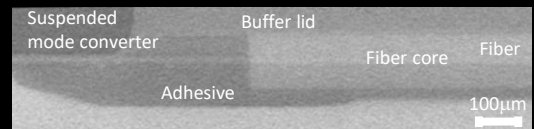
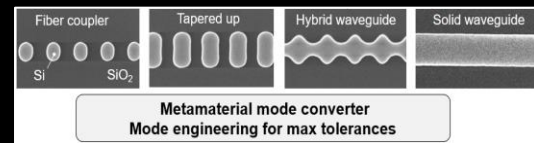
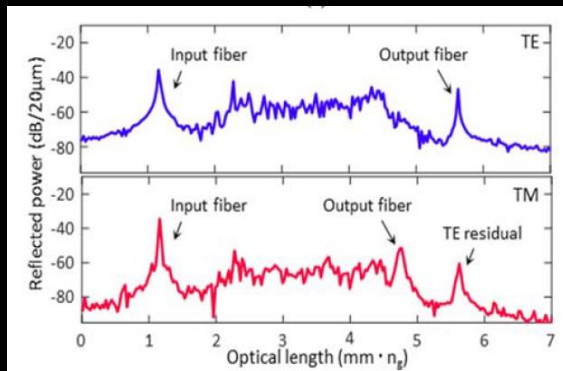
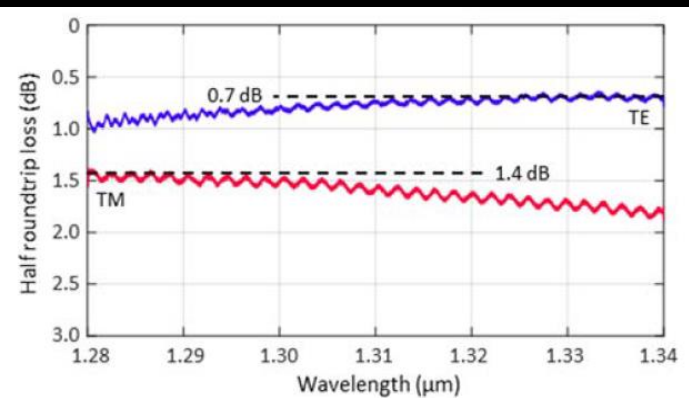


Structural adhesive for fiber

- Mechanical stability/robustness
- Fast UV tack (< 5 sec)

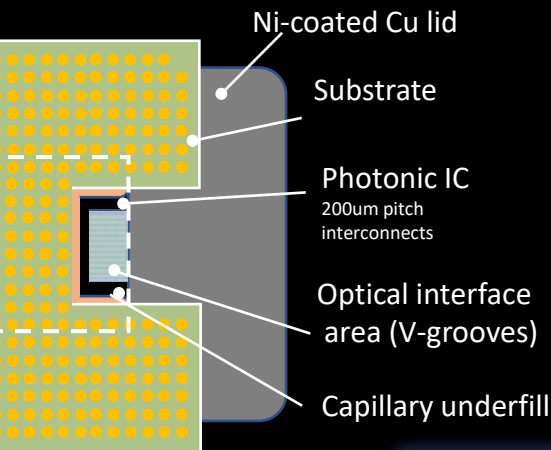
Optical adhesive for suspended region:

- Optical performance
- Reduce stress on fragile membrane



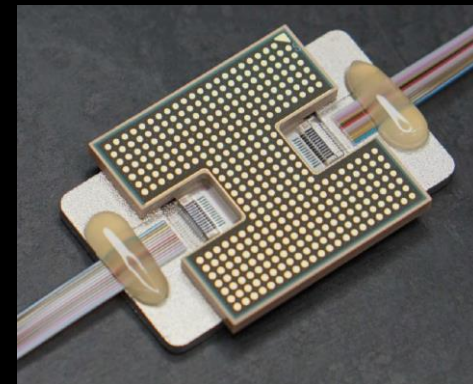
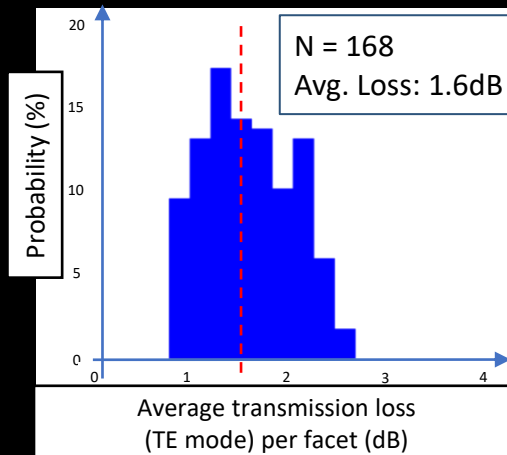
Fiber ribbon assembly in V-grooves (X-ray tomo)

Photonic Flip-Chip assembly example



Bottom view substrate side of the module

Repeatability



15

Formic acid flip-chip bonding

Fluxless solution required to maintain grooves/facet cleanliness and SWG integrity

Fluxless formic acid reflow with temporary adhesive material (tacking fluid)

No voiding / cracking of the IMC & solder

Formic acid reflow available at IBM Bromont



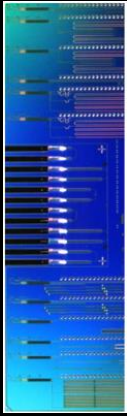
Formic acid furnace

R&D formic acid oven also available

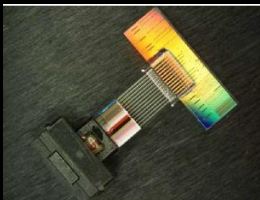
IBM presentation



Fiber Array – Reliability Demonstration

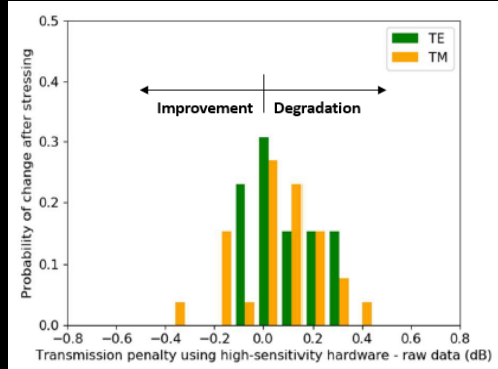


PIC



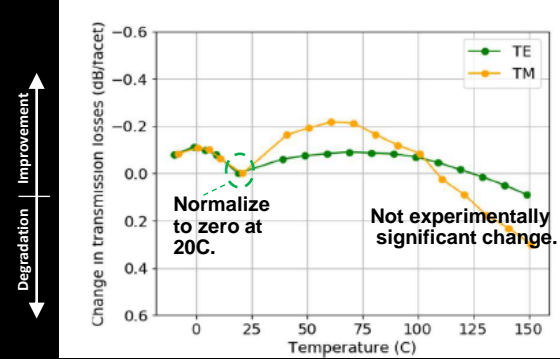
Assembly

Solder reflow (5x) 1min@250C

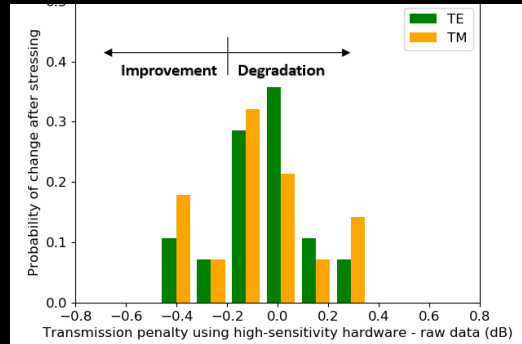


High sensitivity hardware

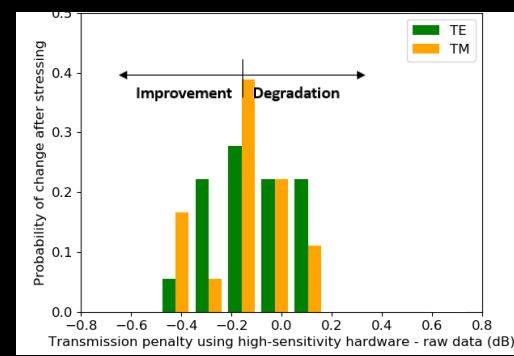
In-situ optical loss change from -10C to 150C



Thermal Cycling -40/85C & -40/125C : total 2000 cycles



Damped heat 85C 85%RH : 2000 hrs



Expertise

- Advance node (7nm)
- Proven material sets for high performance
- Prototyping to high volume manufacturing
- Microelectronics and Copackaged photonics
- Complex MCM/SiP

Time to market

- Benefit from existing models and designs to accelerate MCM implementation
- Beyond groundrules:
 - ✓ Customization
 - ✓ Characterization

Business Model

- Co design partners
- Streamlined manufacturing flow
- Integrated supply chain

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Focusing on your application and performance

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Thank You

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