SILICON PHOTONICS for Future Systems

UNIVERSITY OF Southampton

Germanium ion implantation into silicon for automated wafer-scale testing of photonic integrated circuits

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Meeting: EPIC Online Technology Meeting on PIC Testing
Presenter: Dr Milan Milosevic, Zepler Institute for Photonics and Nanoelectronics

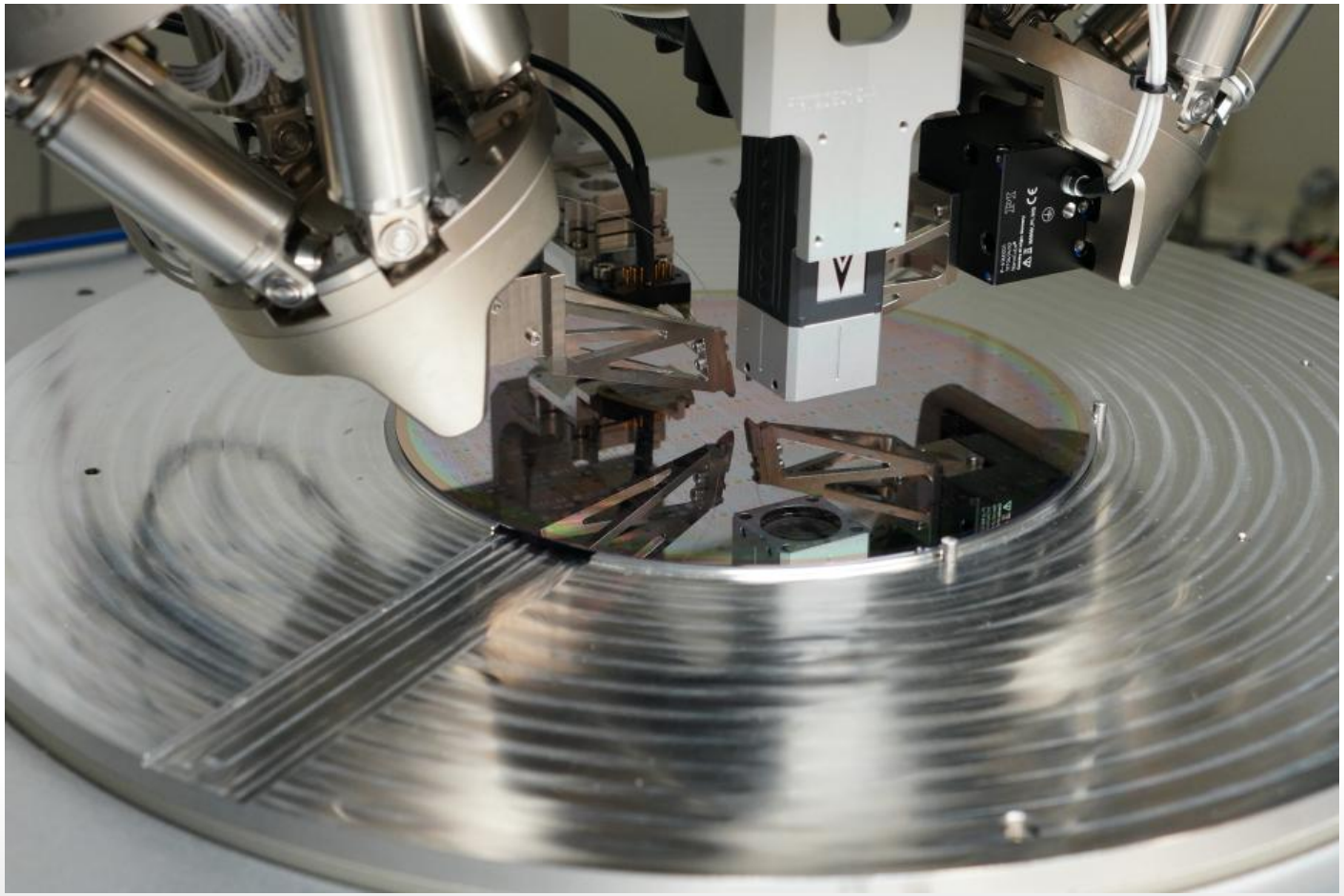
UKRI Engineering and Physical Sciences Research Council

CORNERSTONE

Motivation

Wafer scale testing enables:

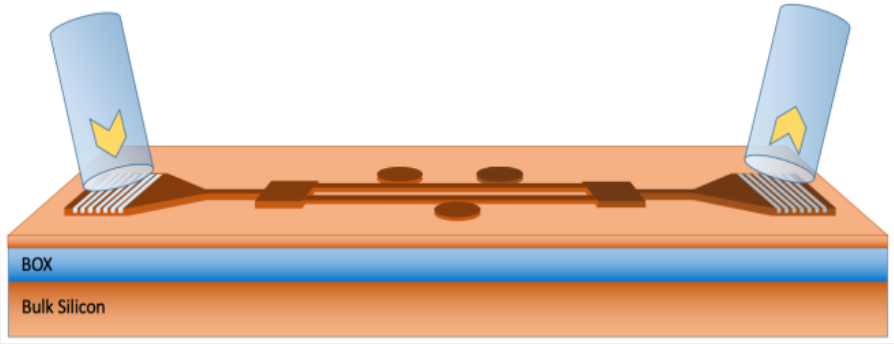
- Characterisation of individual components
- Process development
- Possibility to repair failed chips
- Maximising yield
- Reducing cost per chip
- Reducing time to market

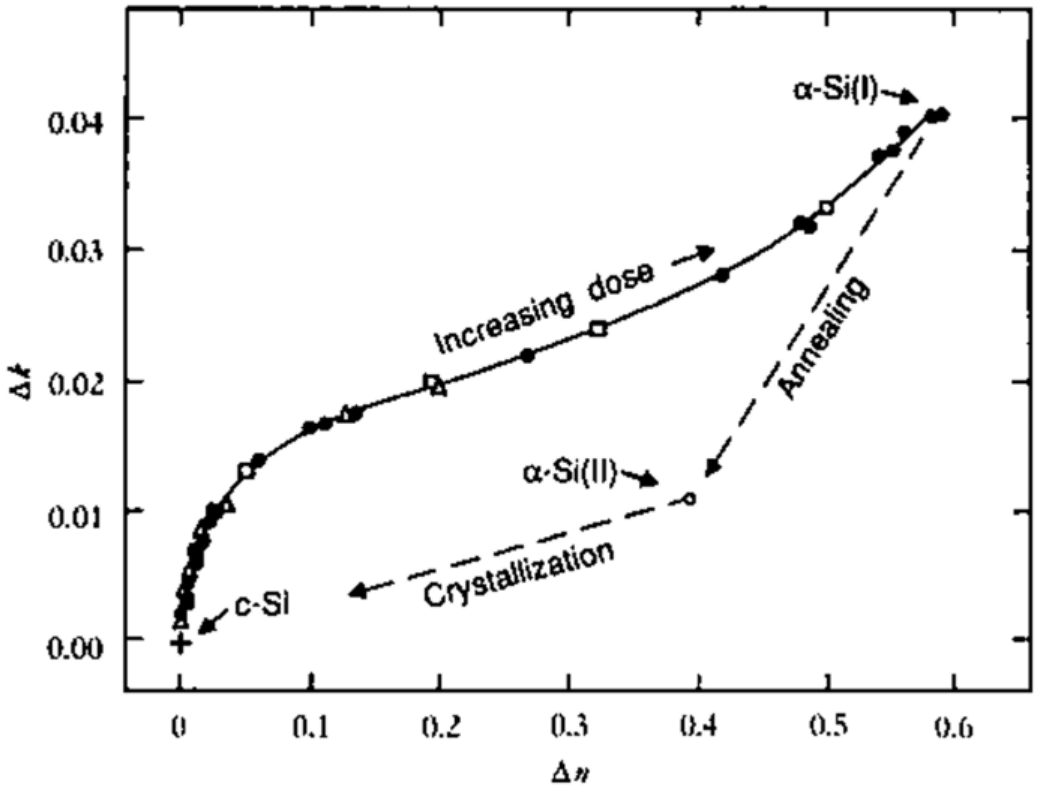


Key to our technology

Ge-ion implantation and annealing for reversible refractive index change in silicon

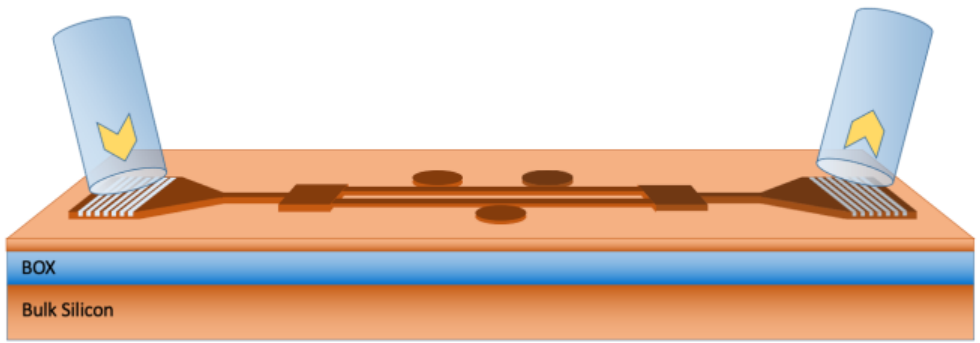
Typical coupling technique:
Limited wafer-scale testing





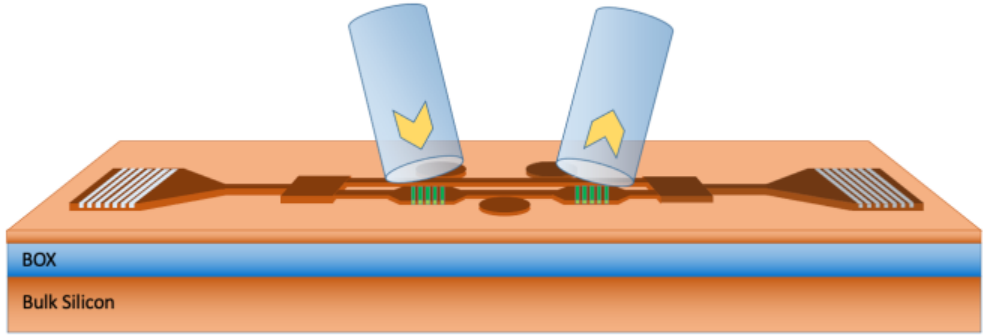
Optical effects of ion implantation (1987) *Reports on Progress in Physics v50 (5) by P. Townsend et. al.*

Erasable components



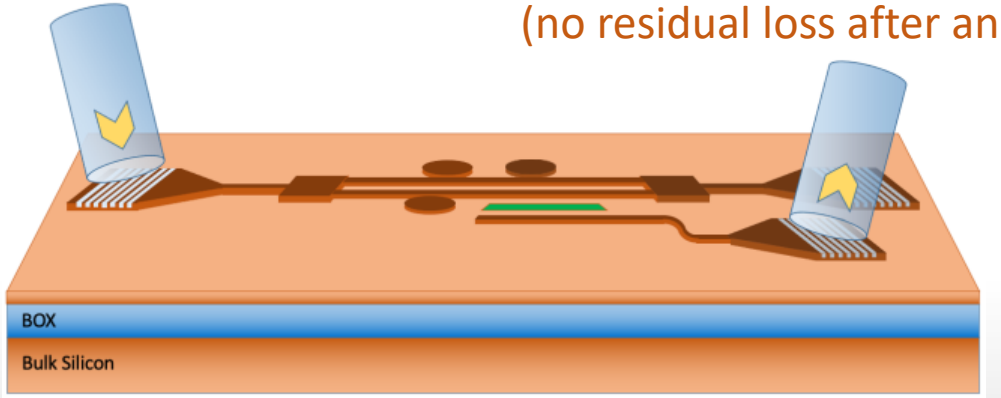
Grating couplers

(0.1dB residual loss after annealing)



Directional couplers

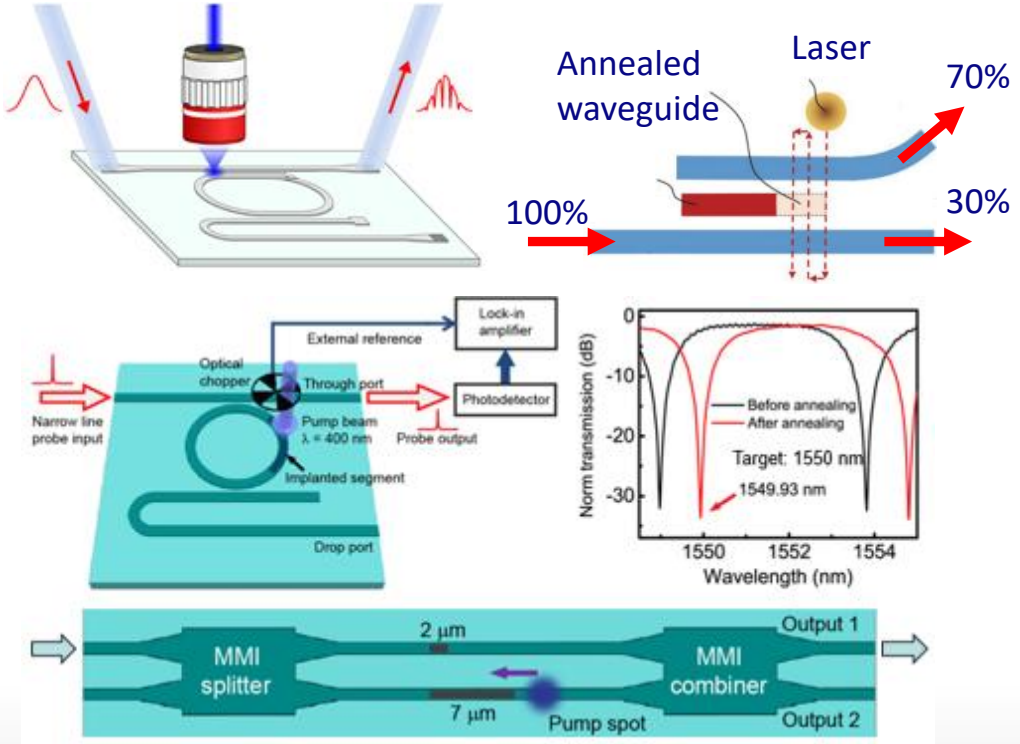
(no residual loss after annealing)



R. Topley et al. Opt. Express, 22:1077, 2014.
R. Topley et al. J. Lightw. Technol., 32:2248, 2014.
M. M. Milosevic et al. Proc. SPIE 10108, 1010817, 2017.
X. Chen et al., Opt. Express, 28:12, 2020.
Patent: GB1704690.5
Patent: US8380027B2

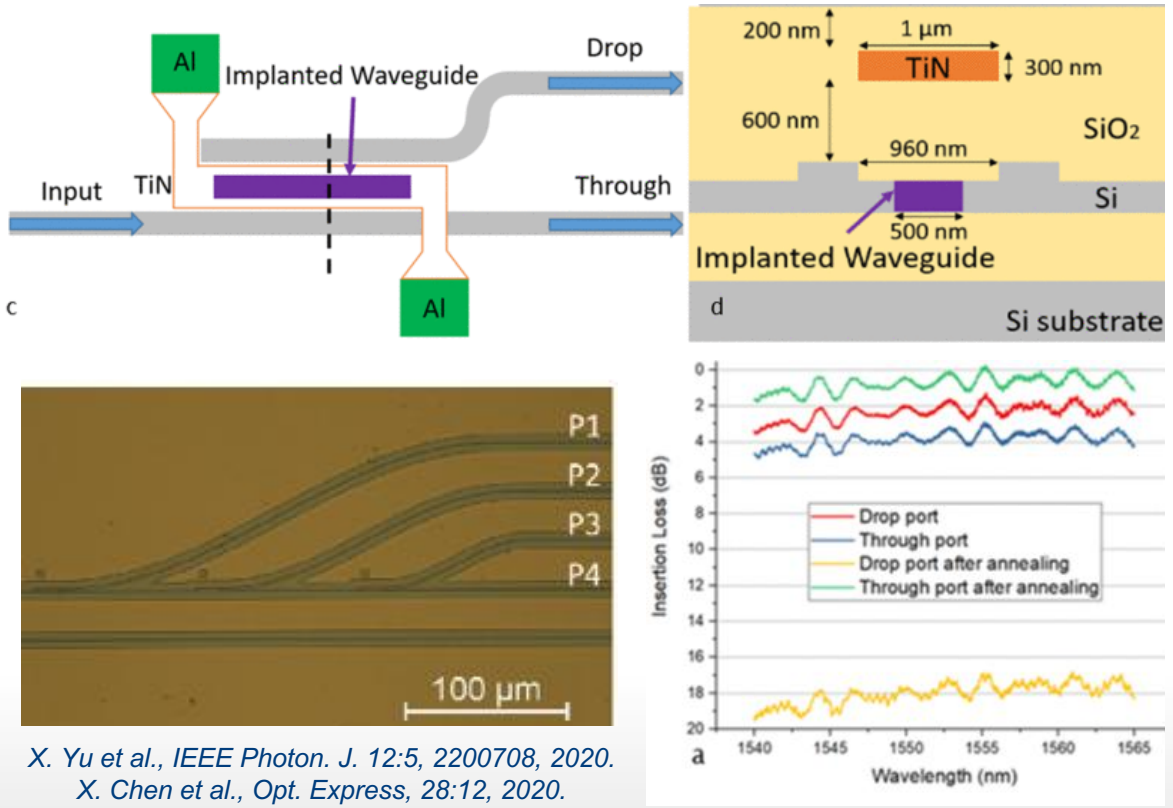
Applications

1. Laser annealing for real time trimming of rings and MZIs



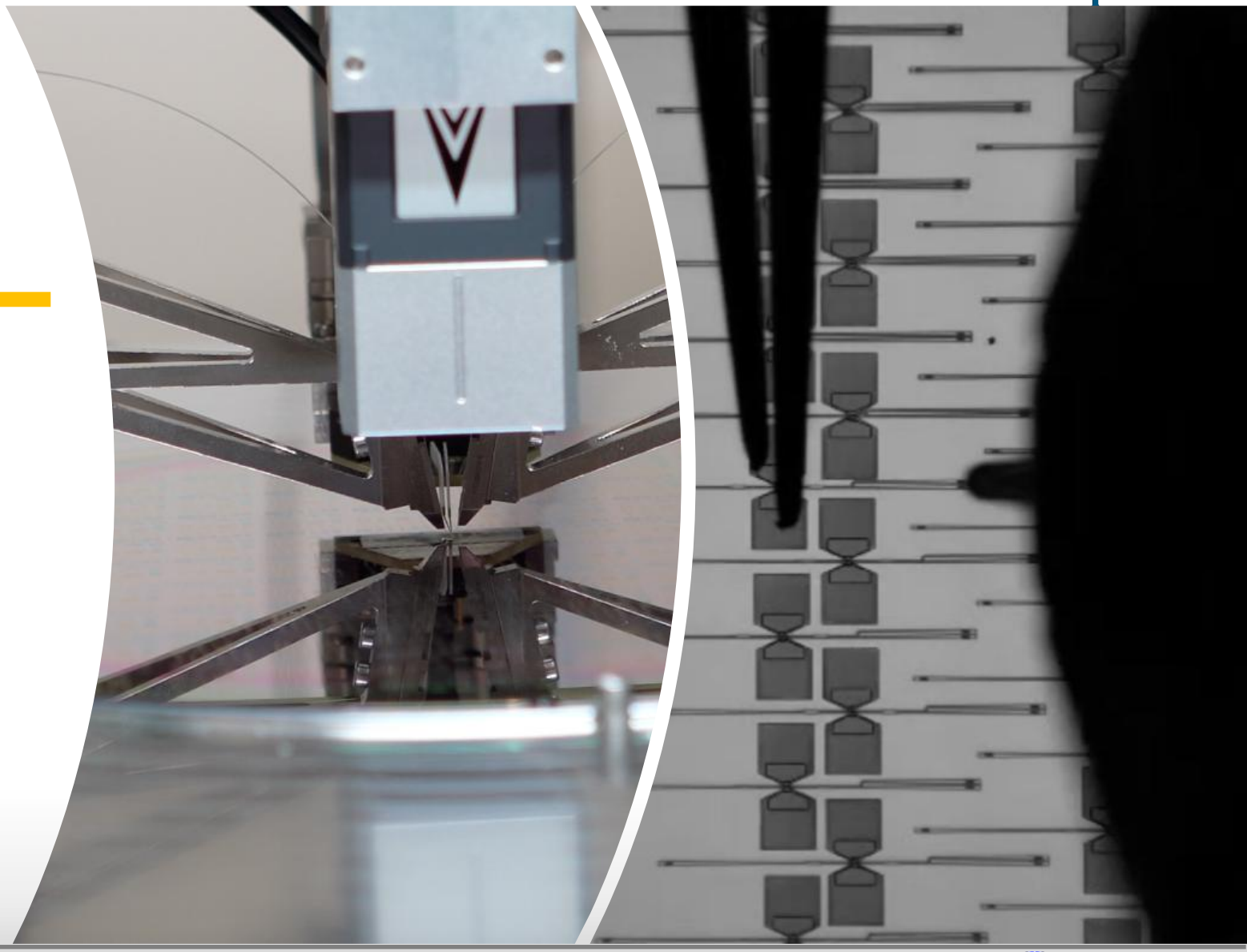
M. M. Milosevic et al. IEEE JLT, 38:7, 20220.
M. M. Milosevic et al. IEEE JSTQE, 24:4, 2018.
B. Chen et al. Opt. Express 26:24953, 2018.
X. Chen et al. Photonics Research 5:578, 2017.

2. Electrical annealing for programmable photonic circuits



X. Yu et al., IEEE Photon. J. 12:5, 2200708, 2020.
X. Chen et al., Opt. Express, 28:12, 2020.
Patent: GB1704690.5

Automation for large scale manufacturing



- Wafer Prober – ficonTEC
- Fully automated process
- Mixed signal electro-optical testing
- Chip and wafer-scale testing
- Automated optical inspection
- Data analysis
- 15k+ devices per 8’’ wafer

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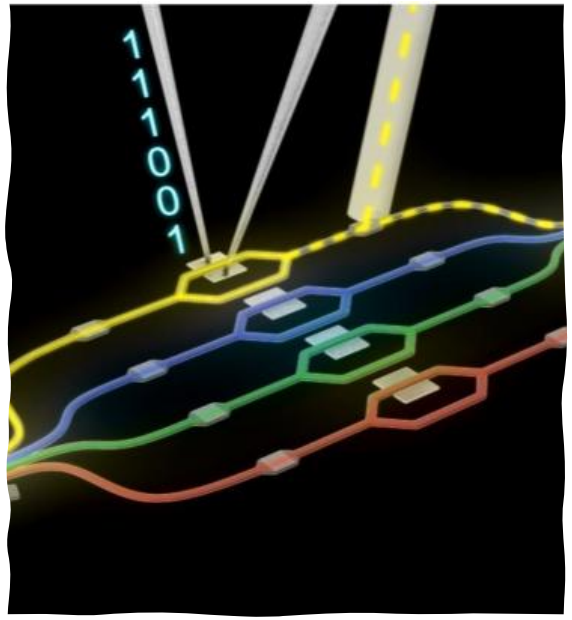
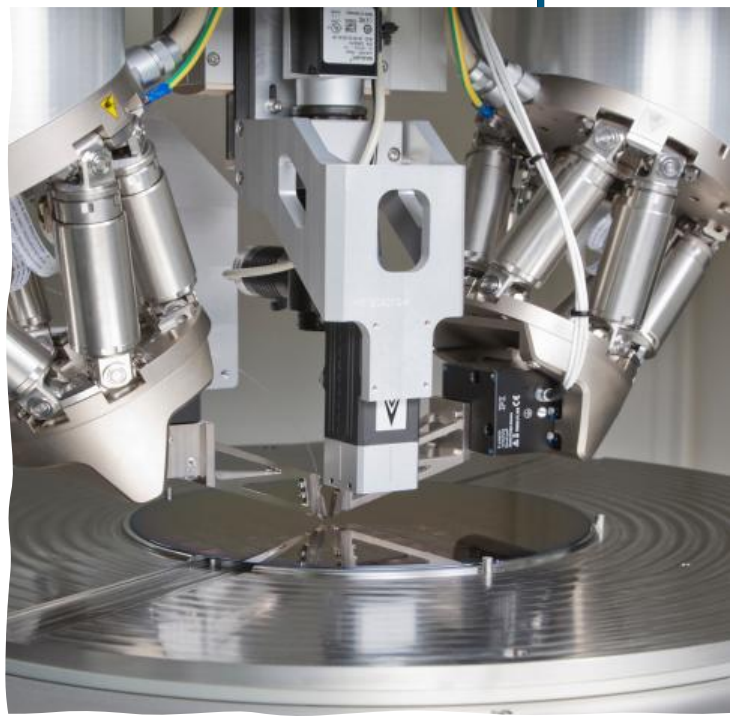
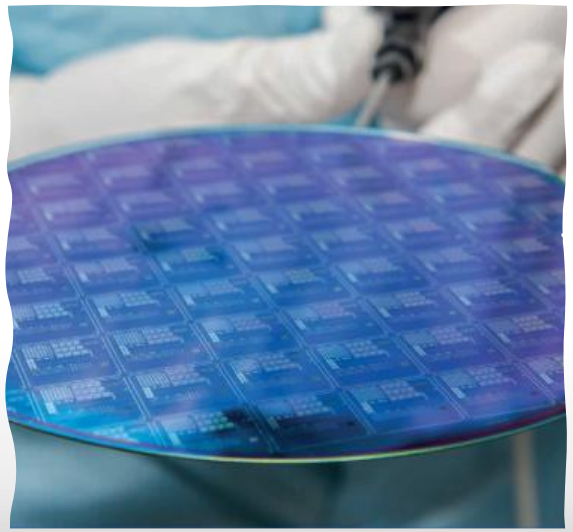
What we offer

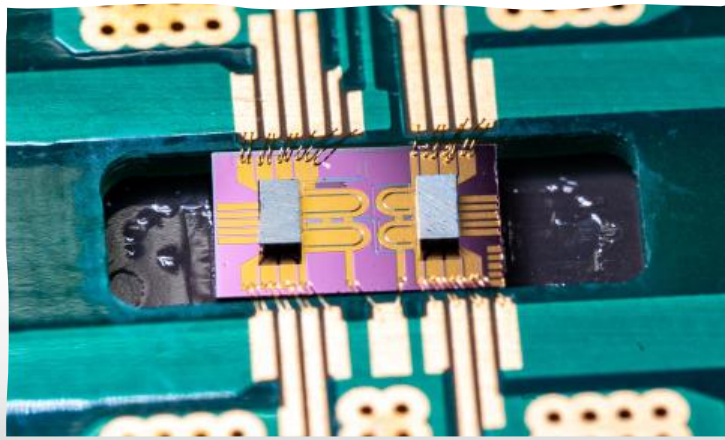
- DUV lithography service
  (Cornerstone: 220/340/500nm SOI)
- Design consultancy
- Bespoke training (partner – Luceda Photon.)
- Wafer scale testing
- Bonding

MPW schedule & costs:
cornerstone.sotonfab.co.uk









Collaborations we are looking for

- Industry and academia
- Use our technology
- Provide us with the feedback
- Tell us about your technological challenges
- Working together on the roadmap

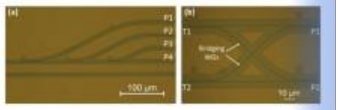
Configurable Circuit Technology Poised to Expand Silicon Photonic Applications

Chips can be programmed after fabrication for use in communication, computing or biomedical applications

WASHINGTON — Researchers have developed a new way to build power efficient and programmable integrated switching units on a silicon photonics chip. The new technology is poised to reduce production costs by allowing a generic optical circuit to be fabricated in bulk and then later programmed for specific applications such as communications systems, LIDAR circuits or computing applications.

"Silicon photonics is capable of integrating optical devices and advanced microelectronic circuits all on a single chip," said research team member Xia Chen from the University of Southampton. "We expect configurable silicon photonics circuits to greatly expand the scope of applications for silicon photonics while also reducing costs, making this technology more useful for consumer applications."

In The Optical Society (OSA) journal Optics Express, researchers led by Graham Reed demonstrate the new approach in switching units that can be used as building blocks to create larger chip-based, programmable photonic circuits.



Caption: The researchers developed a method for making configurable silicon photonics circuits. They used it to fabricate a 1 X 4 programmable photonic switching circuit that produces an output at one of four ports (P1-P4) (a) and a 2 X 2 photonic switching circuit with two output ports (P1, P2) (b).

Credit: Xia Chen, University of Southampton

"The technology we developed will have a wide range of applications," said Chen. "For example, it could be used to make integrated sensing devices to detect biochemical and medical substances as well as optical transceivers for connections used in high-performance computing systems and data centers."

Erasable components

The new work builds on earlier research in which the investigators developed an erasable version of an optical component known as a grating coupler by implanting germanium ions into silicon. These ions induce damage that changes silicon's refractive index in that area. Heating the local area using a laser annealing process can then be used to reverse the refractive index and erase the grating coupler.

In the *Optics Express* paper, the researchers describe how they applied the same germanium ion implantation technique to create erasable waveguides and directional couplers, components that can be used to make reconfigurable circuits and switches. This represents the first time that sub-micron erasable waveguides have been created in silicon.

"We normally think about ion implantation as something that will induce large optical losses in a photonic integrated circuit," said Chen. "However, we found that a carefully designed structure and using the right ion implantation recipe can create a waveguide that carries optical signals with reasonable optical loss."

Building programmable circuits

They demonstrated the new approach by designing and fabricating waveguides, directional couplers and 1 X 4 and 2 X 2 switching circuits, using the University of Southampton's Cornerstone fabrication foundry. Photonic devices from different chips tested both before and after programming with laser annealing showed consistent performance.

Because the technique involves physically changing the routing of the photonic waveguide via a one-time operation, no additional power is needed to retain the configuration when programmed. The researchers have also discovered that electrical annealing, using a local integrated heater, as well as laser annealing can be used to program the circuits.

The researchers are working with a company called ficonTEC to make this technology practical outside the

OSA News, May 2020.

Challenges

- Applications are expanding beyond telecom/datacom
- Need for further time-to-market and costs reduction
- Need for seamless design flow for automation
- Built in self-tests, generic test protocols, in line testing, control and programmability
- Unified materials platform serving various markets

Acknowledgements

- This work was funded by EPSRC projects under the “Silicon Photonics for Future Systems” “Electronic-Photonic convergence”, “Laser-Engineered Silicon” and “CORNERSTONE” projects.
- Graham T. Reed is a Royal Society Wolfson Research Merit Award holder. He is grateful to the Wolfson Foundation and the Royal Society for funding of this award.
- Virtual showcase event (14/Dec/2020): https://www.eventbrite.co.uk/e/silicon-photonics-for-future-systems-virtual-showcase-tickets-121261186473.

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