

GLOBALFOUNDRIES Silicon Photonics Test Capabilities Overview

Ken Giewont EPIC Online Technology Meeting on PIC Testing Nov 16 2020



GF silicon photonics optimized for key markets



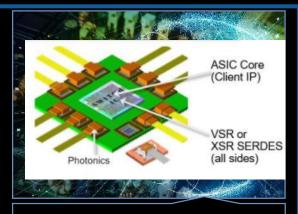
5G Back Haul/ Front Haul (1310 nm)



Data Center Interconnect (400ZR, 1550 nm)



100G/400G Intra Data Center (1310 nm)



Chip-to-Chip, Co-Packaged Optics

90WG/90WG+

45CLO base & features

90WG Base Qualified for Production

- O-band photonics library
- passive v-groove fiber attach
- monolithic 90nm CMOS
- Cadence PDK with custom design support

90WG+ feature development early availability 1Q'21

- 50Gbaud PAM4 MZM, laser attach, Nitride WG

45CLO Base: Proto MPW's 2Q21. Production: 4Q'21

- Leverages 90WG base & features PDK library development
- Added High performance 45nm RF monolithic CMOS
- Base includes Nitride WG, Cu pillar capture pads,

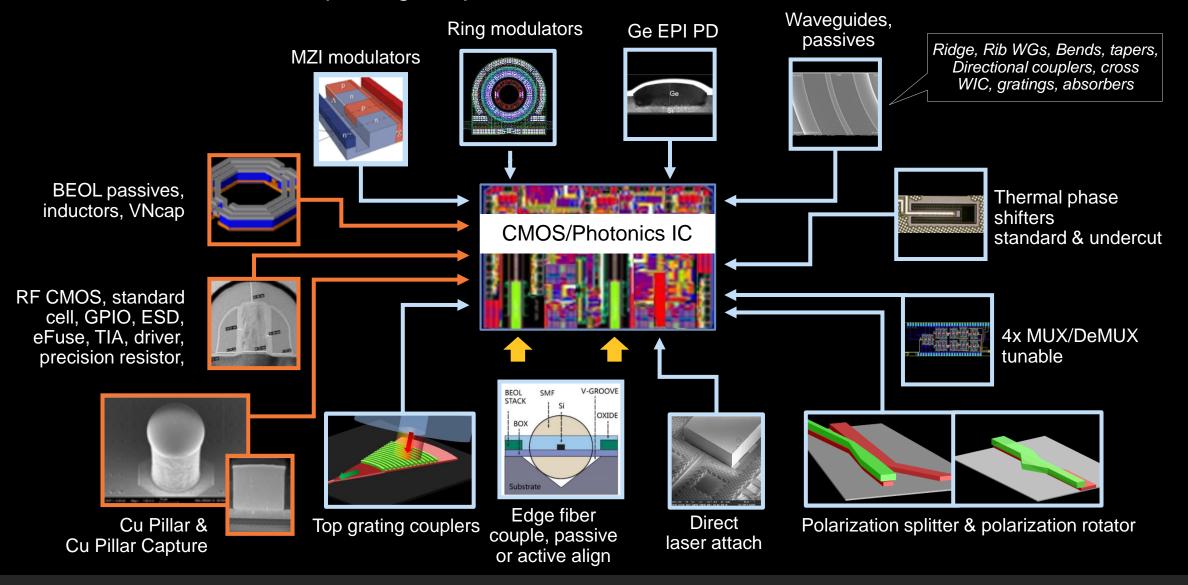
45CLO features development. Proto MPW's 3Q-4Q'21

Cu upillar , MRM, cWDM, sealed UCUT heaters,
127um pitch FA, Laser attach, APD

45SPCLO feature set

Legend: CMOS Optical

Focus on data com & co-packaged optics



State-of-the-art silicon photonics test capability

Technology Verification



- Technology models
- Device level testing
- Semi-automated test
- Two fiber test
- Analog BW
- Tunalble lasers
- Temp range -5C to 85C

Inline Optical Test

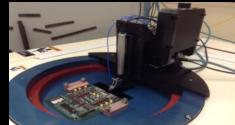


- Volume wafer level
- Full automation
- Device level testing
- Process monitor, WAC
- Process development
- Two lensed fibers

One special AC system

- EO & OE S-paramter
- NRZ & PAM4 eyes
- Fiber array block

Low Frequency EO Wafer sorting



- Volume wafer level PIC test
- Automated fiber alignment
- Optical BIST test
- Sacrificial grating option
- Electrical Scan, DC, AC

High Frequency EO Wafer sorting

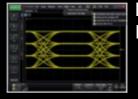


- Volume wafer level PIC test
- 67 Ghz, full automation
- Full automation & calibration
- TIA / Driver
- Optical/DC, OE, EO BW
- Single ended, differential Sparamter
- Fiber array block
- 4 channel support

Full Speed Characterization



Coherent System



NRZ Pam4

- Circuit & Technology verification
- Package limitations
- Adherence to stds
- At speed performance
- Benchmark data
- MCM debug
- Calibration
- EUH bring up

Net: Wafer-level through MCM test capability, direct detect & coherent solutions

Reduce test costs by driving control & containment through automation

- Speed
- Accuracy
- Repeatability
- Adaptability



Thank you

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