What are the requirements for PIC Wafer-level Testing?

EPIC Online Technology Meeting on PIC Testing

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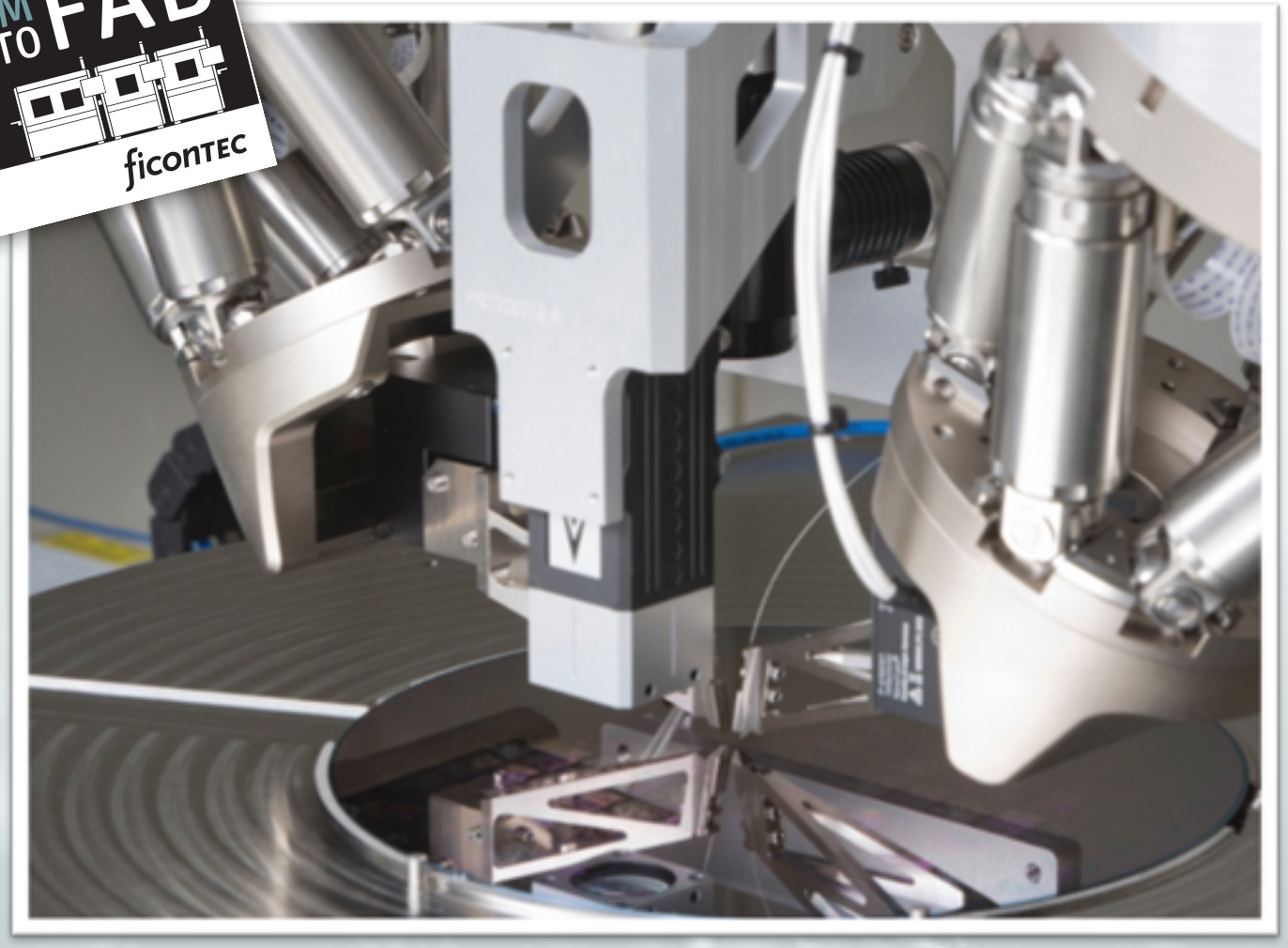


6 min. agenda on PIC testing …

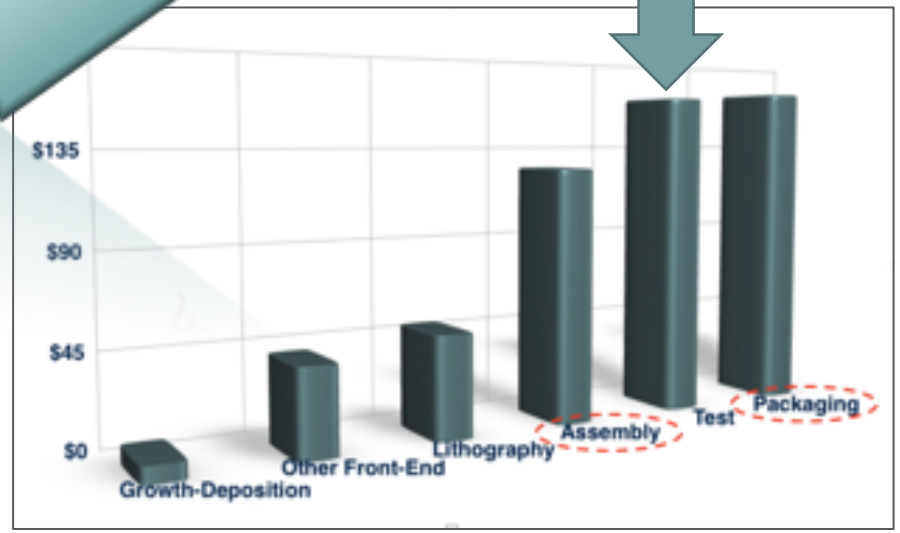
- **Raising questions / finding answers / generating requirements for PIC Wafer-level Testing / Volume manufacturing**

- Not new at EPIC / not new at ficonTEC …
- Testing is costly …
- I have changed role at ficonTEC: from Dir. Business Development to Principal Photonics Testing

Please note! *These slides contain my opinions based on the last few years experiences: I would be pleased to be proven right, be proven wrong, receive feedback, challenges, share ideas …*

An EPIC event in Pisa, February 2017

A 2006 graph used over and over in many presentations including mine …

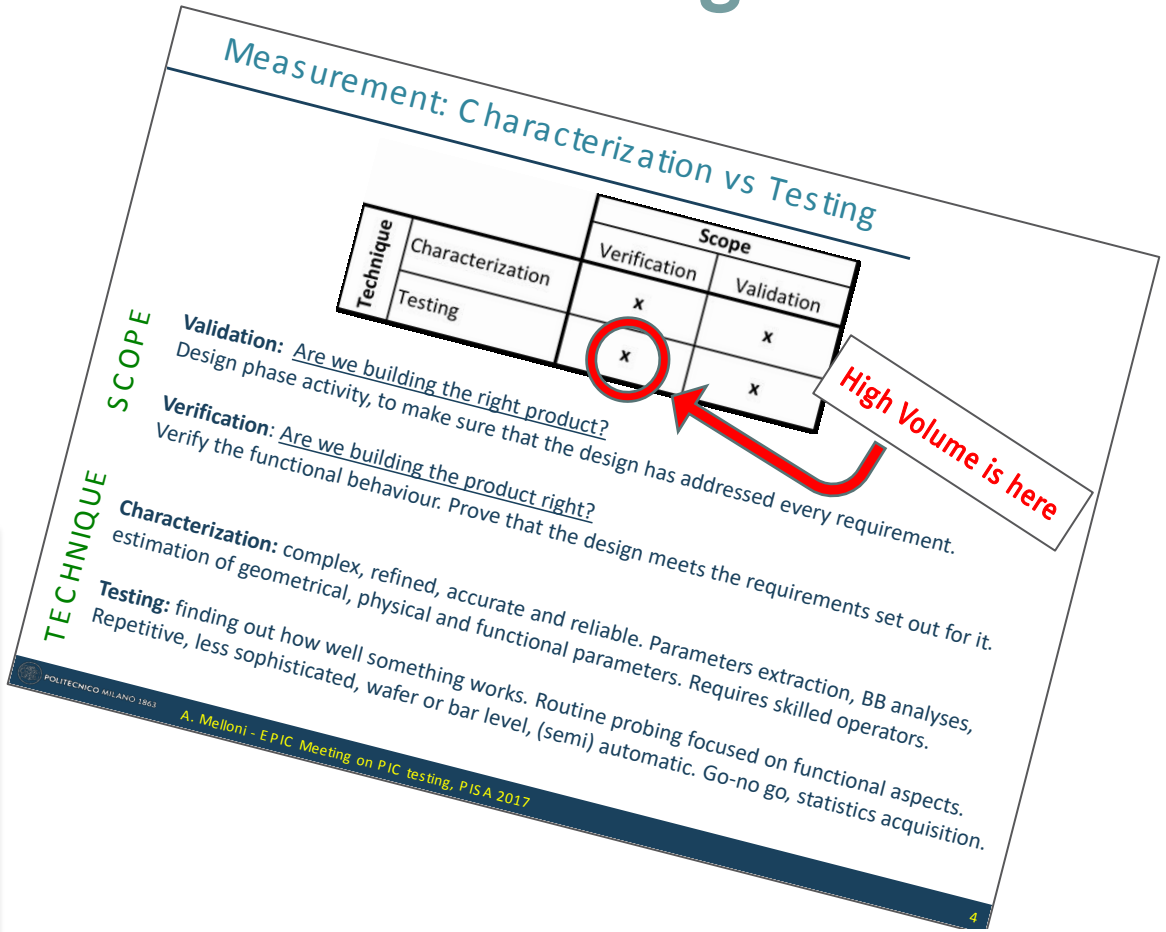


'Process-Based Cost Modeling of Photonics Manufacture: The Cost Competitiveness of Monolithic Integration of a 1550-nm DFB Laser and an Electroabsorptive Modulator on an InP Platform'*, Journal of Lightwave Tech, Vol. 24, No. 8, 2006 (from Peter O'Brien presentation at pOp, Edinburgh Nov. 2016)*

WL characterisation vs volume / production WL testing

- Characterisation: verify & validate, measure all you want and all you can …
- Volume production testing: measure only what is strictly necessary, as fast as possible, as cheaply as possible …

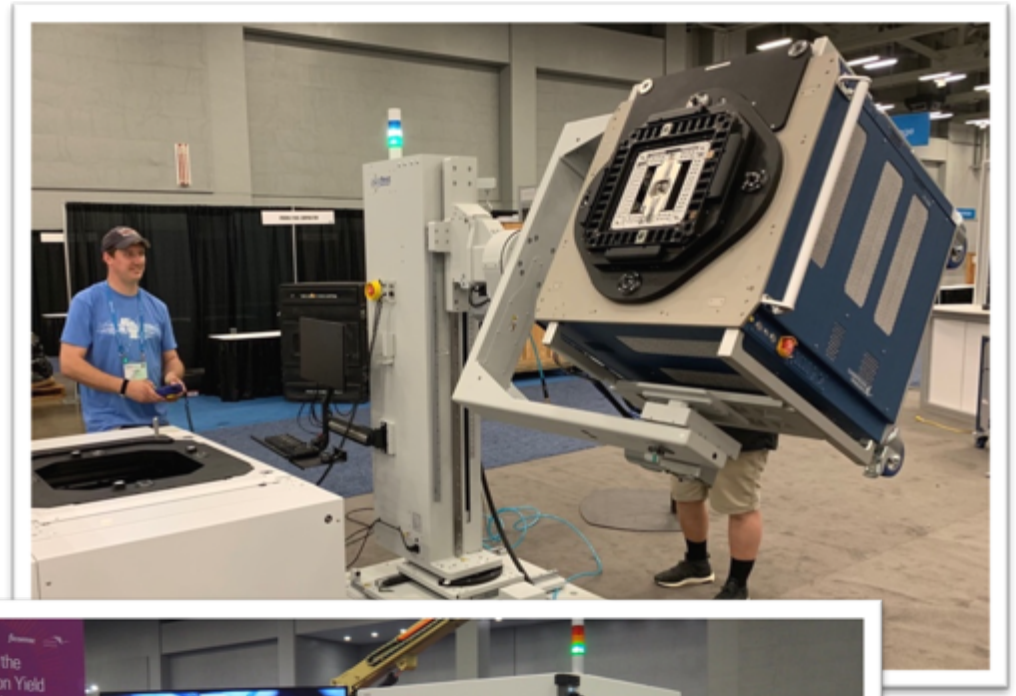
A PIC chip prober / sorter: from blue tape to gel-packs, ficonTEC 2016



Courtesy Prof. A. Melloni, Polytechnic of Milan

What can we (not) borrow from semicon?

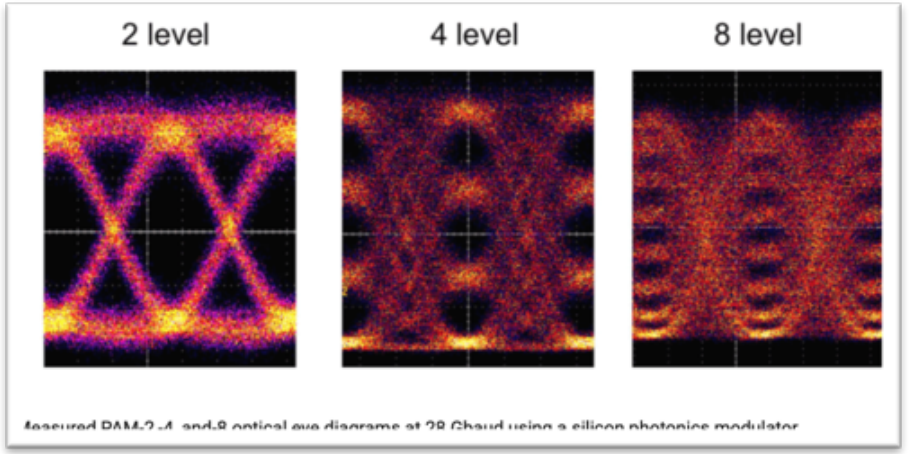
- JTAG (Joint Test Action Group) / Boundary scan / TAP (Test Access Port) started as techniques developed to test PCB and found their way into processors and embedded systems
- JTAG begun in 1985 , known as IEEE 1149.x
- In semicon one deals only with electrical pads / contacts and full wafer simultaneous testing is possible (with tens of thousands of contact pins)
- Higher resolutions / accuracies are needed for optical probing
- Combining optical in/out (both vertical grating couplers and edge coupling), DC and low freq. electrical, and RF in the tens of GHz poses some interesting challenges!
- Photonics WL testing is still very young …

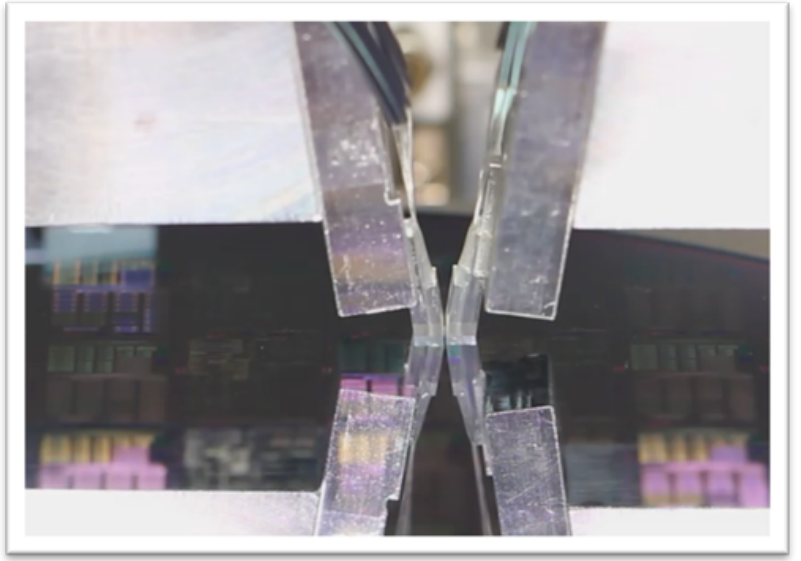


At NI Week , Austin, Texas, May 2019

What do we need to test?

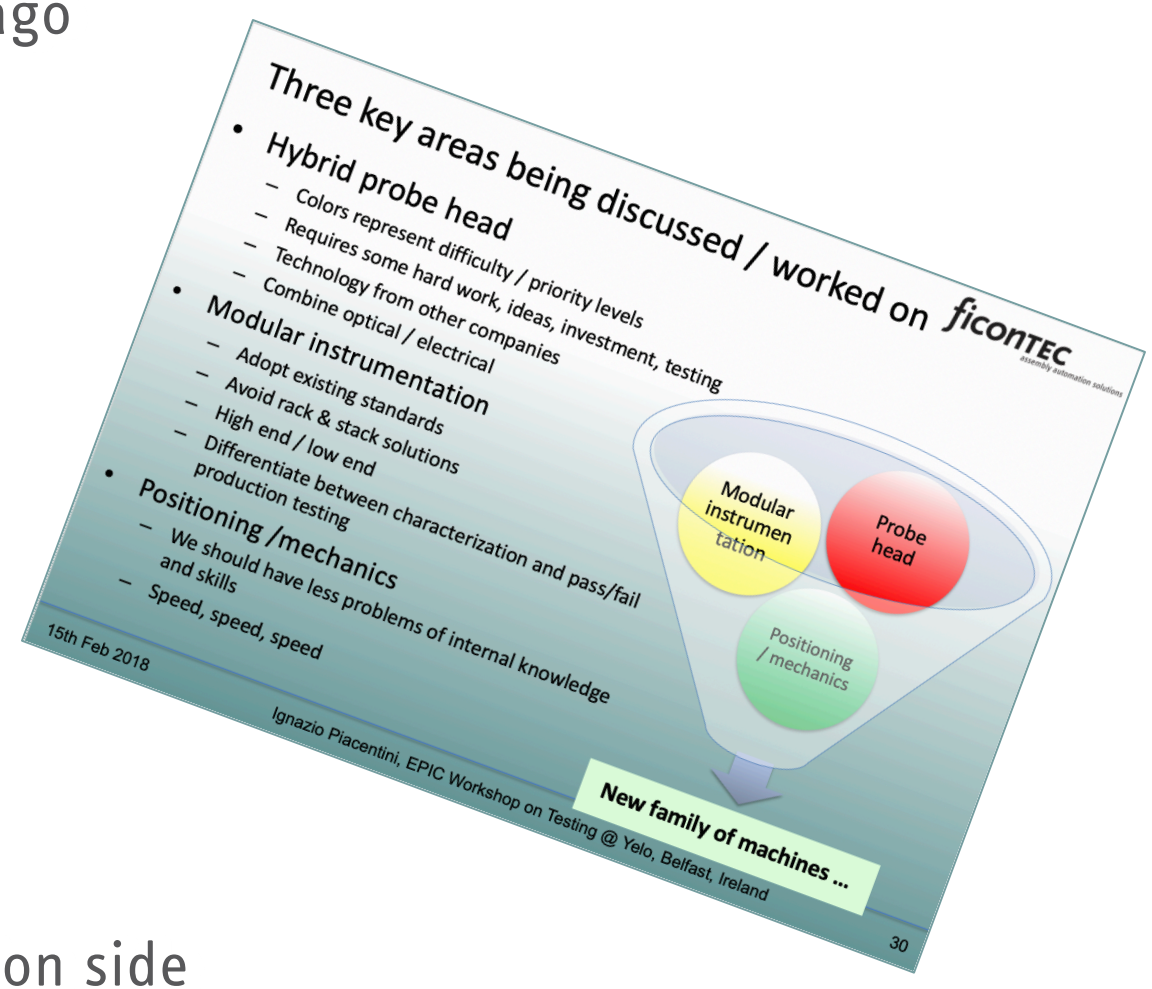
- All the PICs on a wafer?
- Multiple PICs simultaneously?
- From VCSELs to full transceiver PICs?
- From LIV (Light-Current-Voltage) to BERT (Bit Error Rate Testing)
- Is measuring RF always needed?
- Can it be bypassed by end-to-end optical measurements in production (i.e. after full characterisation)?
- At which temperature ranges (temp-controlled wafer chucks)?
- What do you do with all the data you collect?
- How to map it back to your wafer layout and your production KPIs?
- What throughput do you hope to achieve?
- **The list gets long …**





Positioners & handling, probe heads, instrumentation

- Continuing the discussion started a few years ago and building a road map …
- Witnessing an increasing request from the photonics marketplace for WL testing
- ficonTEC has been able to re-use / adapt sub-systems from photonics automated assembly such as passive / active alignment, wafer handling, pick-&-place, machine vision, user interface software …
- On going collaborations and development on probe heads
- More modularity required on the instrumentation side



ficonTEC is better known for PICs assembly, but we have done quite a bit of work also on testing! Let us know your needs …

Instrumentation: going parallel / going modular

- Volume production testing requires a dedicated photonics front-end
- Multi-signal / multi-chip simultaneous testing dictates a lower cost per channel
- The two statements above would indicate that more mix & match modular instrumentation (from different vendors) is needed
- PXI is a possible platform, but has been around for more than 20 years …
- Discussion to be continued …

Conclusion: a workgroup on PIC testing?

- I hope that in these 6 min I've tickled some interest
- There is a need to harmonise / clarify PIC WLT requirements
- Would it be feasible to create a dedicate PIC WLT workgroup within our own association?

Any questions?

… and thanks for listening !!

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