



# Si-Photonics Packaging : Development and Challenge

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**EPIC Online Technology Meeting on Co-packaged Optics**



# ASE in the Electronics Value Chain

## Bridging OSAT and EMS



### ASE Group Service



Engineering Test



{Bumping, Assembly, Wafer Sort,  
Component Test  
Substrate}



{Module Design, Module Assembly  
Module Test, Component Sourcing  
FAE Support}



{System Design, System Assembly  
System Test,  
Software Development, Logistics  
Product Marketing, Sales & Support}

ASE Quick Facts:  
Established: 1984  
Employees: 100K+  
Global Facilities: 19  
FY 2019 revenue: US\$13.38B



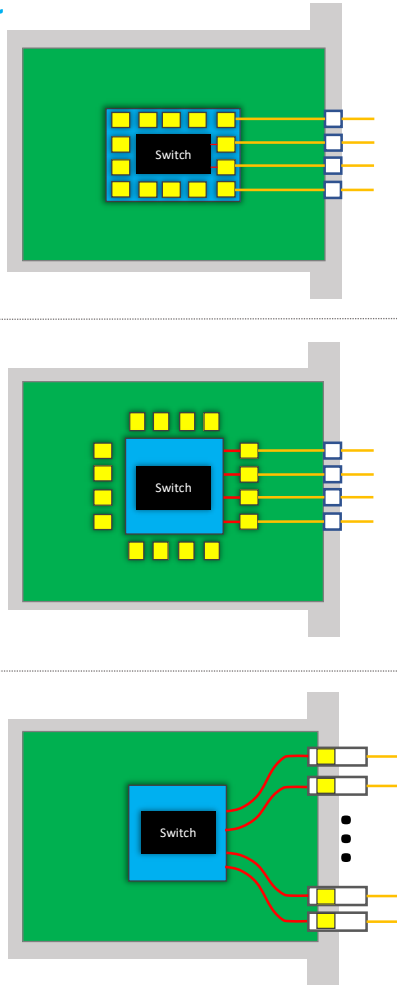
# Key Discuss Area Today

- **SiPh Overview: Switch & Optics Integration Evolution**
- **Typical SiPh Engine Packaging Structure**
- **Co-Packaging Optics Challenges**
- **Consolidate Supply Chain for Cost Reduction & Toolbox**

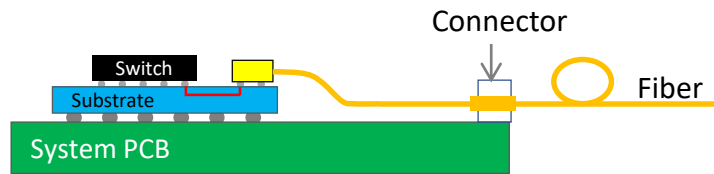


# Switch & Optics Integration Evolution

Higher bandwidth  
Lower power  
Lower Cost



Top View



System PCB

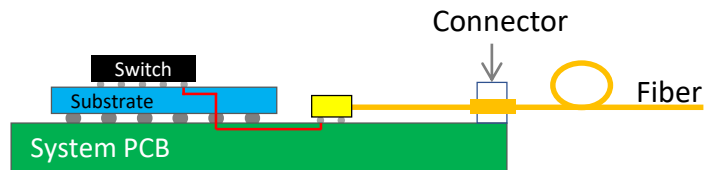
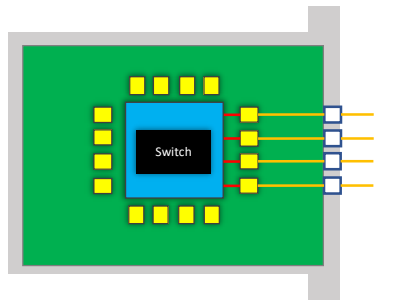
Side View

Co-Packaging Optics

PKG Solution?

Optical Engine Data Rate

>1.6Tbps

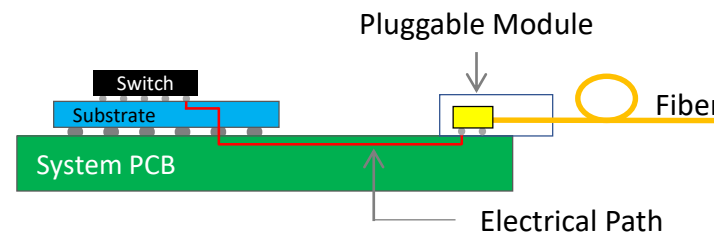
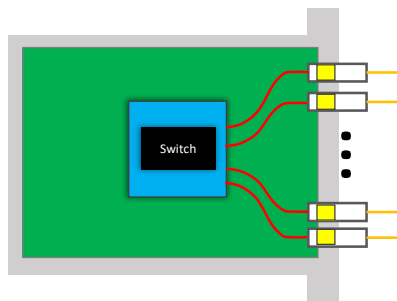


System PCB

On-Board Optics

PKG Solution?

400Gbps  
~1.6Tbps



System PCB

Pluggable Transceiver Optics

QSFP-28  
QSFP-DD  
OSFP

100Gbps  
~400Gbps



# Typical SiPh Engine Packaging Structure

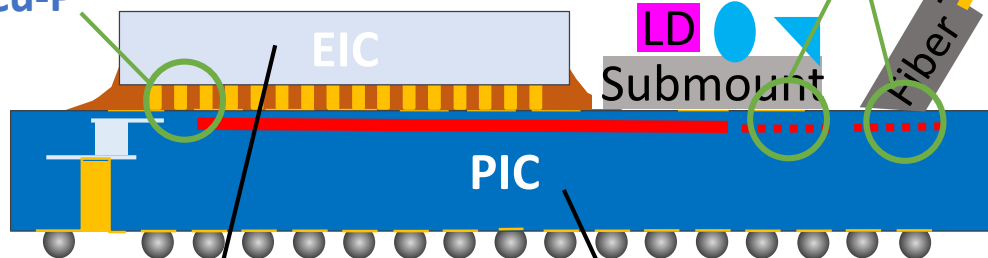
## SiPh Engine

- Embedded , Discrete or remote
- WLCSP with hermetic PKG
- <math><1\mu\text{m}</math> LD D/A on Sub mount (AuSn)
- Lens/ rotator placement (KOH pit)

- Single mode fiber (Array)
- Vertical or edge coupling

Active alignment

CoC Cu-P

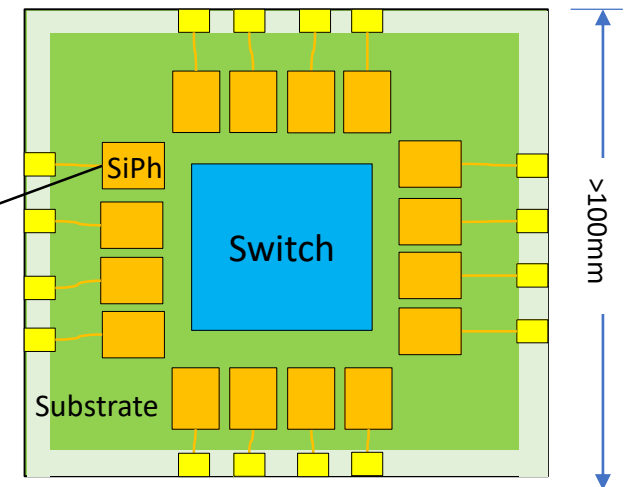


- Laser DRV/ PD TIA (65nm)
- DSP/PAM4 (16->7nm)
- All in one or separated

- Si Wave guide /modulator/ MUX/De-Mux
- Grating light coupler
- Integrated SiGe PD
- TSV /high speed connection

## Switch-SiPh Co-packaged

Integrated on Substrate



EIC+PIC ASSY

Laser/optics ASSY

Module ASSY/Fiber attach

# Co-Packaging Optics Challenges

## Ultra-high D2D Bandwidth

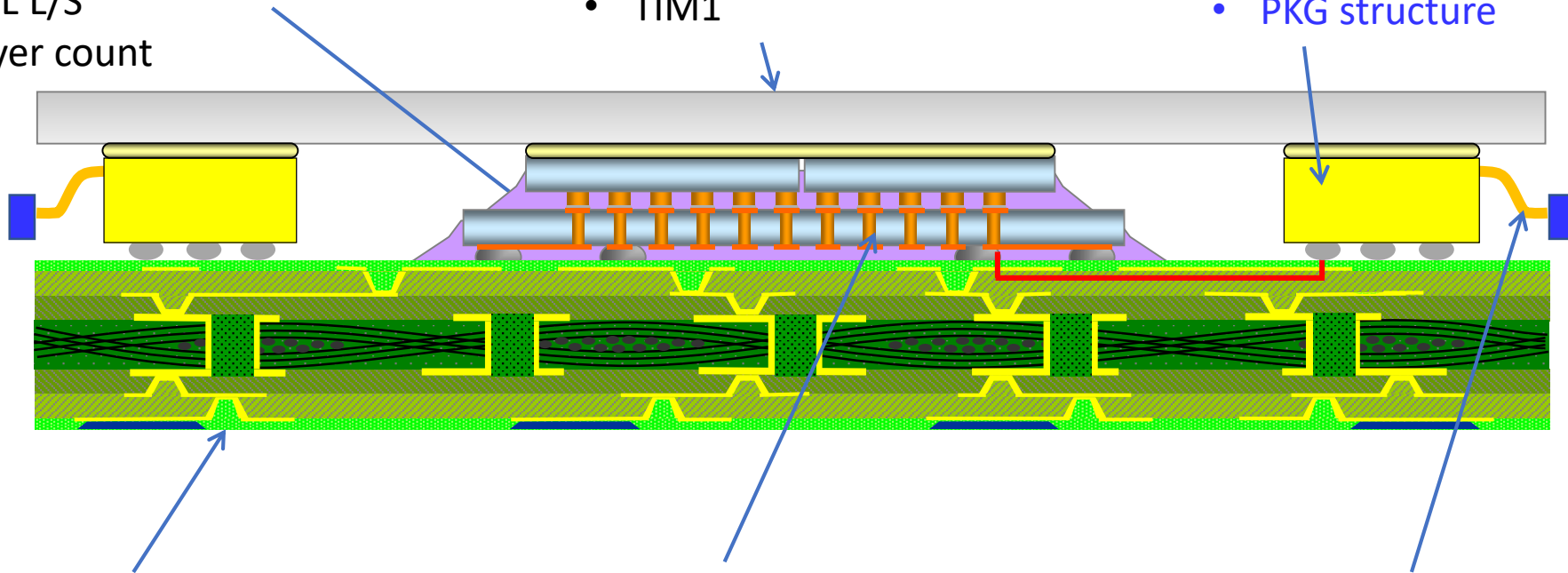
- Interconnect pitch
- RDL L/S
- Layer count

## High Power Solution

- Lid
- TIM1

## Optical engine

- Engine size/ Data rate
- PKG structure



## Super Large Package

- Package Warpage
- L2 Reliability

## Large Fan-Out / Interposer Size

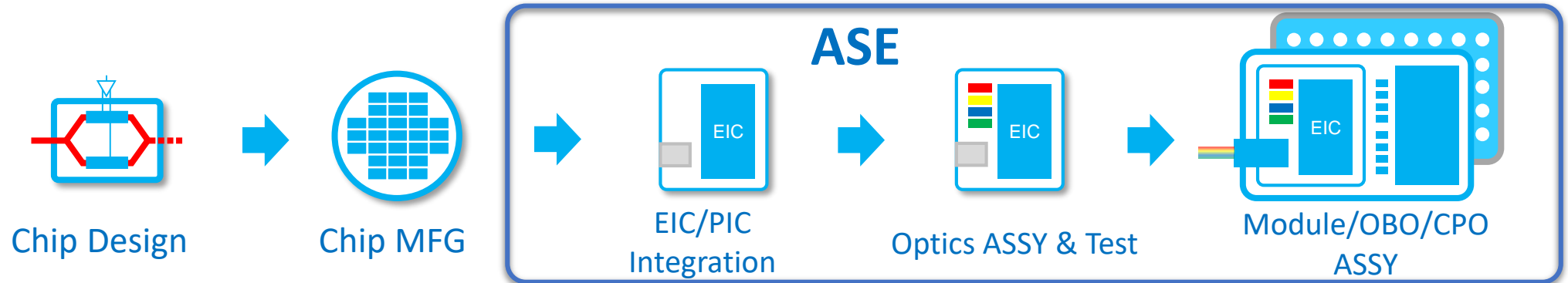
- Warpage
- Package Reliability

## Fiber Attach

- Fiber connector workability
- Warpage/ Thermal stability

# ASE Toolbox :

## Consolidate supply chain to lead to cost reduction



### Post-CMOS process

- Cu-pillar bumping
- UBM metallization
- WL dam process
- Oxide etching & DRIE
- Au mirror process
- AuSn process
- ARC film process
- KOH V-groove
- BS Via process
- Fanout process

### Wafer Level Assembly

- CoW process
- Wafer level WB assembly
- High accuracy laser attachment
- Optical components placement

### Wafer Level Test

- Wafer sorting
- Probe card design
- Test program service
- WL optical test

### Module Assembly

- SMT process
- Substrate level FC/WB
- Encapsulation
- Fiber attachment
- Housing assembly
- Module test

### Lab Service

- Electrical/Optical
- Thermal/ Stress
- Material/Chemical/FA

Specific for optical packaging

# Thank You





# SiPh Optical Engine Roadmap (Laser/Fiber/PIC/EIC)

