

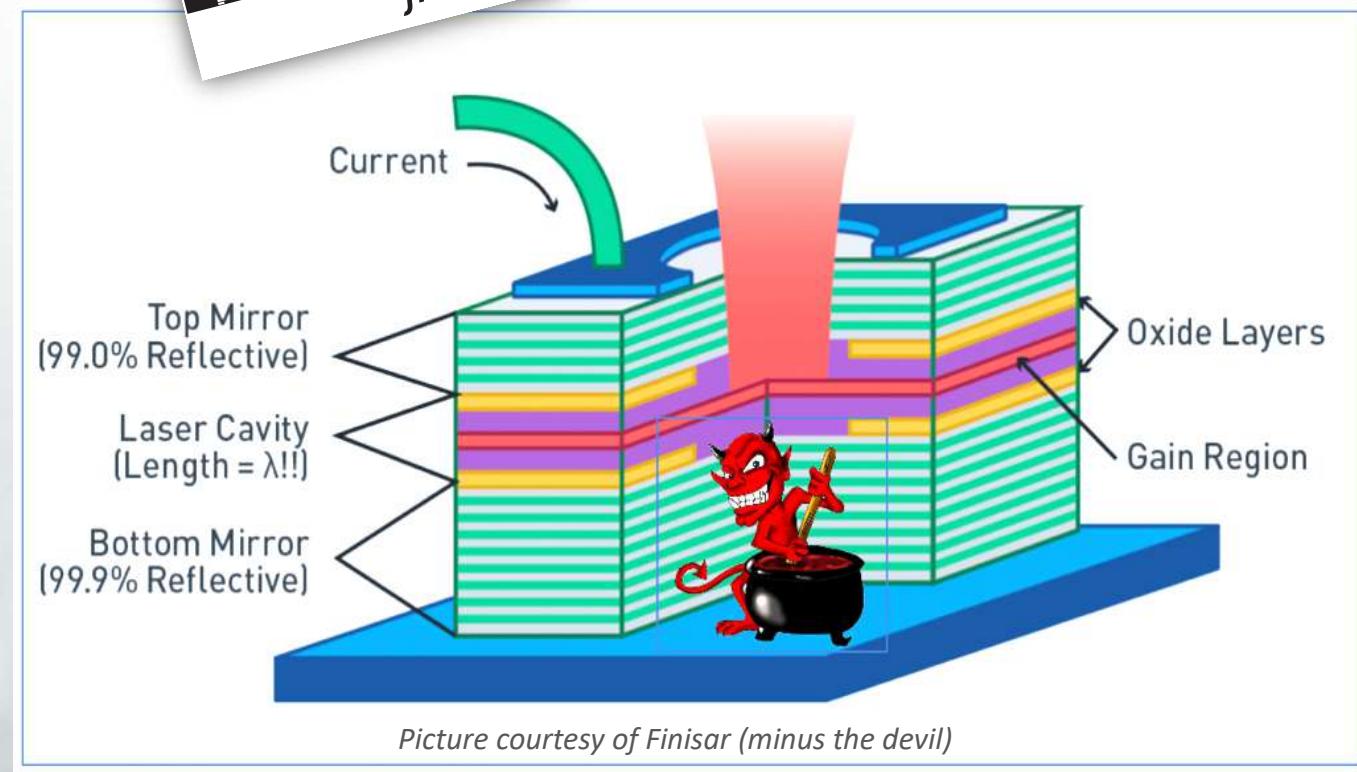
VCSEL Wafer Level Testing

EPIC Online Technology Meeting on
VCSEL Technology and Applications

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Company overview / My role

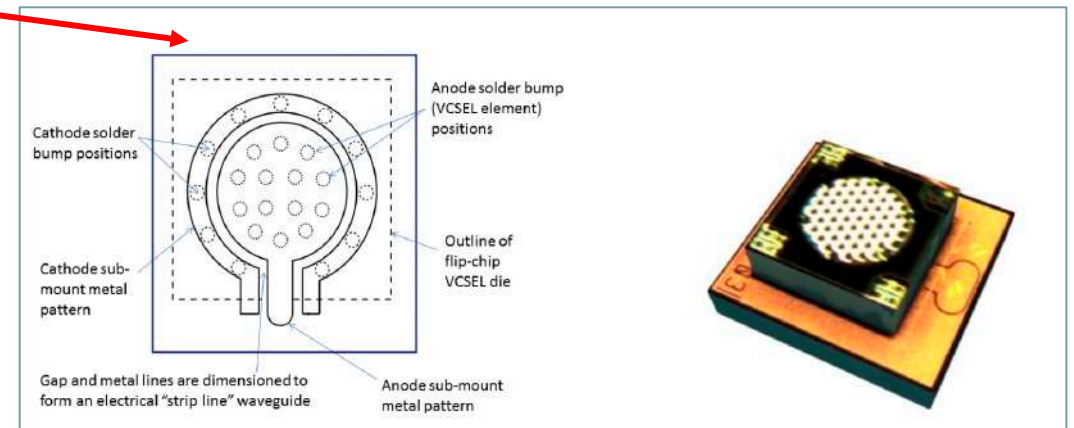
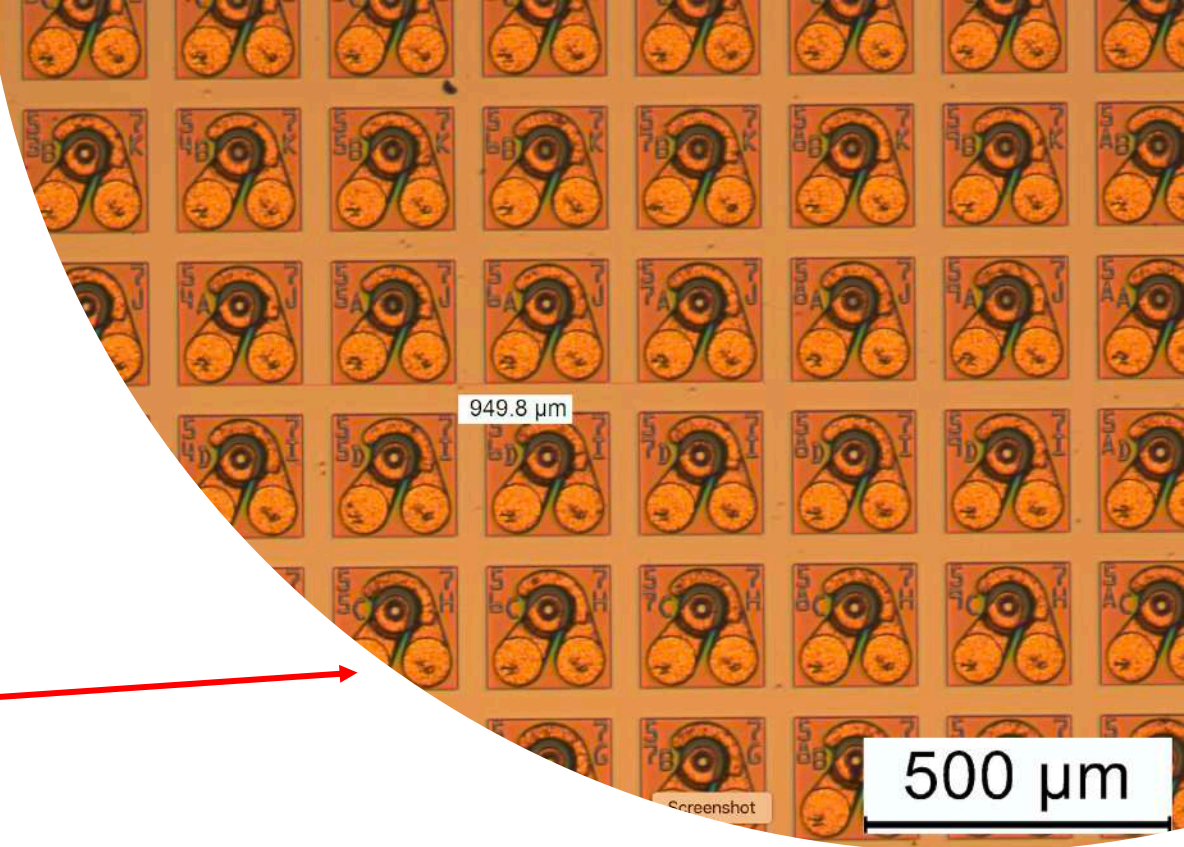
- We are better known for automated photonics packaging and assembly, but we have been engaged also with LD (edge emitting) and PICs testing for quite a while
- I have recently moved from ‘Dir. Business Development’ to ‘Principal-Photonics Testing’
- More about us on: www.ficontec.com ..



Established:	2001. 20 years of <i>#photonics_assembly_and_test</i>
Headquarter:	Achim, Germany
Offices:	USA, China, Thailand, Estonia, Ireland
Product focus:	Cyber-Physical Systems for the Assembly And Test Of Photonic Devices
Installed base:	More than 800 Machines Operational Worldwide
Organization:	>50% are Engineers of which: 30% in R&D; 60% in Engineering, Assembling and Service; 10% in Sales
Revenue:	€ 50M (2019)

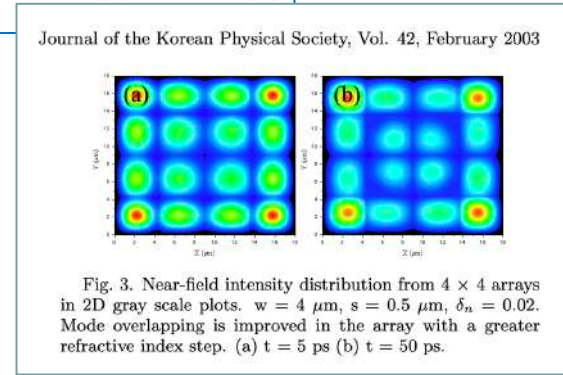
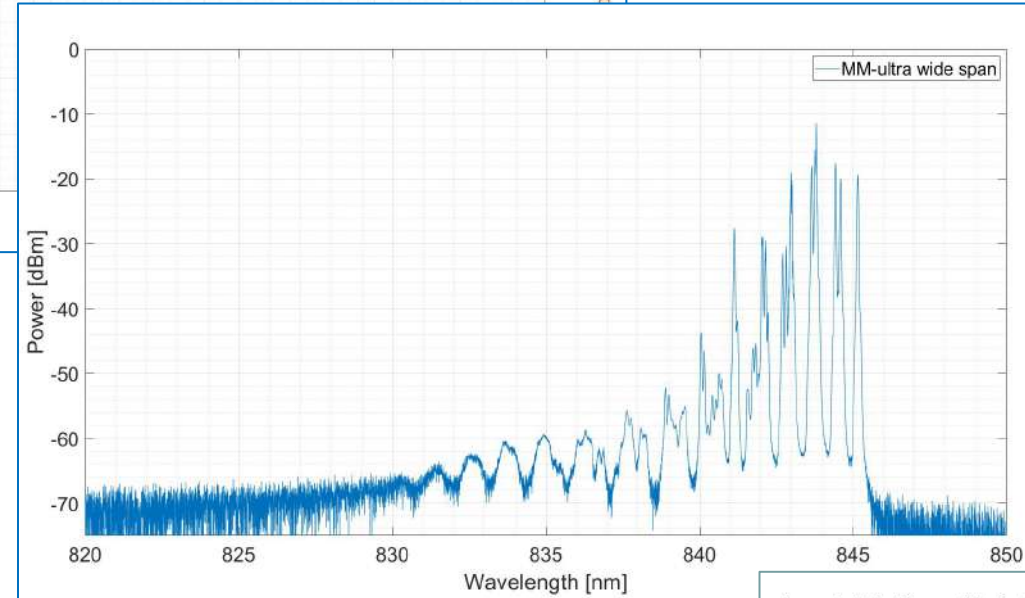
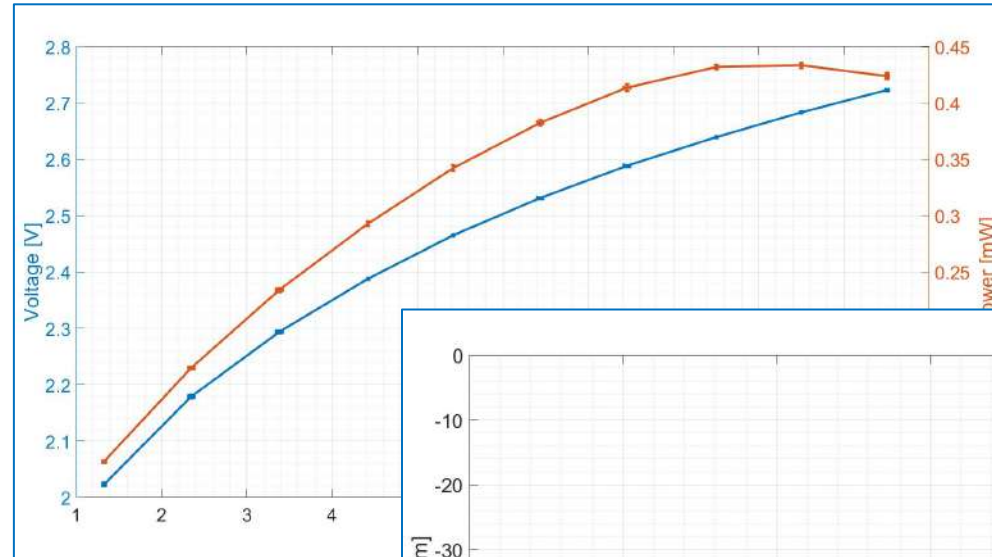
What about WL VCSEL testing?

- Topic of today: VCSELs can be found in smartphones, laptops, cars, communication links and high-resolution devices (4K). This meeting will discuss the requirements in the **design, fabrication, and packaging of VCSELs for volume applications.**
- Volume application requires volume testing: **WAFER LEVEL TESTING**
- Only two application examples here (but there are plenty more..):
 - Datacom / telecom 250 μm pitch VCSELs
 - ‘Smart illumination’ cluster of VCSELs
- On a 6” GaAs wafer (the max size for the time being, 4” for InP) there are close to a 1/4 million VCSELs
- **Cost / speed of testing becomes a major issue**



Testing what?

- Primarily:
 - LIV & spectral properties
- Additionally:
 - Near Field – Far Field
 - Modulation
 - Burn in
 - ..
- Test all you like in R&D / Test strictly what you really need in production



Beyond mechanical speed: go parallel!

- LIV and spectral measurements can be achieved in few tens of milliseconds
- Moving reliably and accurately on a 250 μm pitch requires more time
- Even considering an overall 1 s / VCSEL would take close to 70 hours on a single 6"/250.000 VCSELs wafer
- ficonTEC has been working on a scalable multi-site optical – electrical probe head
- This solution adds overall speed with less stress / extending life-time of the prober mechanics (including the replacement of electrical probe tips ..)
- NDA required to discuss details



An early - 2002 - 2" wafer VCSEL tester

Beyond integrating spheres

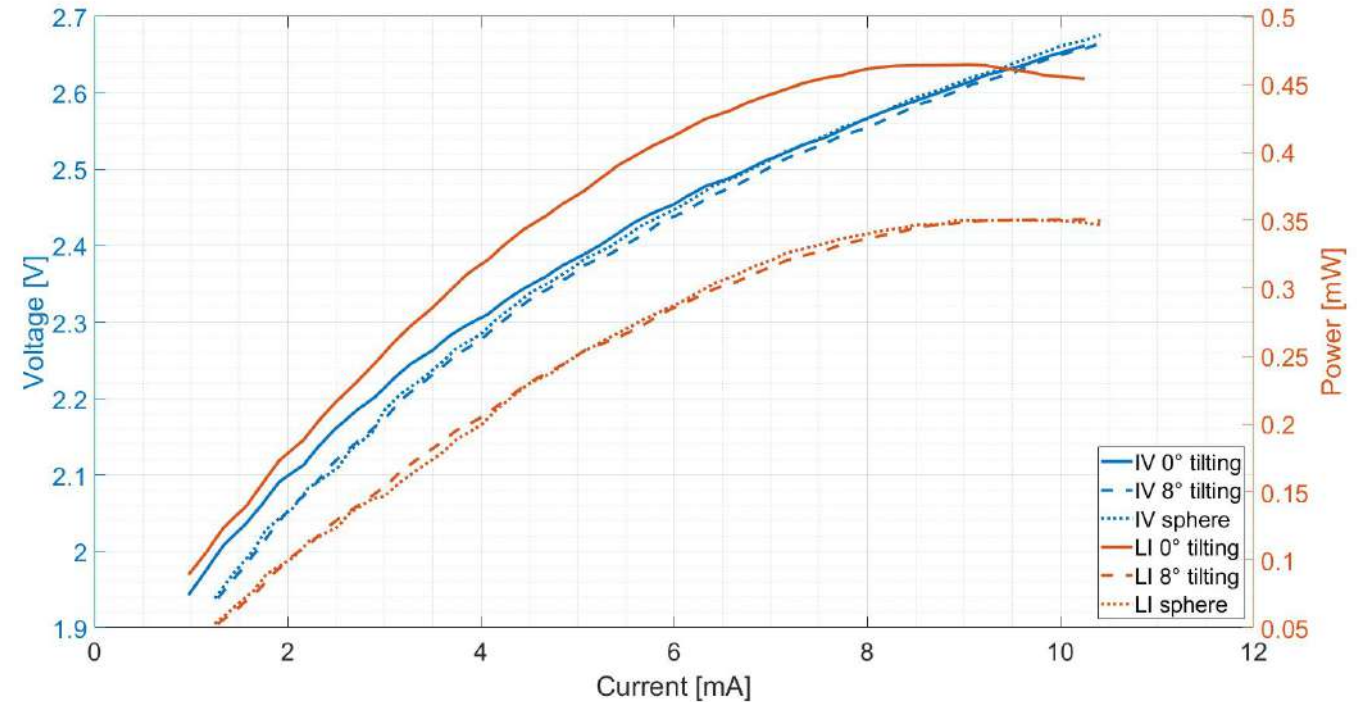
Fiber Probing – Integrating Sphere Comparison



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ficontec
photonics assembly & testing

- On horizontal cavity LD we have traditionally used integrating spheres
- This does not fit well with a wafer-level multi-site probe head solution
- Early tests have validated the FO based probe head design



Modular / scalable instrumentation

- Multi-site probe-heads offer speed but raise a need of cost-effective multi-channel instrumentation
- This applies to both VCSELs and PICs and requires modular / direct optical front-end **cost-effective** instrumentation
- A lot of software is 'hidden' in our machines, ready to interface instrumentation from vendors like Coherent Solutions, National Instruments, Keysight, ...
- **Our goal is to offer fully integrated wafer-level testing solutions:**
 - Mechanics
 - Probe-heads
 - Instrumentation
 - User-configurable Software



I hope that in these 6 min I've tickled some interest!

Any questions?

...and thanks for listening !!

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