Successfully combining VCSELs with silicon

A PhotonX Networks perspective

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Co-Founder Photonx Networks

PhotonX Networks

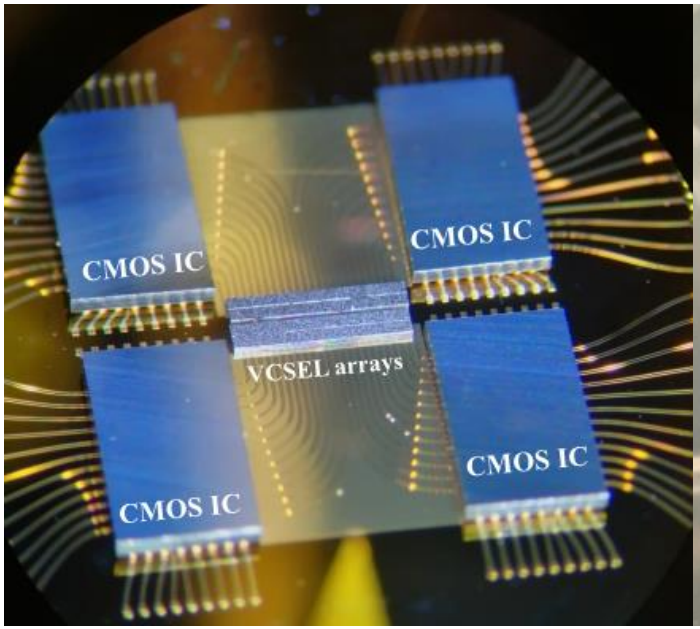
- **Founded 2013**
- **Based in Eindhoven, The Netherlands**
- **Strongly linked to the Eindhoven University of Technology (TU/e)**
- **Access to state of the art clean room**
- **Full prototyping capabilities including:**
  - **Design of package (EM simulation, mask design, etc)**
  - **Fabrication and manual assembly (clean room, Flip-Chip assembly)**
  - **Testing of E/O performance up to 56GBaud, PAM4 bit rate**

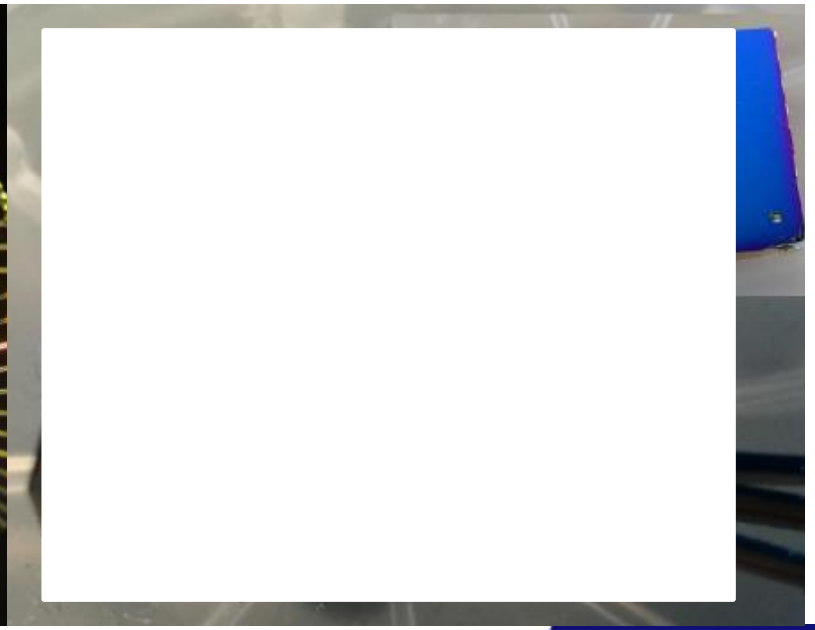
PhotonX Networks approach

- **Use off the shelf devices (KGD) for final sub-systems**
- **Come up with clever low cost packaging concepts to increase bandwidth density and make integration with ASICs/CMOS as intimate as possible**
- **Use expertise from the research work done in the TU/e for solving problems in packaging related to thermal design, co-packaging of electronics and opto-electronics and optical coupling solutions**

Unique capabilities

- Dense packaging of VCSELs
- Full wafer plating of Au and Au/Sn pads
- Dense on package fiber connectivity
- Record 48 VCSELs in 1 package





Examples of recent relevant work in TU/e

2.5D and 3D high density device integration

- **Ongoing research focus for >5 years.**
- **Three PhD projects and two EU projects supported technology development.**

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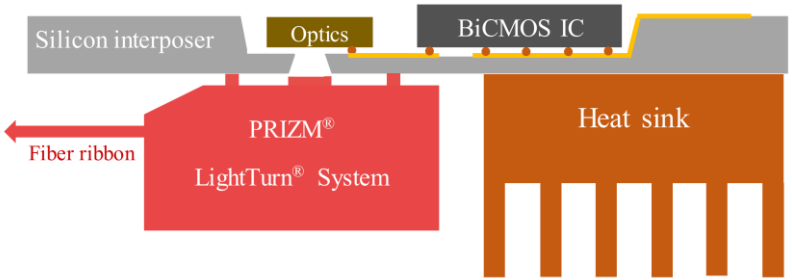
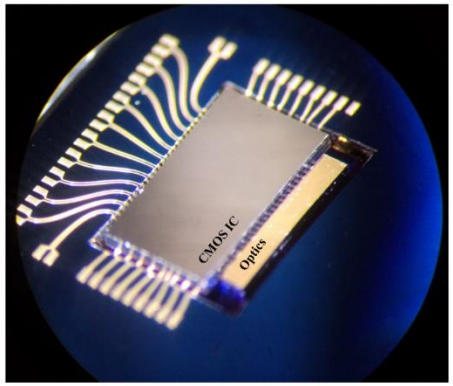
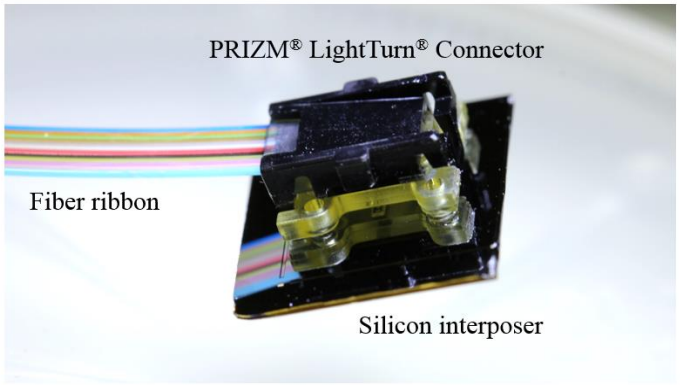
2.5D integration

- **Electrical connection to PCB/ASIC**
- **Optical connection to Optical fiber**
- **Heat transfer**



- **12-Channel 10 Gb/s Optical Transmitter and Receiver**





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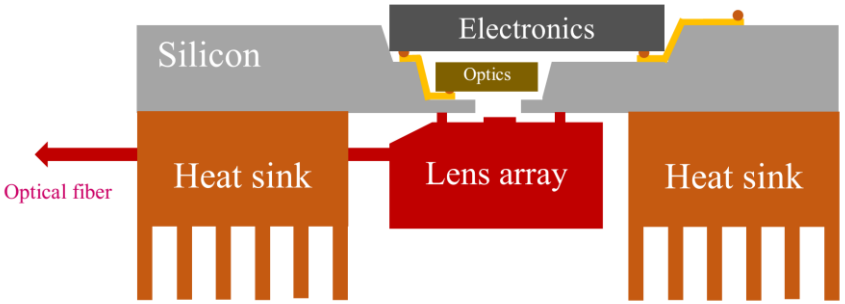
3D integration

- **Electrical/Optical connection**
- **Higher density**
- **Thermal isolation air gap**



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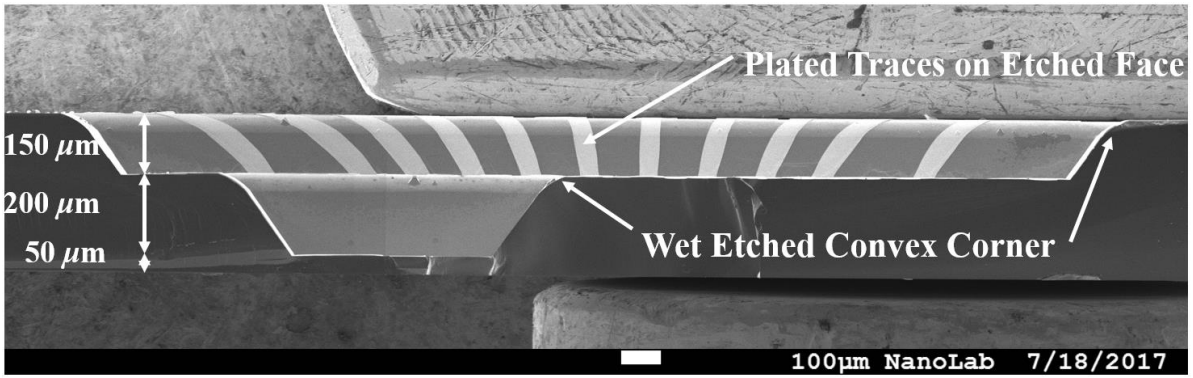

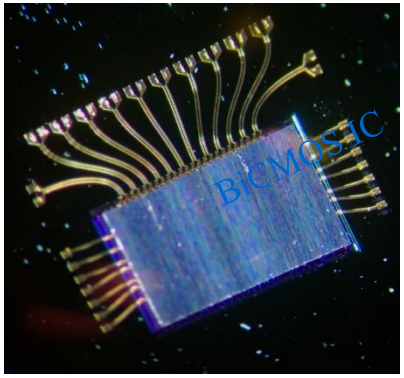

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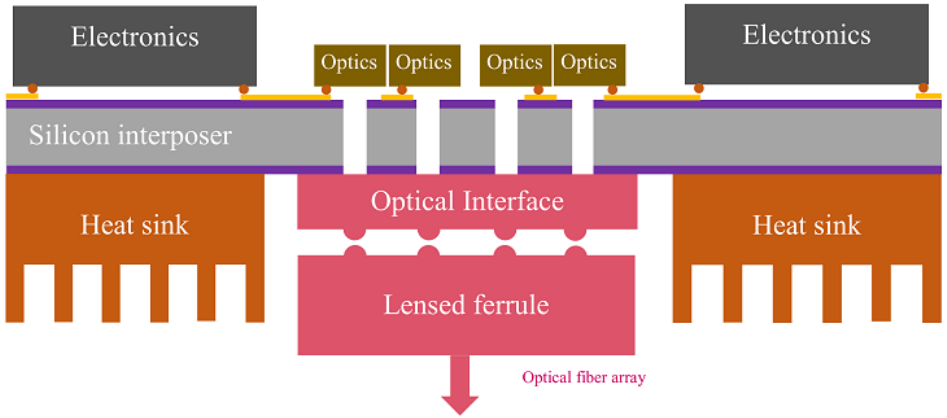
2D Optical Ports on Wet Etched Silicon Interposer

- **Optical connection**
  - **2D optical interface**
- **Electrical connection**
  - **2D arrangement**

- Higher density
  - 25 Gb/s chipset
- Higher port counts
  - 4 rows
- Low cost



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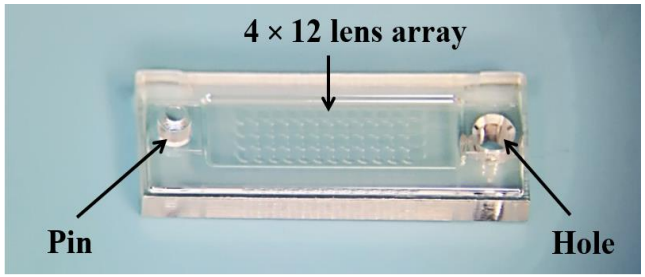
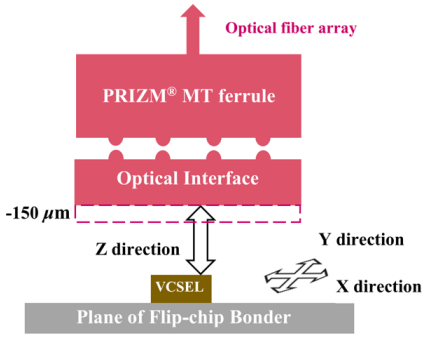
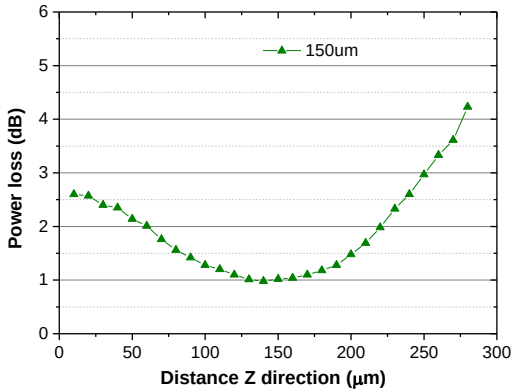
Optical Interface

- **PRIZM® MT ferrule**
  - **Lens**
  - **Channel 16-fiber / 4 rows**
- **Light coupling test**
  - **Flip-chip bonder**
  - **Minimum optical loss 0.9 dB**







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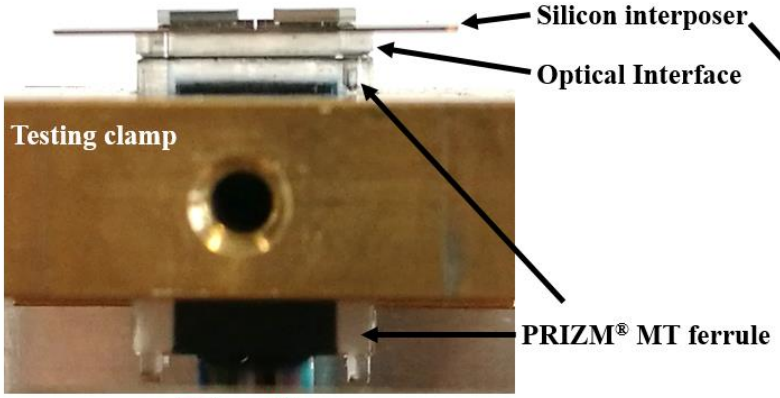
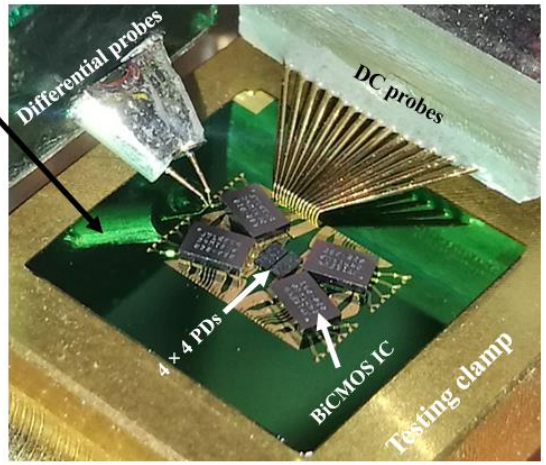
Testing

- Electrical probes
- Assembled with PRIZM® MT ferrule Fiber array outputs
- Eye patterns/ BERT
- Crosstalk





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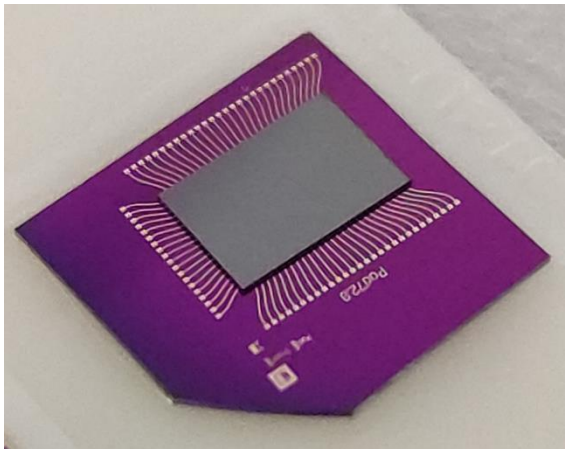
Expanding into single mode photonics

- **Recent project connecting SM 1550nm VCSEL with SiPh is running in the university (building up knowhow on the alignment challenges)**
- **Recent joint activity with Effect Photonics on co-integration of Effect Photonics dies on PhotonX silicon bench technologies**



- **Exploring opportunities also to work with customers on bespoke Bi-CMOS ICs for best in class co-design possibilities**

Conclusions

- **Very strong knowledge base created in the TU/e**
- **Research demo's are in TRL 4 and are ready for the next step**
- **Processes are suitable for wafer scale and access to fabrication and assembly facilities has been recognized**
- **If you have an optical packaging need using VCSELs we can help you!**
- **If you want to combine VCSELs with PIC we are happy to investigate the possibilities with you!**

Questions?

This presentation was presented at EPIC Meeting on VCSELs Technology and Applications 2019

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