iPRONICS
Programmable Photonics

# Field programmable photonic gate arrays:

## *A new window of opportunity for integrated photonics*

***José Capmany***

**www.ipronics.com**

# Agenda

**01** Company description & products

**02** FPPGA technology

**03** FPPGA Challenges & Applications

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# Company Description

# The Problem at Sight

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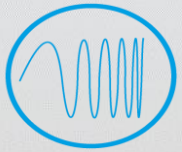
Applications that require flexible, faster and power-efficient hardware are constantly emerging.


5G and Beyond

Bio instruments

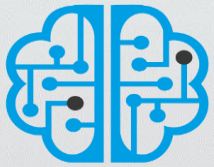

Internet of Things



HW acceleration

Sensors

Transport



Neurocomputing and AI

Quantum Information

**Electronics needs to team up with other technologies** to meet these requirements.

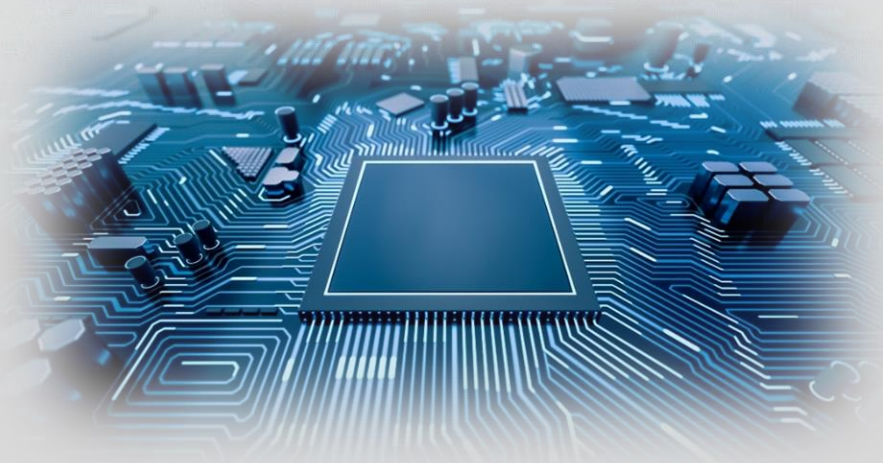
# The solution: Electronics + Photonics

**Photonics** provides bandwidth, low power consumption and is complementary to Electronics.

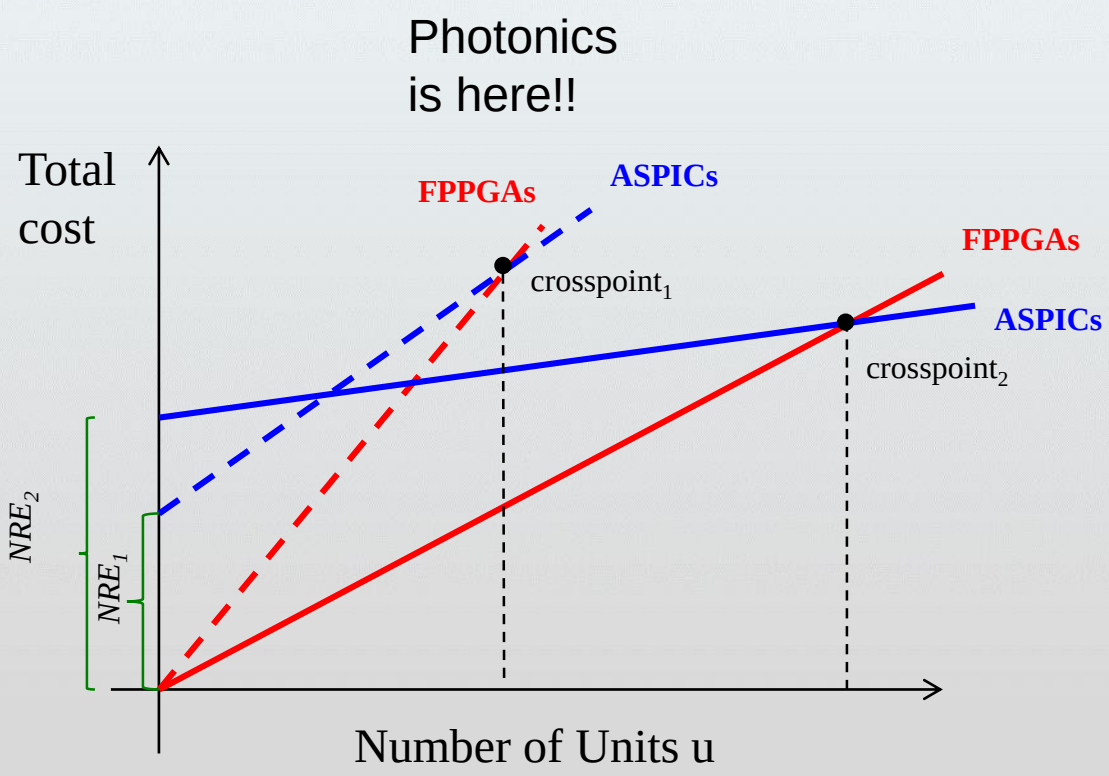
**Application-Specific Photonic Integrated Circuits** are being successfully integrated into applications yet, their time-to-market and fabrication cost can be a show stopper.

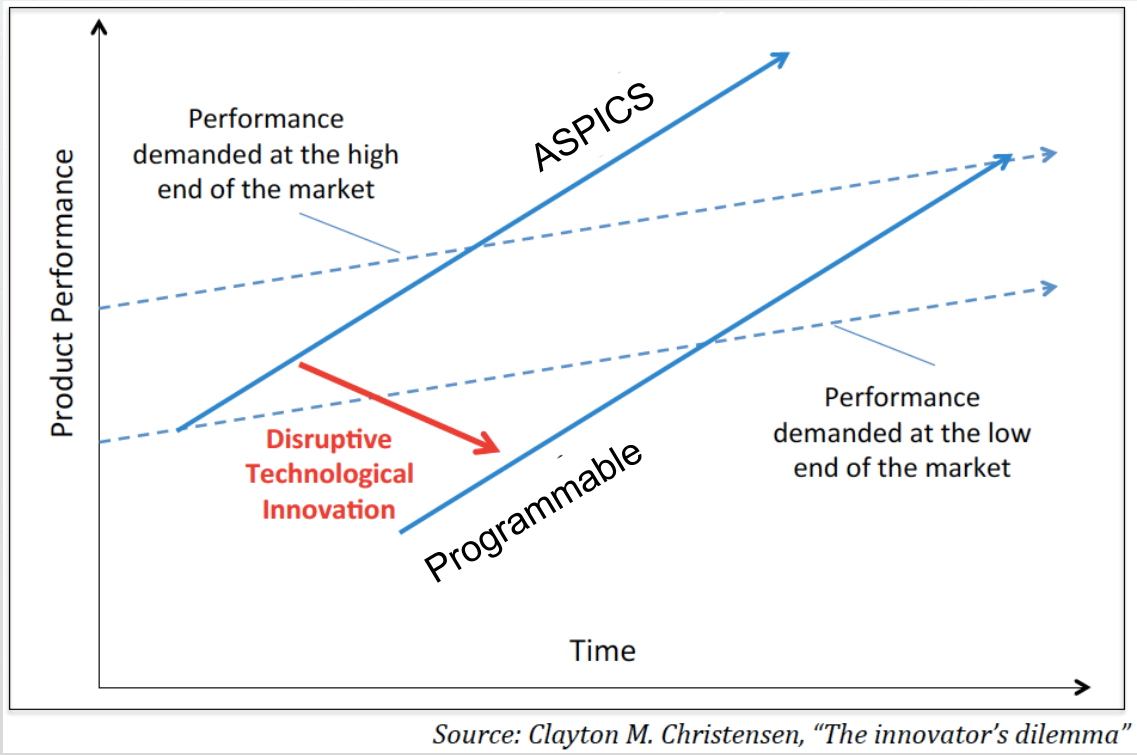
*Yet, this might be the right* time for ***Programmable Photonics!***

Solutions equivalent to FPGAs, DSPs and microprocessors will be needed.



# The solution: Electronics + Photonics




*Source: Clayton M. Christensen, "The innovator's dilemma"*

# Company Mission


*To develop and provide access to both the hardware and software of Programmable Photonic Solutions. In particular Field Programmable Photonics Gate Arrays.*


# Company Vision

*Let our customers invent the future of Integrated Photonics by expanding photonics chips into a new class of reconfigurable and multipurpose powerful light-enabled devices.*

# Products

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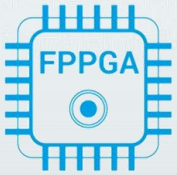
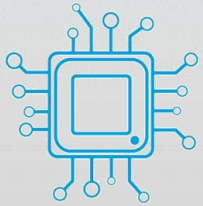



## iPRONICS FPPGA

iPronics develops the hardware of a multipurpose photonic processor including a flexible optical core and IP/High-performance blocks.

## iPRONICS SMARTLIGHT

iPronics develops the necessary software to program, control and optimize our solutions in a user-friendly yet, powerful way.



## iPRONICS BESPOKE

iPronics caters to its clients to support and assist in the adaptation of iPronics solutions to their needs.

## iPRONICS ACADEMY

iPronics strives to spread and educate in the use of its technology through special focus given by trainings, workshops and MOOCs.

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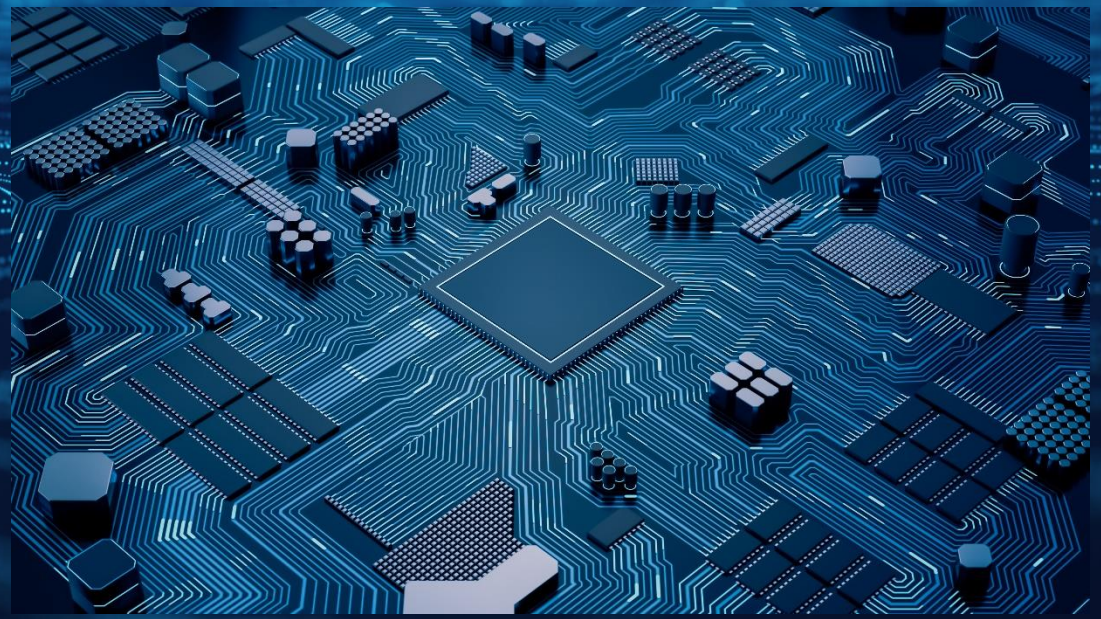
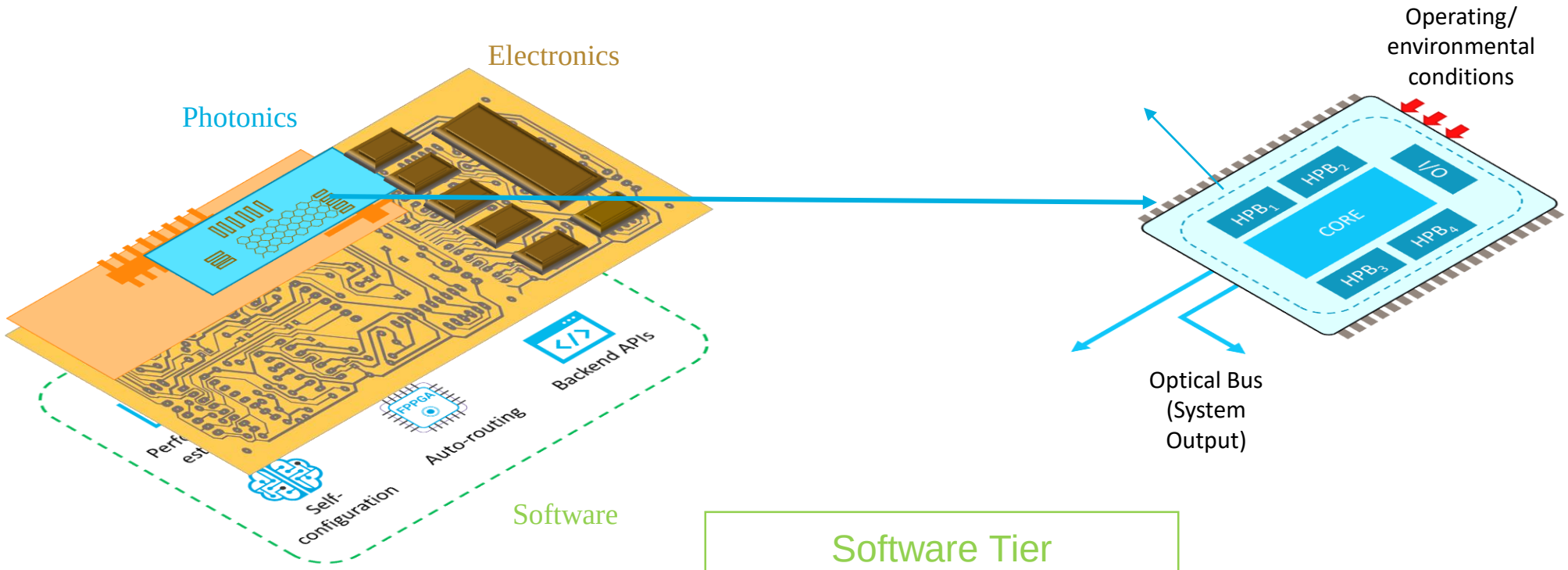
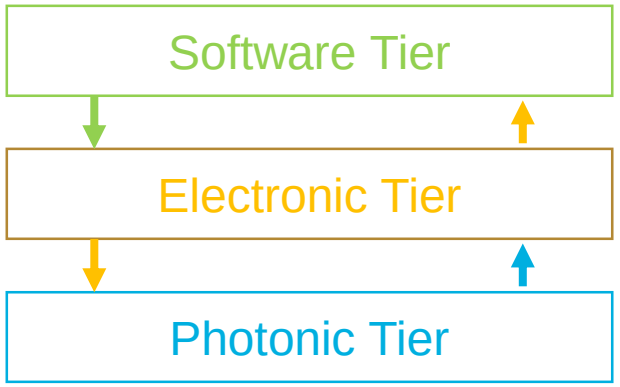
# FPPGA Technologies



# Overall device description

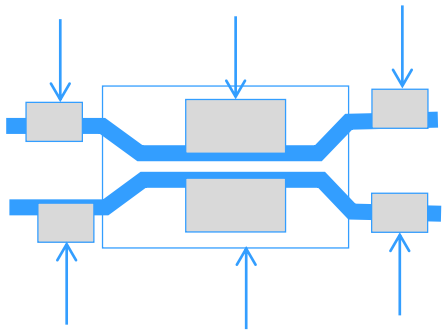


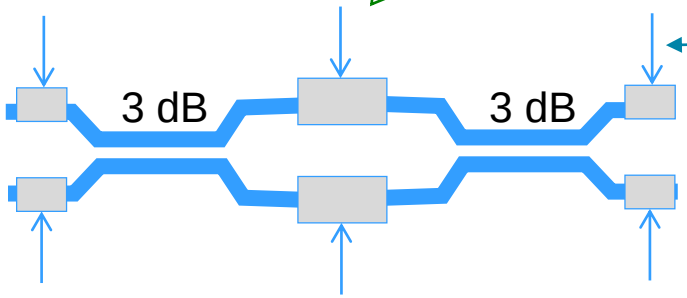



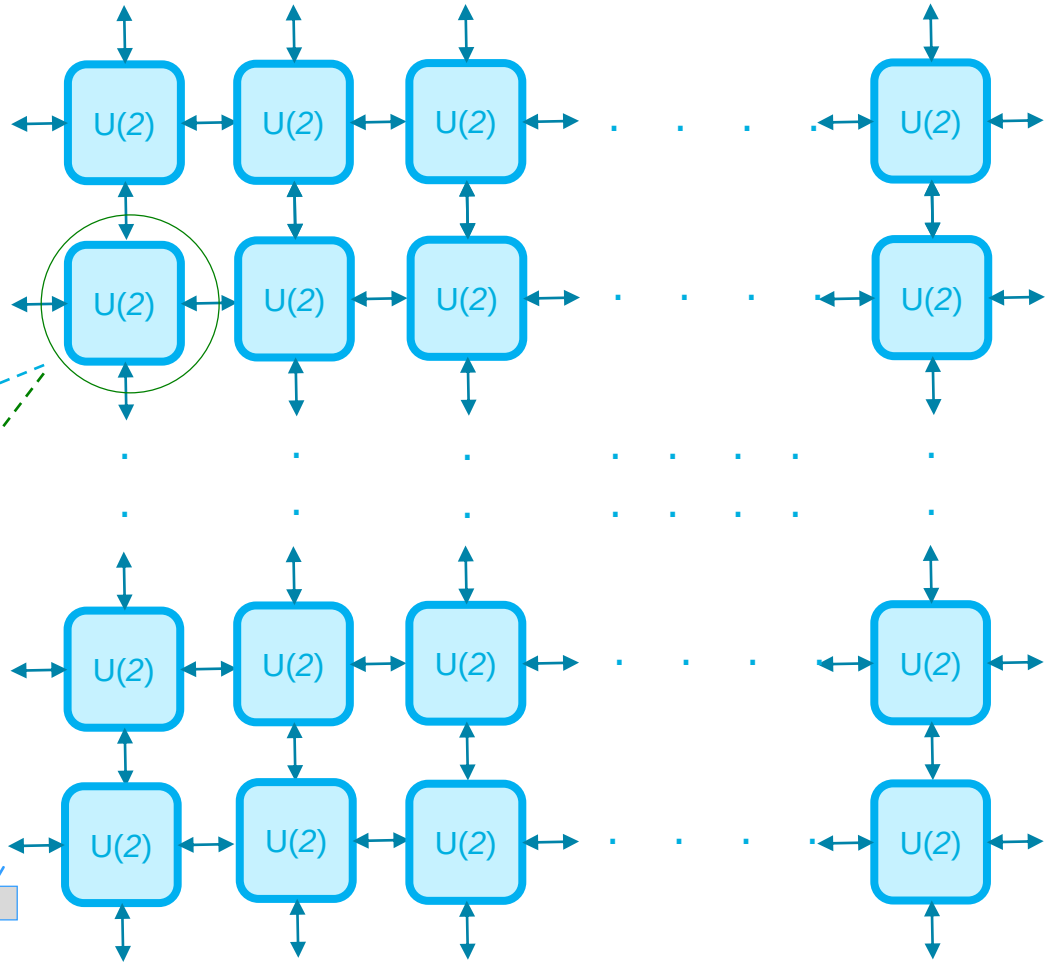
# FPPGA Photonic Tier: Core

FPPGAs are built using a 2D mesh of interconnected **reversible 2x2 unitary gates** implementing unitary analog transformations

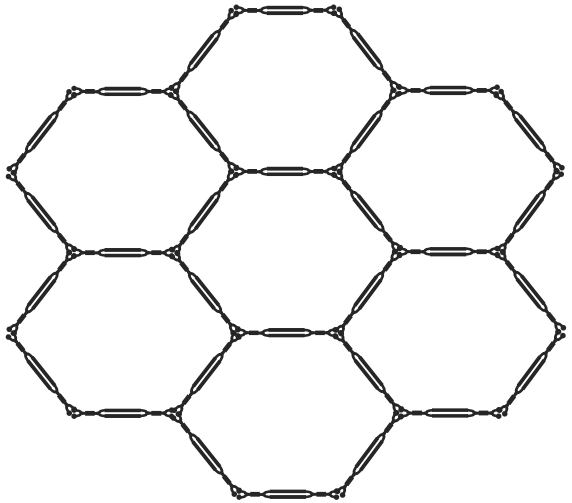
FPPGAs work with **analog signals** and unitary **2x2 matrix Algebra U(*2*)**

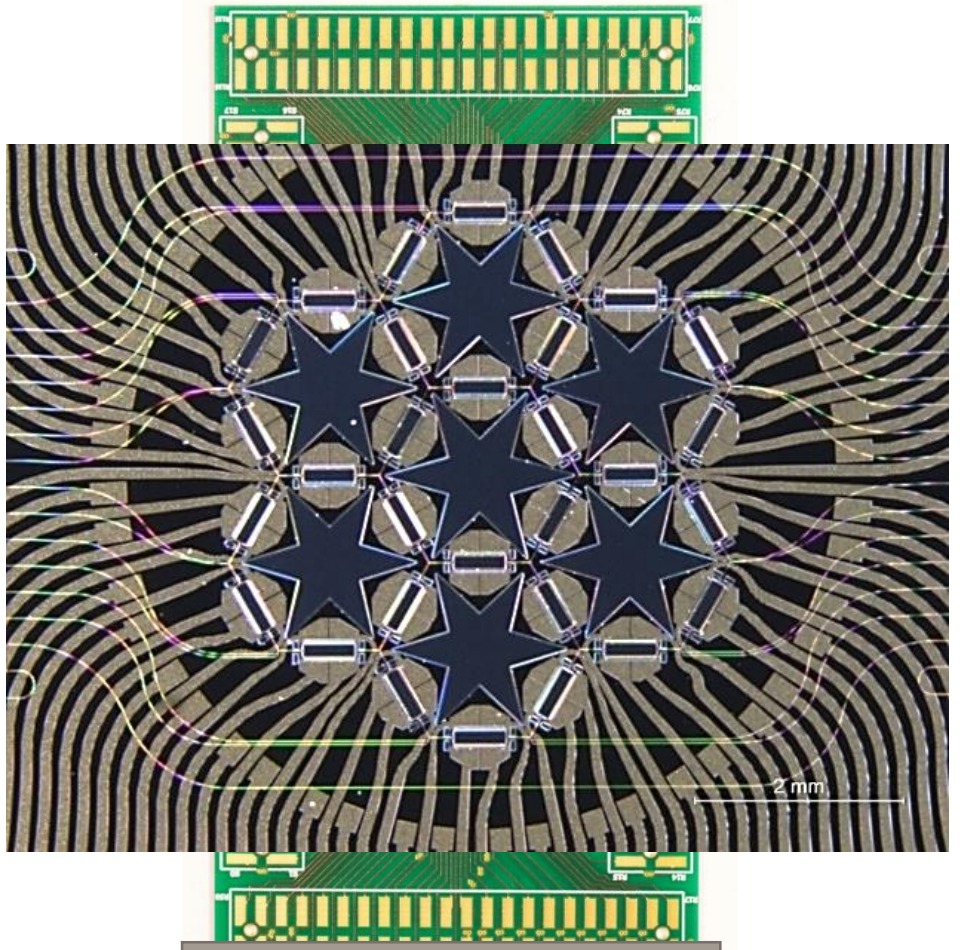




# FPPGA Photonic Tier: Core implementation






**30** programmed PICs from a potential value of 100.

Single and complex combinations of **Tunable Couplers, Delay Lines**, **MZIs**, **ORRs**,

**All, in one single chip.**

Design

Fabrication

Validation

# FPPGA Electronic Tier

Hardware for:

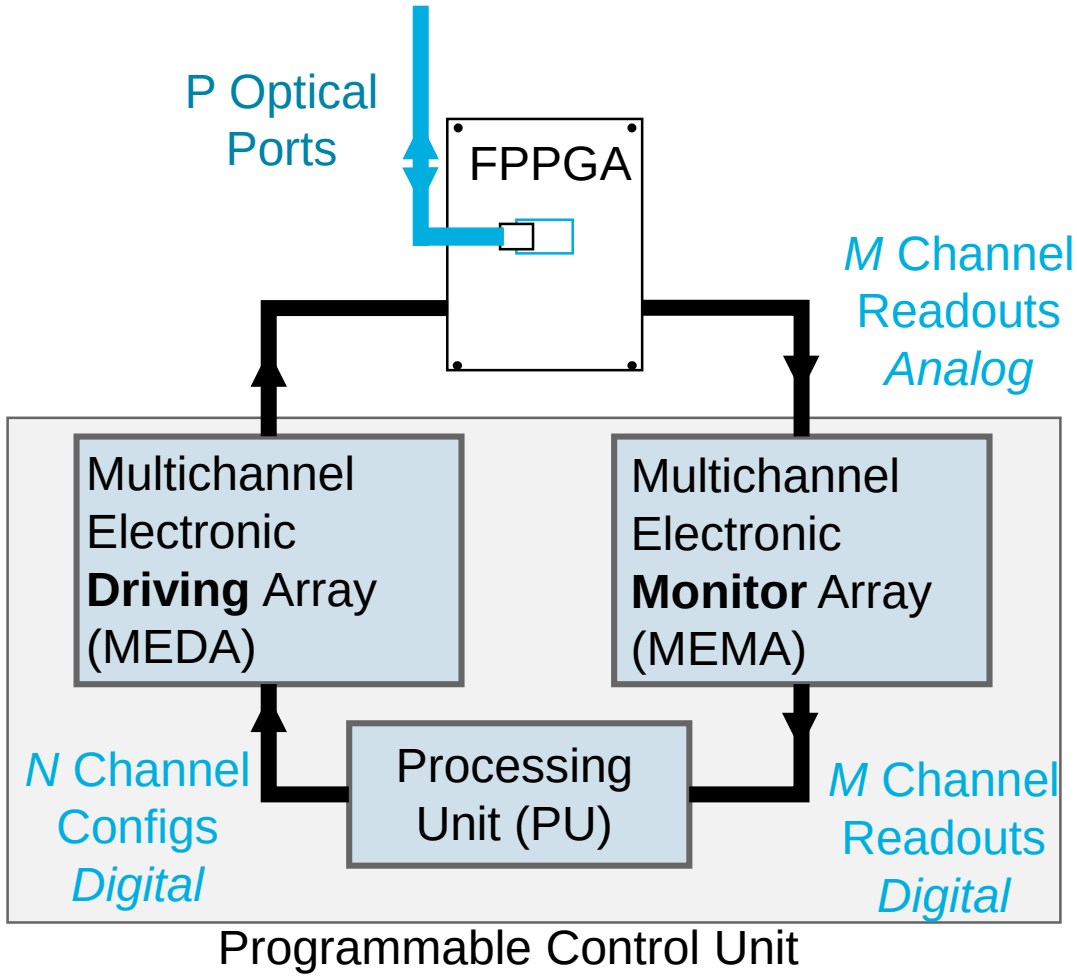
a) Monitoring from the on-chip optical readouts
b) Running the configuration algorithms
c) Driving the electro-optical actuators.

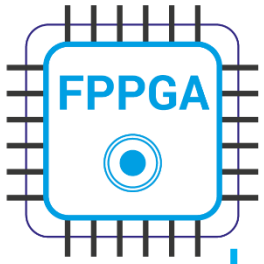
Together with the PIC, it forms a closed-loop control system,

**Processing Unit:** The PU configures and sets the signals sent to the driving system circuitry.

**Multi-channel Electronic Driving Array (MEDA):** receives a digital signal from the PU and drives the particular state of each photonic element in the FPPGA.

**Multi-channel Electronic Monitoring Array (MEMA):** This subsystem obtains electronic readouts from the FPPGA and digitizes it before passing it to the PU.






# FPPGA Software Tier

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## Low-level Layer:

Basic routines to drive the actuators and to extract on-chip readouts. These basic routines are employed as an interface by more advanced routines that enable the programming of photonic integrated circuits

## High-level layer:

### Programming Software based on **global algorithms and presets**

- Requires the pre-characterization of the FPPGA core.
- Includes preset configurations, auto-routing algorithms, user-defined configurations.

### Programming Software based on **computational optimization algorithms**

- Do not require prior knowledge. They optimize a given cost function defined over FPPGA Outputs
- Enable *self-configuring*, *self-healing*, *black-box optimizations* and ***mitigates non-ideal operation of photonic components***.

# Field Programmable Photonic Gate Array

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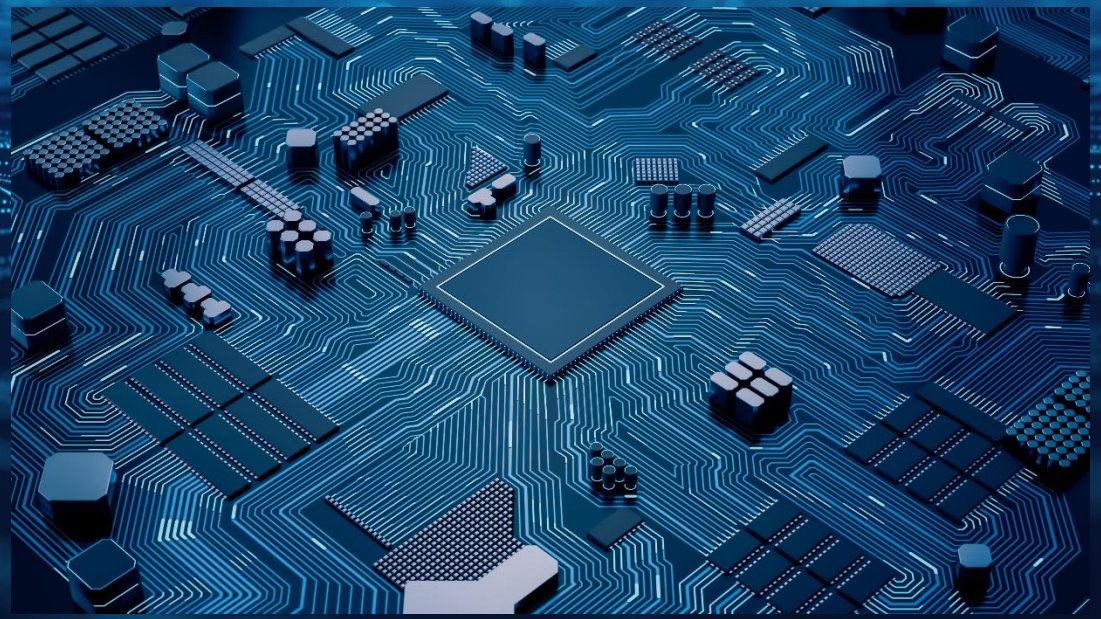
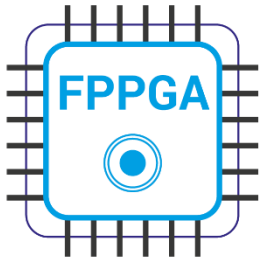
Challenges & Applications






# Hardware Scalability challenges

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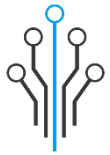
Power consumption

Accumulated optical loss

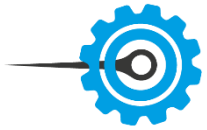


Electrical Interfacing

System integration

Packaging

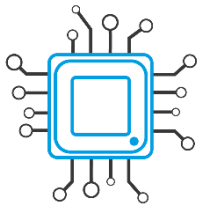
Optical monitoring points.



Optical crosstalk

Tuning crosstalk

Some of them can be mitigated by a smart software layer and thanks to the massively interconnected nature of the FPPGA core.



# Software Scalability challenges

Reconfiguration Convergence

Reconfiguration Times for

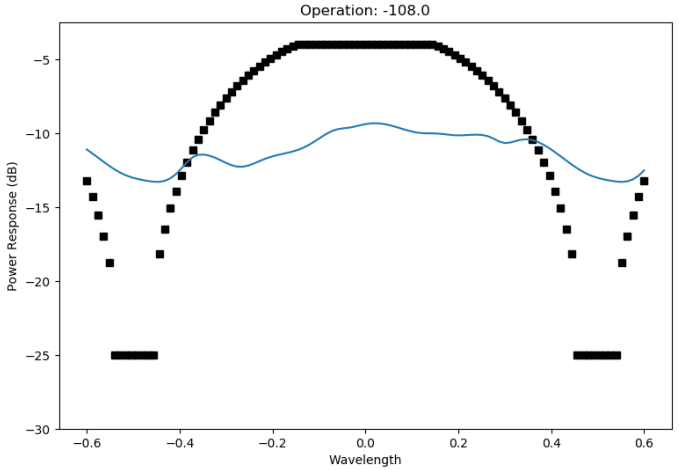
critical applications

Managing hundreds/thousands

variables requires automated solutior

Robust solutions able to manage

non ideal components




Combining all these features in

a single framework

# More Info….

## Session 3:
## Integration, Manufacturing and Photonic Circuits

Monday 3 February 2020
3:40 PM - 6:30 PM
Location: Room 76 (Lower Mezzanine South)

Session Chair: Bertrand Szelag, CEA-LETI (France)

**Towards field-programmable photonic gate arrays** *(Invited Paper)*
Paper 11284-14
Time: 5:25 PM - 5:50 PM
Author(s): Daniel Pérez López, Aitor López Hernández, Andrés Macho Ortiz, Prometheus DasMahapatra, José Capmany Francoy, Univ. Politècnica de València (Spain)

# This presentation was presented at EPIC World Photonics Technology Summit 2020

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